

# NDF03N60Z, NDD03N60Z

## N-Channel Power MOSFET 600 V, 3.6 Ω

### Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDD	Unit
Drain–to–Source Voltage	V <sub>DSS</sub>	600		V
Continuous Drain Current R <sub>θJC</sub>	I <sub>D</sub>	3.1 (Note 1)	2.6	A
Continuous Drain Current R <sub>θJC</sub> T <sub>A</sub> = 100°C	I <sub>D</sub>	2.9 (Note 1)	1.65	A
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	12	10	A
Power Dissipation R <sub>θJC</sub>	P <sub>D</sub>	27	61	W
Gate–to–Source Voltage	V <sub>GS</sub>	±30		V
Single Pulse Avalanche Energy, I <sub>D</sub> = 3.0 A	E <sub>AS</sub>	100		mJ
ESD (HBM) (JESD 22–A114)	V <sub>esd</sub>	3000		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C) (Figure 17)	V <sub>ISO</sub>	4500		V
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	3.0		A
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260		°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to 150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

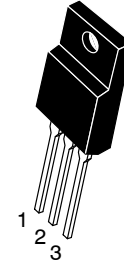
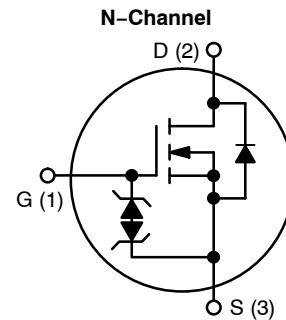
1. Limited by maximum junction temperature
2. I<sub>SD</sub> = 3.0 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, T<sub>J</sub> = +150°C



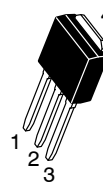
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

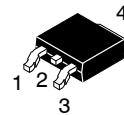
V <sub>DSS</sub>	R <sub>DS(on)</sub> (MAX) @ 1.2 A
600 V	3.6 Ω



**NDF03N60ZG,  
NDF03N60ZH  
TO-220FP  
CASE 221AH**



**NDD03N60Z-1G  
IPAK  
CASE 369D**



**NDD03N60ZT4G  
DPAK  
CASE 369AA**

### MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

# NDF03N60Z, NDD03N60Z

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit	
Junction-to-Case (Drain)	$R_{\theta JC}$	NDF03N60Z NDD03N60Z	4.7 2.0	°C/W
Junction-to-Ambient Steady State		(Note 3) NDF03N60Z (Note 4) NDD03N60Z (Note 3) NDD03N60Z-1	51 40 80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$BV_{DSS}$	600			V
Breakdown Voltage Temperature Co-efficient	Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	25°C		1	μA
			150°C		50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	$I_{GSS}$			±10	μA

### ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.2\text{ A}$	$R_{DS(on)}$		3.3	3.6	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0	3.9	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 1.5\text{ A}$	$g_{FS}$		2.0		S

### DYNAMIC CHARACTERISTICS

Input Capacitance (Note 6)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	$C_{iss}$	248	312	372	pF
Output Capacitance (Note 6)		$C_{oss}$	30	39	50	
Reverse Transfer Capacitance (Note 6)		$C_{rss}$	4	8	12	
Total Gate Charge (Note 6)	$V_{DD} = 300\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 10\text{ V}$	$Q_g$	6	12	18	nC
Gate-to-Source Charge (Note 6)		$Q_{gs}$	1.5	2.5	4	
Gate-to-Drain ("Miller") Charge (Note 6)		$Q_{gd}$	3	6.1	9	
Plateau Voltage		$V_{GP}$		6.4		
Gate Resistance		$R_g$		6.0		Ω

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		9		ns
Rise Time		$t_r$		8		
Turn-Off Delay Time		$t_{d(off)}$		16		
Fall Time		$t_f$		10		

### SOURCE-DRAIN DIODE CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 3.0\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 3.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$		265		ns
Reverse Recovery Charge		$Q_{rr}$		0.9		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Width  $\leq 380\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Guaranteed by design.

# NDF03N60Z, NDD03N60Z

## TYPICAL CHARACTERISTICS

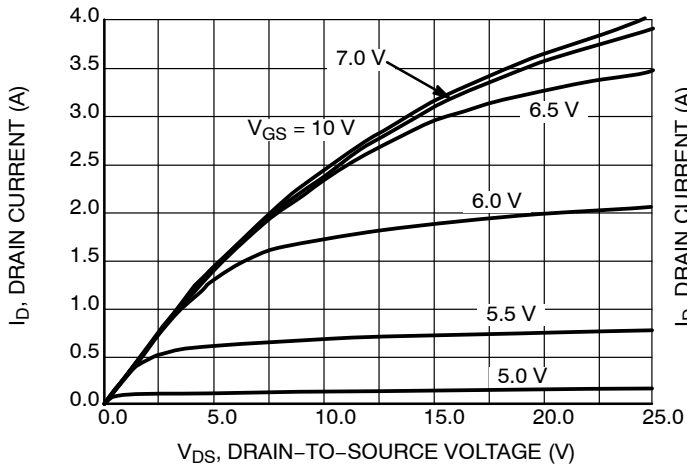


Figure 1. On-Region Characteristics

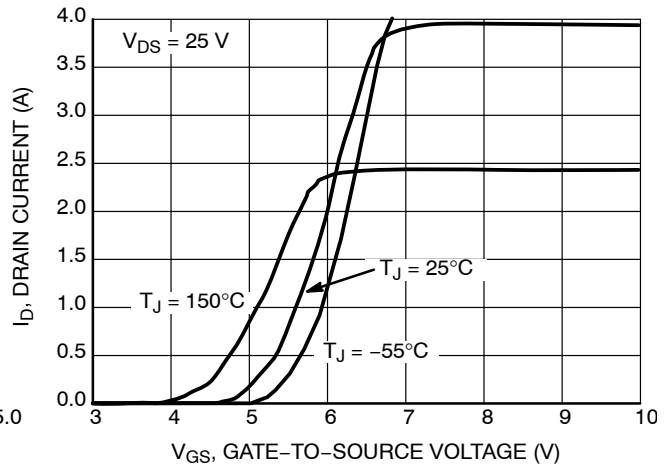


Figure 2. Transfer Characteristics

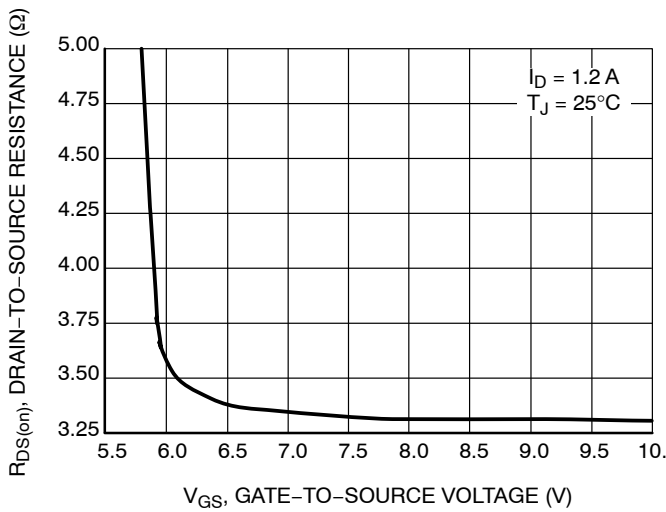


Figure 3. On-Region versus Gate-to-Source Voltage

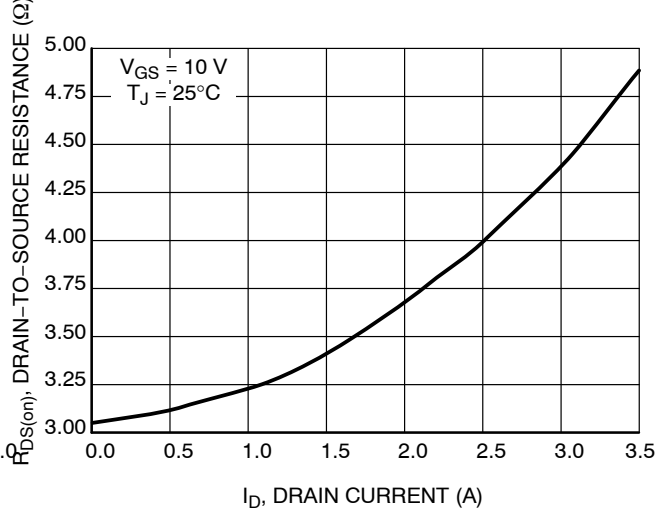


Figure 4. On-Resistance versus Drain Current and Gate Voltage

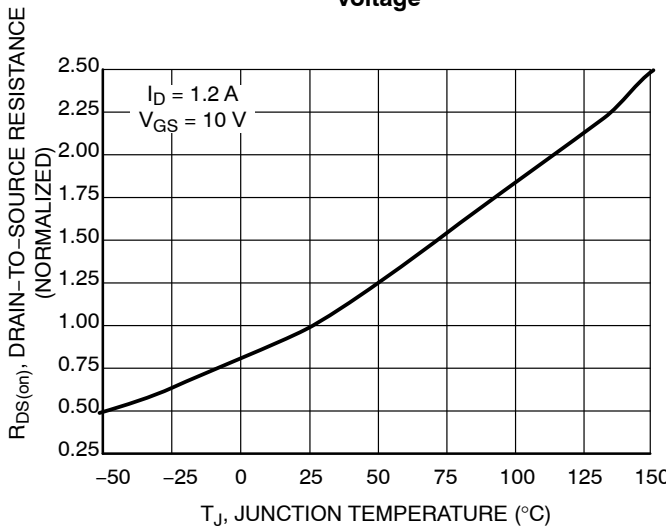


Figure 5. On-Resistance Variation with Temperature

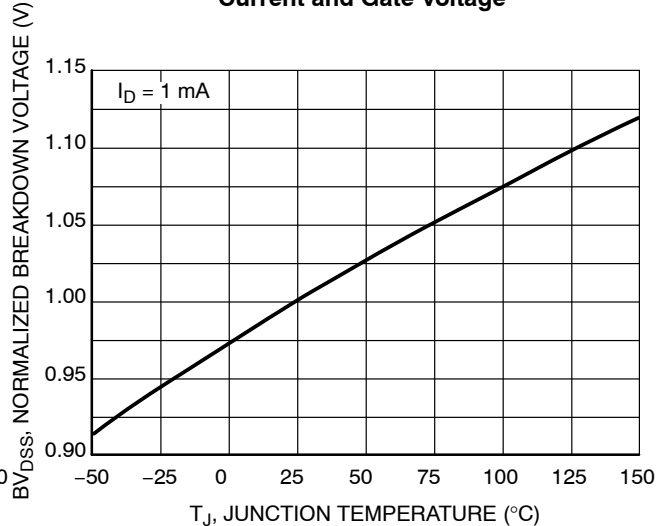
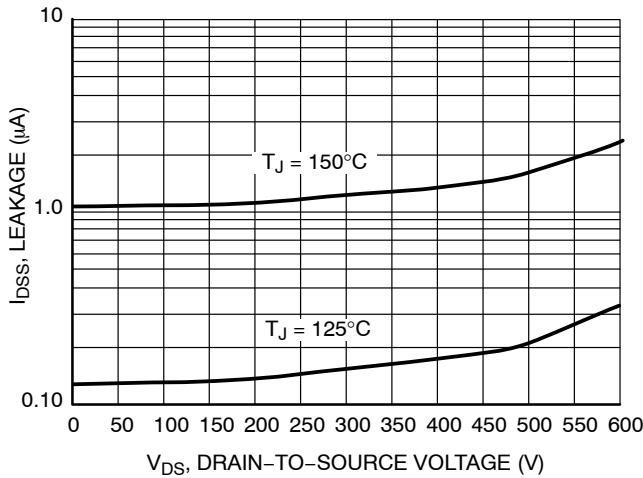


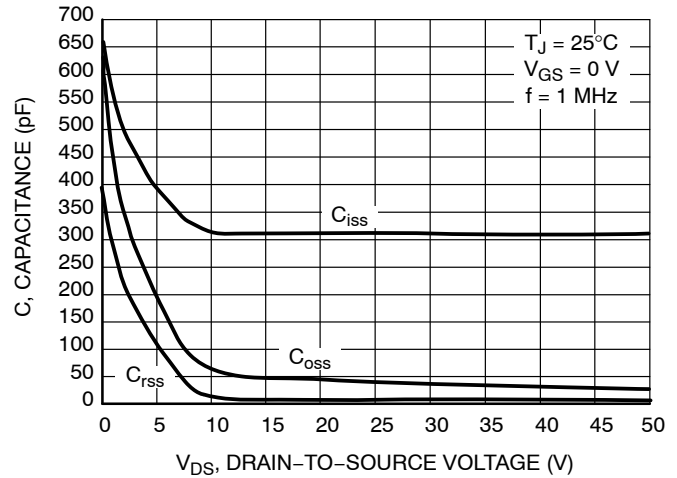
Figure 6.  $BV_{DSS}$  Variation with Temperature

# NDF03N60Z, NDD03N60Z

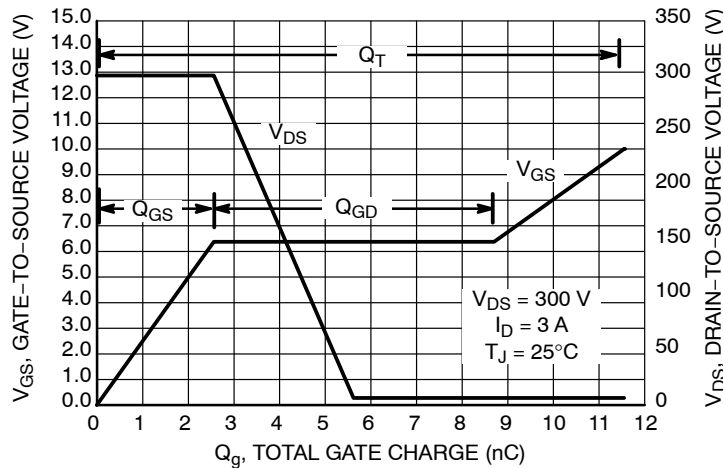
## TYPICAL CHARACTERISTICS



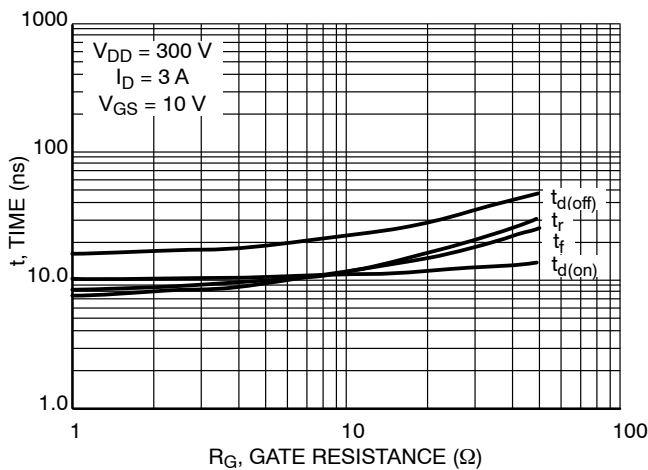
**Figure 7. Drain-to-Source Leakage Current versus Voltage**



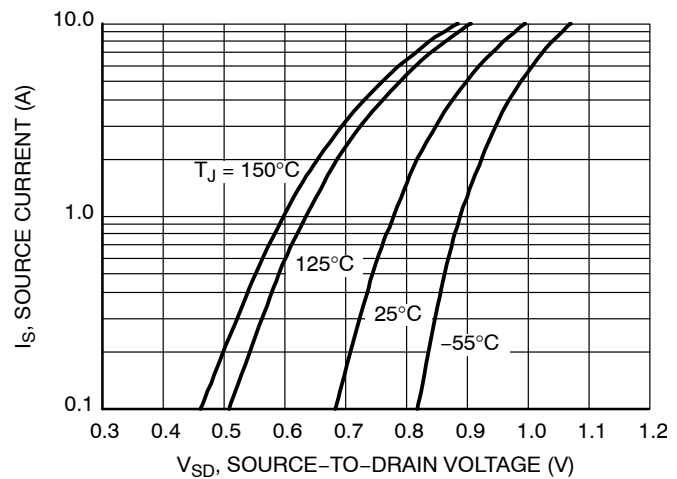
**Figure 8. Capacitance Variation**



**Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge**



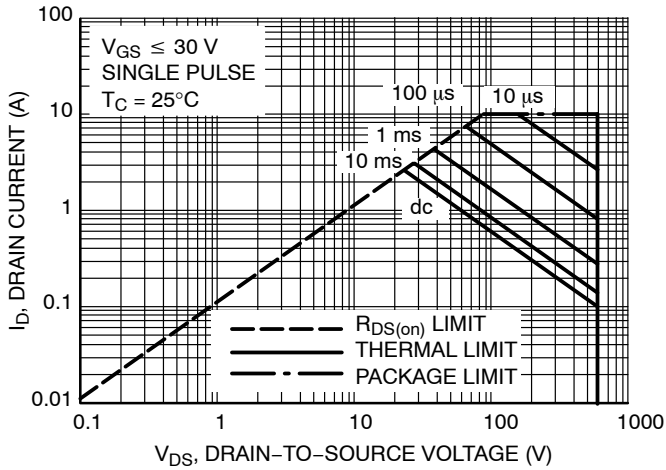
**Figure 10. Resistive Switching Time Variation versus Gate Resistance**



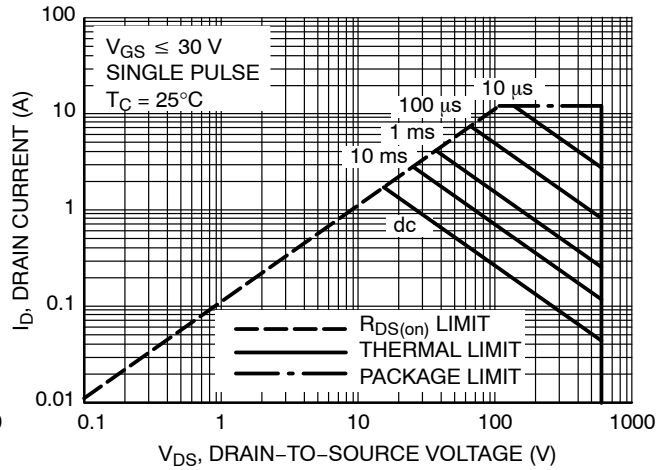
**Figure 11. Diode Forward Voltage versus Current**

# NDF03N60Z, NDD03N60Z

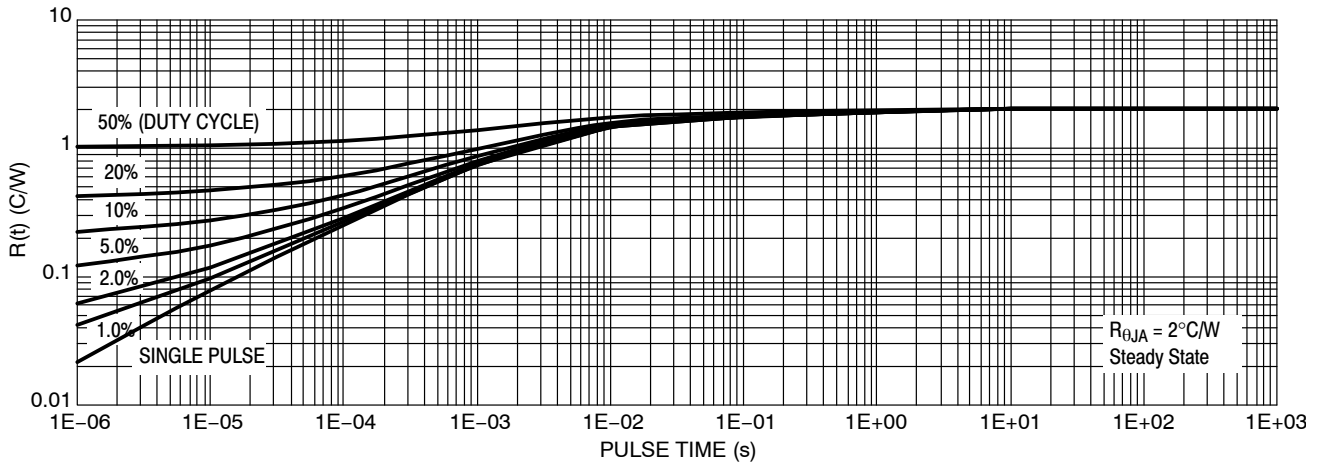
## TYPICAL CHARACTERISTICS



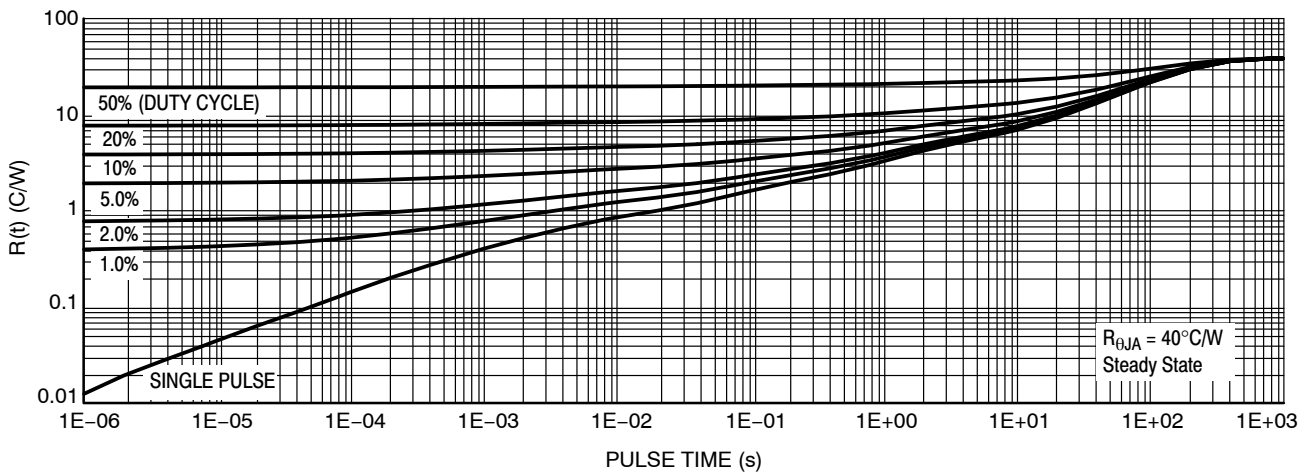
**Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD03N60Z**



**Figure 13. Maximum Rated Forward Biased Safe Operating Area NDF03N60Z**



**Figure 14. Thermal Impedance (Junction-to-Case) for NDD03N60Z**



**Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD03N60Z**

# NDF03N60Z, NDD03N60Z

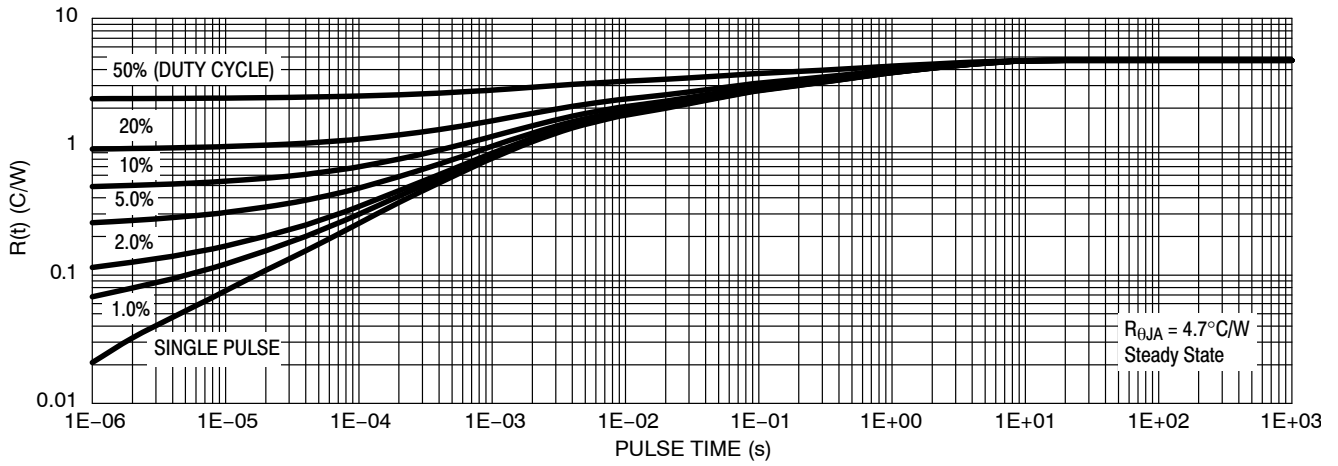


Figure 16. Thermal Impedance (Junction-to-Case) for NDF03N60Z

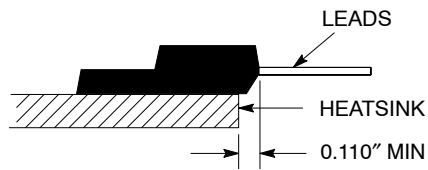


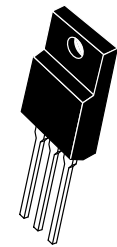
Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

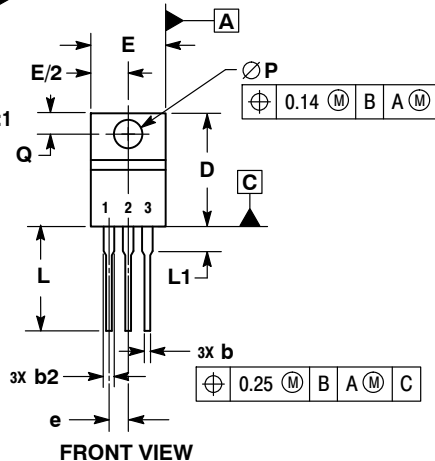
\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TO-220 FULLPACK, 3-LEAD  
CASE 221AH  
ISSUE F

DATE 30 SEP 2014



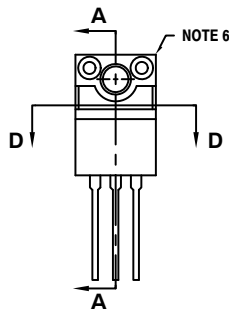
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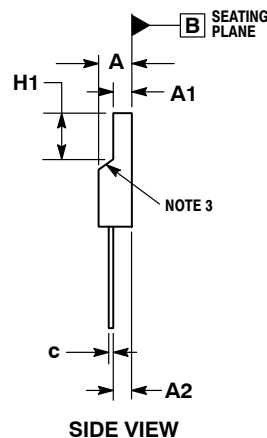
FRONT VIEW



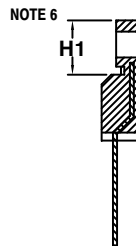
SECTION D-D



ALTERNATE CONSTRUCTION



SIDE VIEW



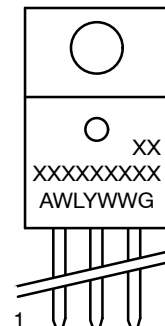
SECTION A-A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

MILLIMETERS		
DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

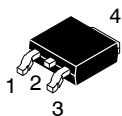
1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

1. CATHODE
2. ANODE
3. GATE

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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD	PAGE 1 OF 1

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DPAK-3 6.10x6.54x2.28, 2.29P  
CASE 369AA  
ISSUE C

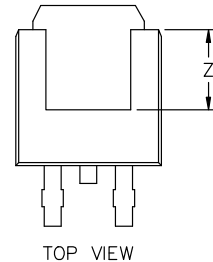
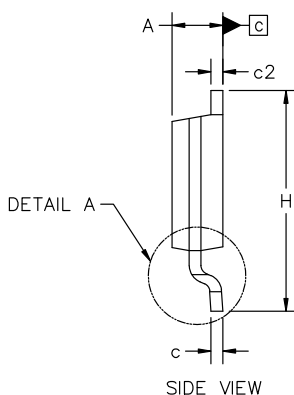
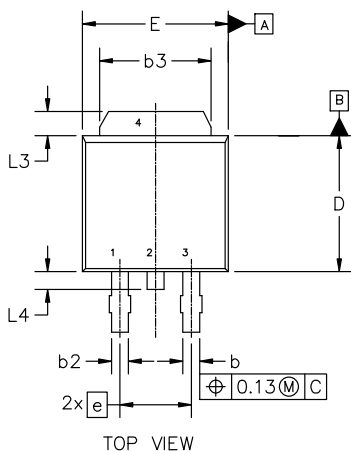
DATE 14 MAY 2026

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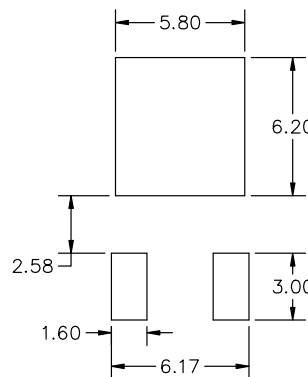
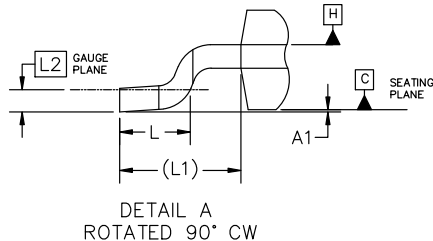
NOTES

1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H

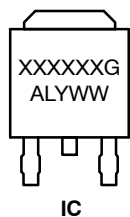
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.76	0.95	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



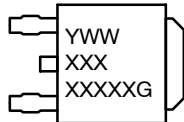
RECOMMENDED MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM\*



IC



Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

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DESCRIPTION:	DPAK-3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 1

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