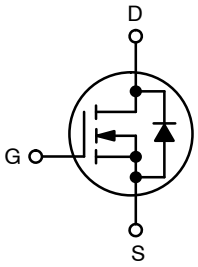
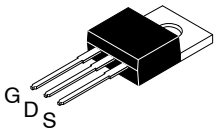
MOSFET – N-Channel, Field Effect Transistor, Enhancement Mode

NDP6060L / NDB6060L

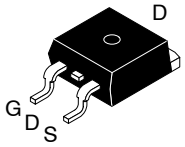
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
60 V	0.025 mΩ @ 5 V	48 A



N–CHANNEL MOSFET



TO–220–3LD
CASE 340AT



D2PAK–3
(TO–263, 3–LEAD)
CASE 418AJ

General Description

These logic level N–Channel enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on–state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in–line power loss, and resistance to transients are needed.

Features

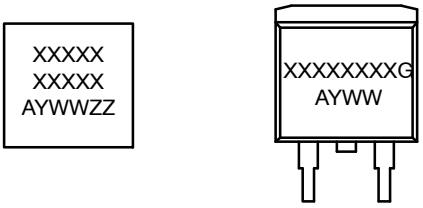
- 48 A, 60 V
  - $R_{DS(ON)}$ = 0.025 mΩ @ V_{GS} = 5 V
- Low Drive Requirements Allowing Operation Directly from Logic Drivers. $V_{GS(TH)}$ < 2.0 V
- Critical DC Electrical Parameters Specified at Elevated Temperature
- Rugged Internal Source–Drain Diode Can Eliminate the Need for an External Zener Diode Transient Suppressor
- 175°C Maximum Junction Temperature Rating
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- TO–220 and TO–263 (D^2PAK) Package for Both Through Hole and Surface Mount Applications
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Rating	NDP6060L / NDB6060L	Unit
V_{DSS}	Drain–Source Voltage	60	V
V_{DGR}	Drain–Gate Voltage (R_{GS} ≤ 1 MΩ)	60	V
V_{GSS}	Drain–Source Voltage – Continuous – Nonrepetiti (t_p < 50 μs)	 ±16 ±25	V
I_D	Drain Current – Continuous – Pulsed	 48 144	A
P_D	Total Power Dissipatiion @ T_C = 25°C	100	W
	– Derate above 25°C	0.67	W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	–65 to 175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NDP6060L	TO–220–3LD (Pb–Free / Halide Free)	800 / Units / Tube
NDB6060L	D2PAK–3 (TO–263, 3–LEAD) (Pb–Free)	800 / Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DRAIN−SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain−Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A	–	–	200	mJ
I_{AR}	Maximum Drain−Source Avalanche Current		–	–	48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	–	–	250	μA
		T_J = 125°C	–	–	1	mA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −16 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	–	2	V
		T_J = 125°C	0.65	–	1.5	
$R_{DS(ON)}$	Static Drain−Source On−Resistance	V_{GS} = 5 V, I_D = 24 A	–	–	0.025	W
		T_J = 125°C	–	–	0.04	
		V_{GS} = 10 V, V_{DS} = 24 A	–	–	0.02	W
$I_{D(on)}$	On−State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	48	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A	10	–	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	1630	2000	pF
C_{oss}	Output Capacitance		–	460	800	pF
C_{rss}	Reverse Transfer Capacitance		–	150	400	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn − On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 5 V, R_{GEN} = 15 Ω, R_{GS} = 15 Ω	–	15	30	nS
t_r	Turn − On Rise Time		–	320	500	nS
$t_{D(off)}$	Turn − Off Delay Time		–	49	100	nS
tf	Turn − Off Fall Time		–	161	300	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 48 A, V_{GS} = 5 V	–	36	60	nC
Q_{gs}	Gate−Source Charge		–	8.2	–	nC
Q_{gd}	Gate−Drain Charge		–	21	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain−Source Diode Forward Current		–	–	48	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	144	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)	–	–	1.3	V
		T_J = 125°C	–	–	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/μs	35	75	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case		–	–	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient		–	–	62.5	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

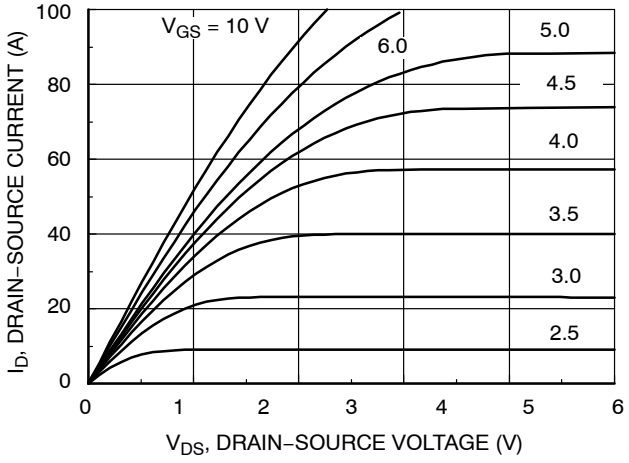


Figure 1. On−Region Characteristics

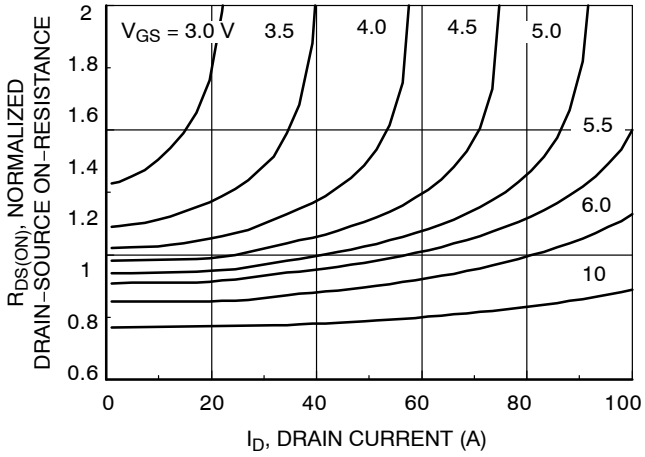


Figure 2. On−Resistance Variation with Gate Voltage and Drain Current

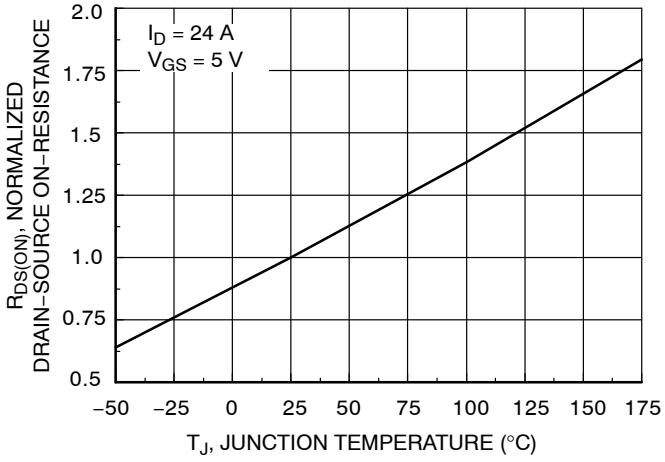


Figure 3. On−Resistance Variation with Temperature

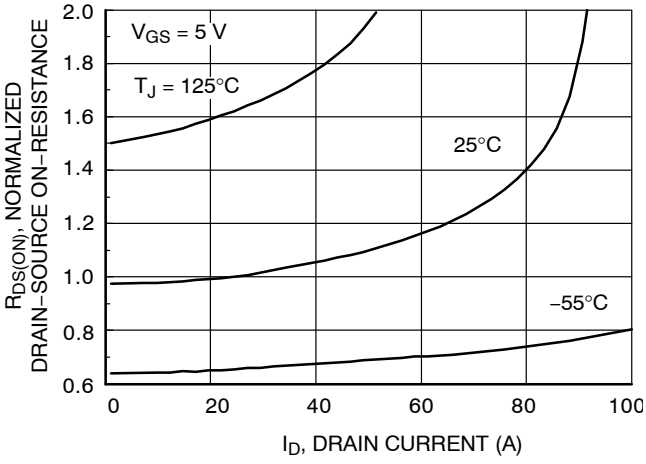


Figure 4. On−Resistance Variation with Drain Current and Temperature

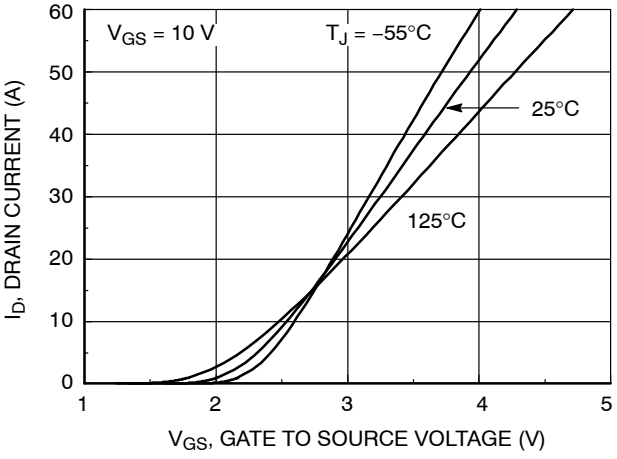


Figure 5. Transfer Characteristics

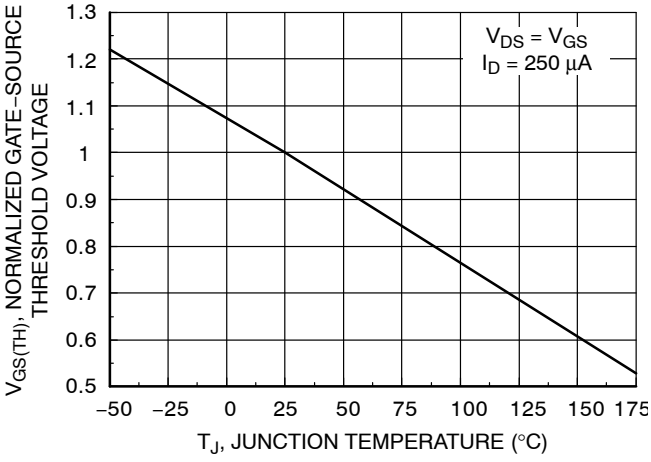


Figure 6. Gate Threshold Variation with Temperature

TYPICAL CHARACTERISTICS (continued)

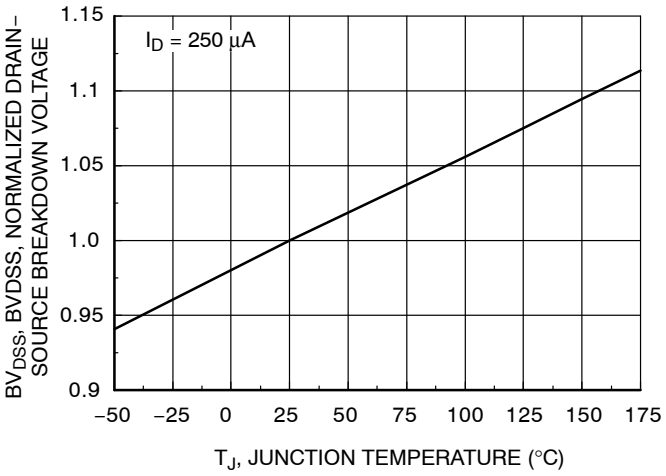


Figure 7. Breakdown Voltage Variation with Temperature

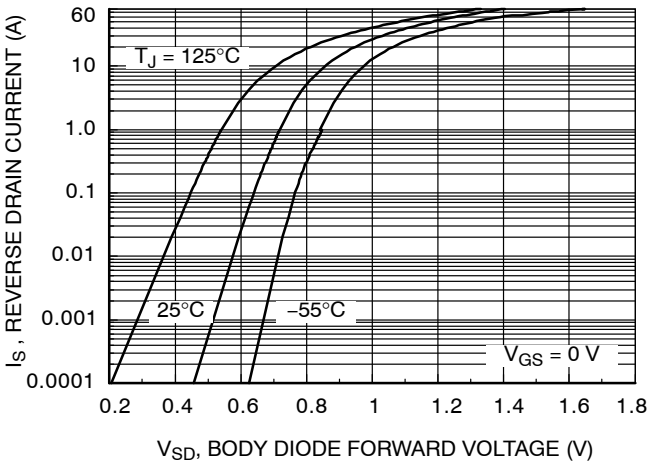


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

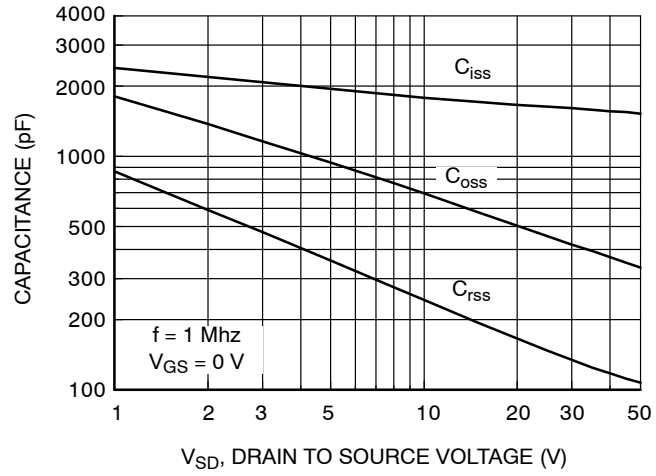


Figure 9. Capacitance Characteristics

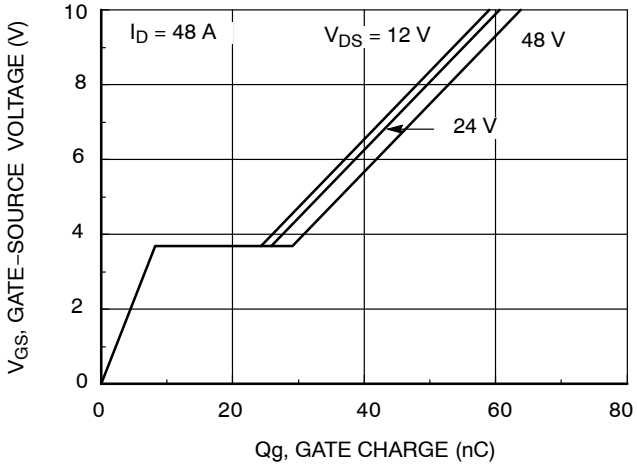


Figure 10. Gate Charge Chracteristics

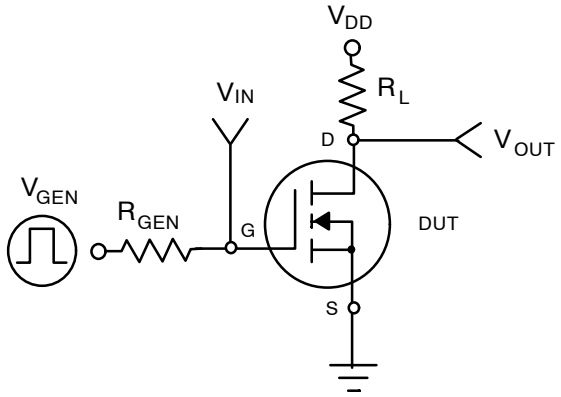


Figure 11. Switching Test Circuit

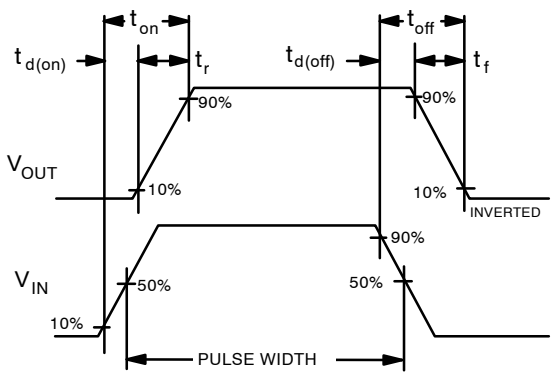


Figure 12. Switching Waveforms

TYPICAL CHARACTERISTICS

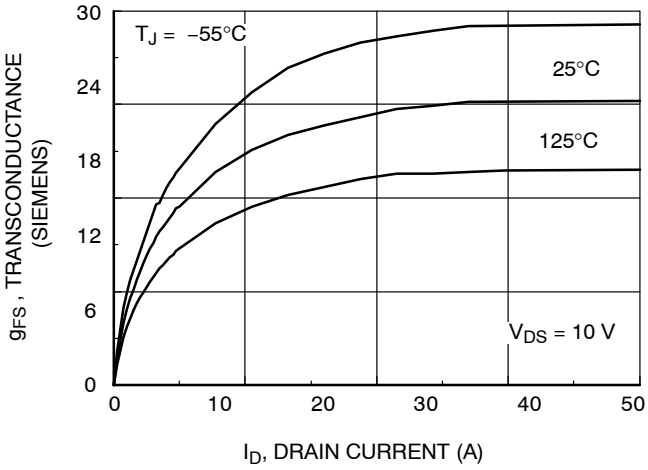


Figure 13. Transconductance Variation with Drain Current and Temperature

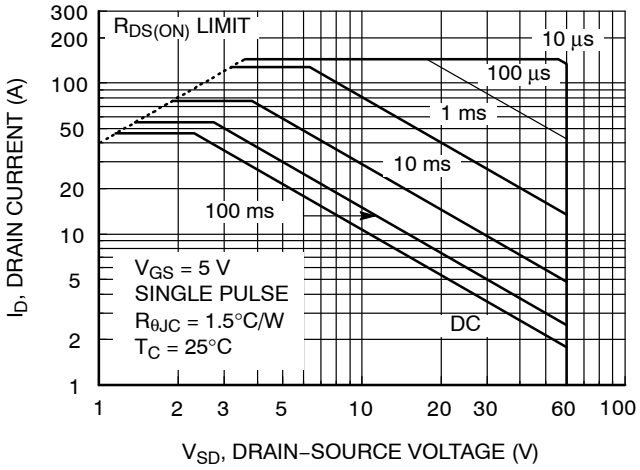


Figure 14. Maximum Safe Operating Area

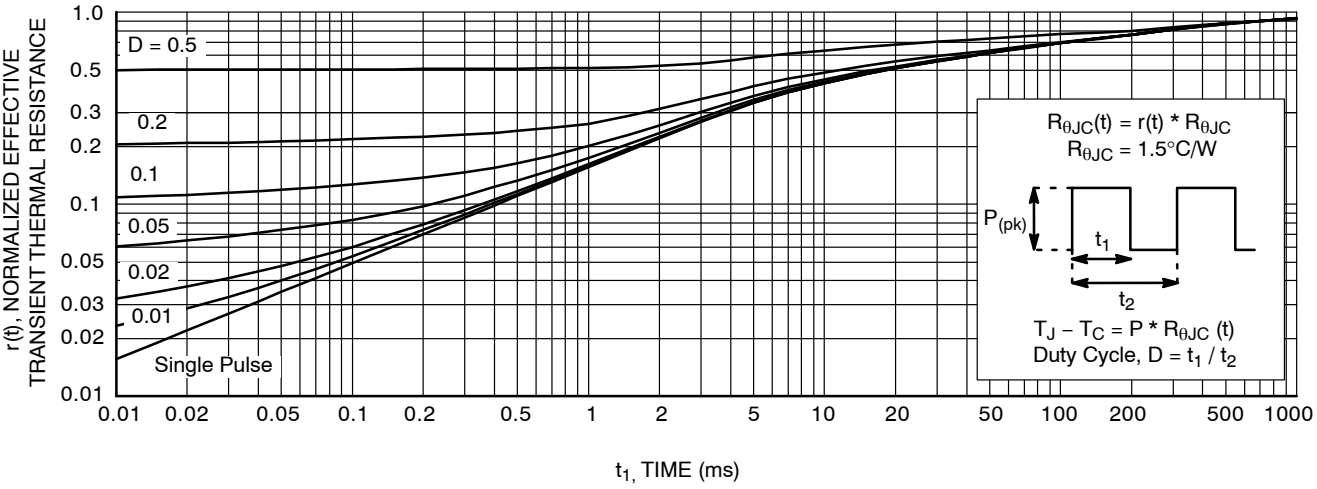


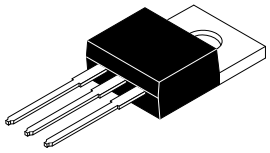
Figure 15. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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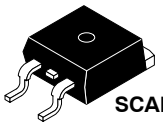
DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

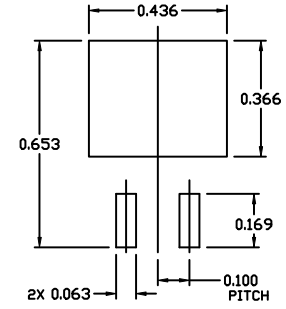
ON Semiconductor®



SCALE 1:1

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



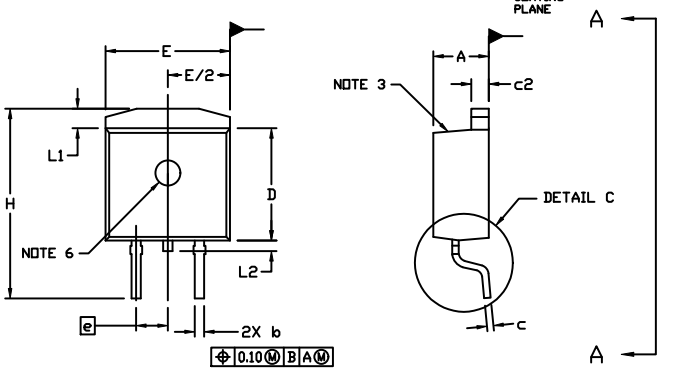
RECOMMENDED
MOUNTING FOOTPRINT

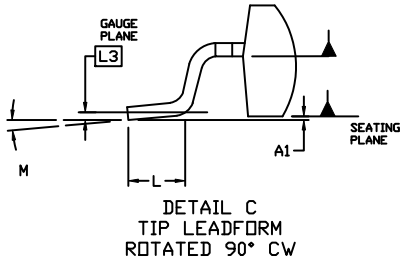
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

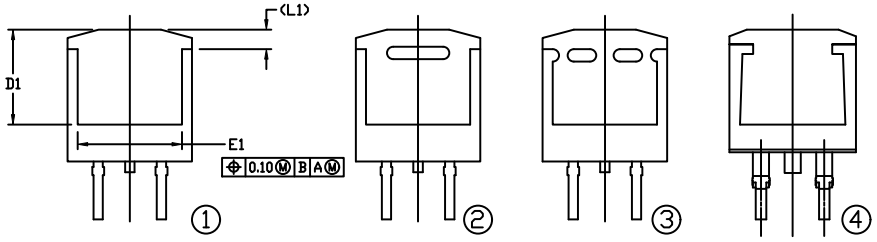
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°





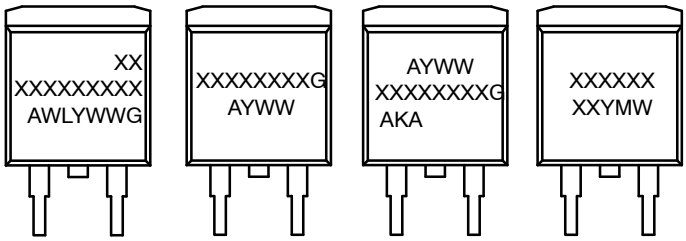
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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