NDT02N60Z

N-Channel Power MOSFET 600 V, 8.0 Ω

Features

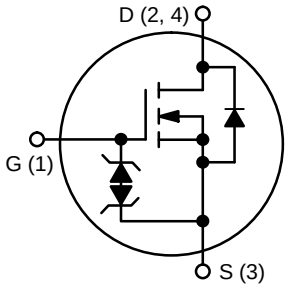
- 100% Avalanche Tested
- Extremely High dv/dt Capability
- Gate Charge Minimized
- Zener−protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX
600 V	8.0 Ω @ 10 V

N−Channel



ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	600	V
Gate−to−Source Voltage	V_{GS}	±30	V
Continuous Drain Current $R_{\theta JA}$ Steady State, T_C = 25°C	I_D	0.3	A
Continuous Drain Current $R_{\theta JA}$ Steady State, T_C = 100°C	I_D	0.21	A
Power Dissipation – $R_{\theta JA}$ Steady State, T_C = 25°C	P_D	2.0	W
Pulsed Drain Current	I_{DM}	5	A
Continuous Source Current (Body Diode)	I_S	2.2	A
Single Pulse Drain−to−Source Avalanche Energy (I_D = 1.4 A)	EAS	38	mJ
Peak Diode Recovery (Note 1)	dV/dt	4.5	V/ns
Maximum Temperature for Soldering Leads	T_L	260	°C
Operating Junction and Storage Temperature	T_J, T_{STG}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_S < 2.2 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, T_J = +150°C

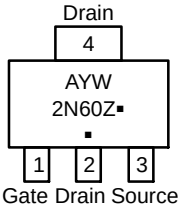
THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction−to−Ambient Steady State NDT02N60Z (Note 2) NDT02N60Z (Note 3)	$R_{\theta JA}$	 61 148	°C/W

2. Surface mounted on FR4 board using 1″ sq. pad size (Cu area = 1.127″ sq. [2 oz] including traces)
3. Surface−mounted on FR4 board using minimum recommended pad size (Cu area = 0.026” sq. [2 oz]).

MARKING DIAGRAM

SOT−223
CASE 318E
STYLE 3



A = Assembly Location
Y = Year
W = Work Week
2N60Z = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		600			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to 25°C, I_D = 1 mA			605		mV/°C
Drain−to−Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	T_J = 25°C			1	μA
			T_J = 125°C			50	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±20 V				±10	μA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 50 μA		3.0	3.9	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C, I_D = 50 μA			10.2		mV/°C
Static Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.7 A			5.9	8.0	Ω
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 0.7 A			1.3		S
DYNAMIC CHARACTERISTICS							
Input Capacitance (Note 5)	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz			170		pF
Output Capacitance (Note 5)	C_{oss}				22		
Reverse Transfer Capacitance (Note 5)	C_{rss}				4.8		
Effective output capacitance, energy related (Note 7)	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 to 480 V			7.8		
Effective output capacitance, time related (Note 8)	$C_{o(tr)}$	I_D = constant, V_{GS} = 0 V, V_{DS} = 0 to 480 V			12.4		
Total Gate Charge (Note 5)	Q_g	V_{DS} = 300 V, I_D = 1.6 A, V_{GS} = 10 V			7.4		nC
Gate-to-Source Charge (Note 5)	Q_{gs}				1.8		
Gate-to-Drain (“Miller”) Charge (Note 5)	Q_{gd}				3.8		
Plateau Voltage	V_{GP}				6.4		V
Gate Resistance	R_g				11.5		Ω
RESISTIVE SWITCHING CHARACTERISTICS (Note 6)							
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 300 V, I_D = 1.6 A, V_{GS} = 10 V, R_G = 0 Ω			10		ns
Rise Time	t_r				6		
Turn-off Delay Time	$t_{d(off)}$				14		
Fall Time	t_f				8		
SOURCE−DRAIN DIODE CHARACTERISTICS							
Diode Forward Voltage	V_{SD}	I_S = 1.6 A, V_{GS} = 0 V	T_J = 25°C		0.9	1.2	V
			T_J = 100°C		0.8		
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, V_{DD} = 30 V, I_S = 1.6 A, d_i/d_t = 100 A/μs			230		ns
Charge Time	t_a				50		
Discharge Time	t_b				180		
Reverse Recovery Charge	Q_{rr}				495		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.
5. Guaranteed by design.
6. Switching characteristics are independent of operating junction temperatures.
7. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
8. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

TYPICAL CHARACTERISTICS

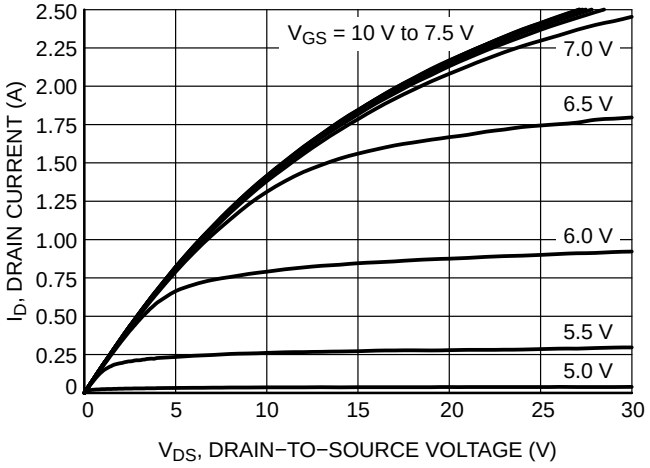


Figure 1. On−Region Characteristics

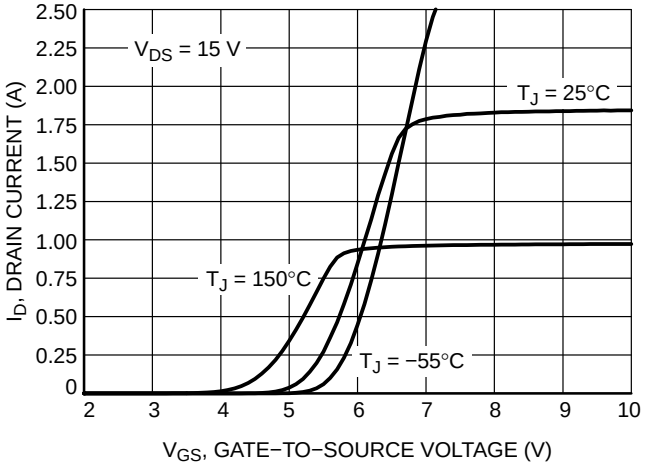


Figure 2. Transfer Characteristics

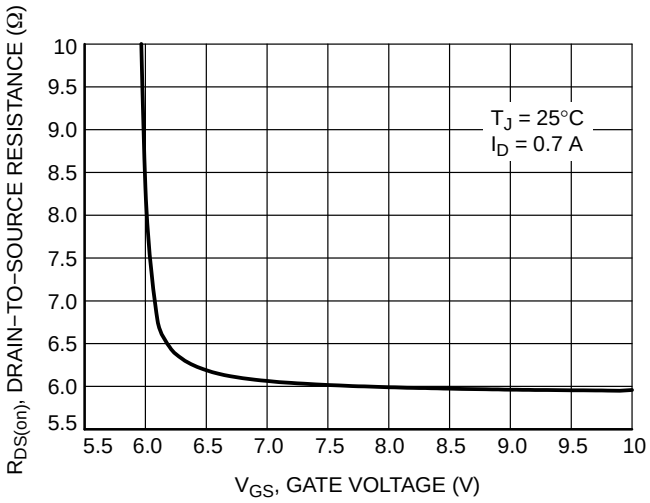


Figure 3. On−Resistance vs. Gate−to−Source Voltage

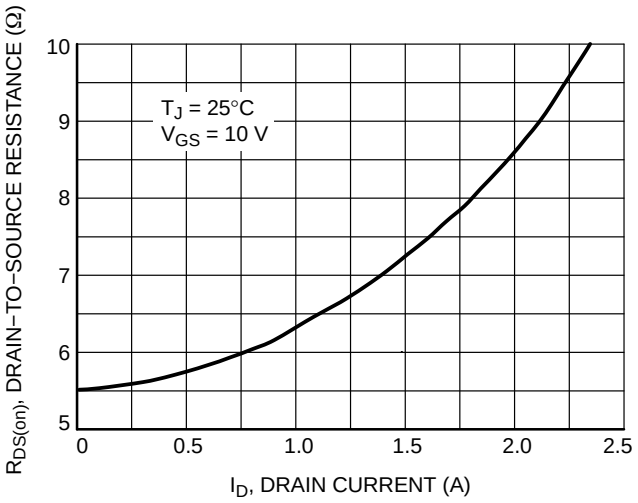


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

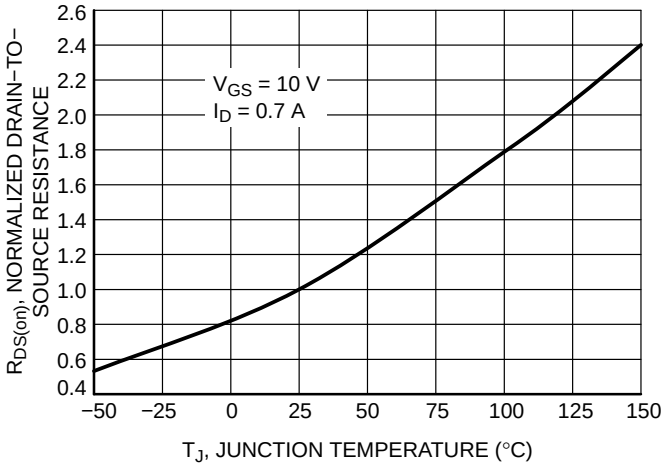


Figure 5. On−Resistance Variation with Temperature

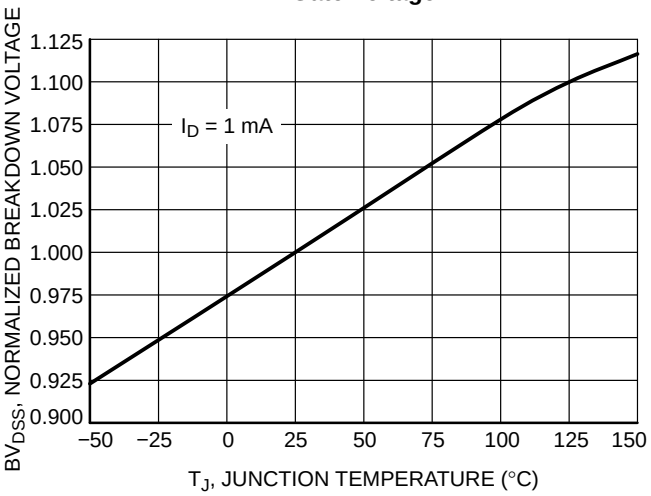


Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

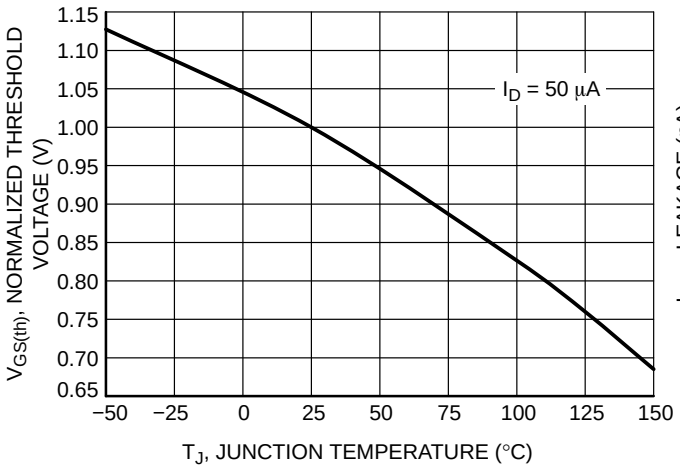


Figure 7. Threshold Voltage Variation with Temperature

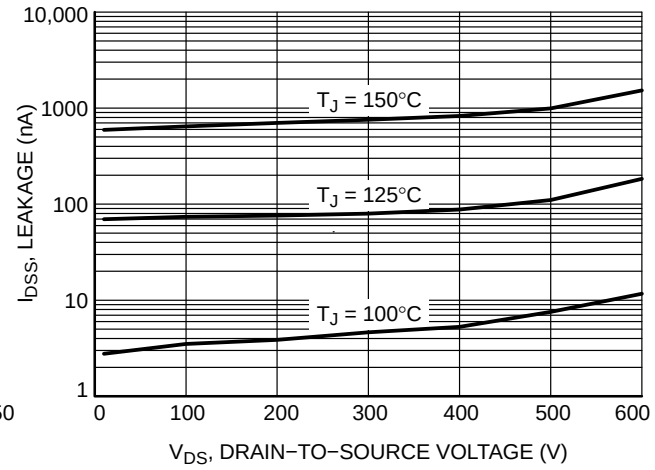


Figure 8. Drain−to−Source Leakage Current vs. Voltage

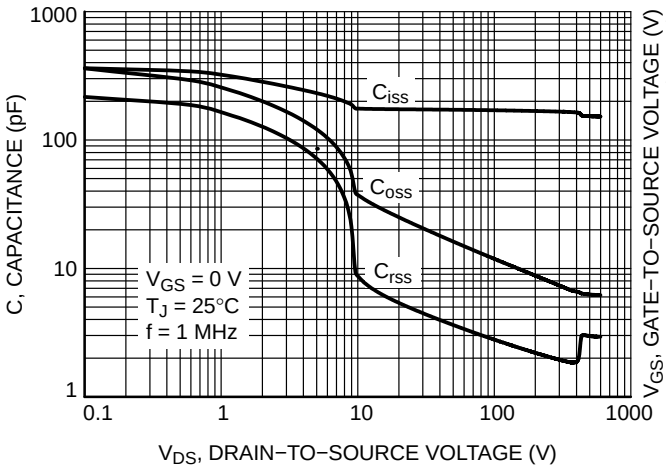


Figure 9. Capacitance Variation

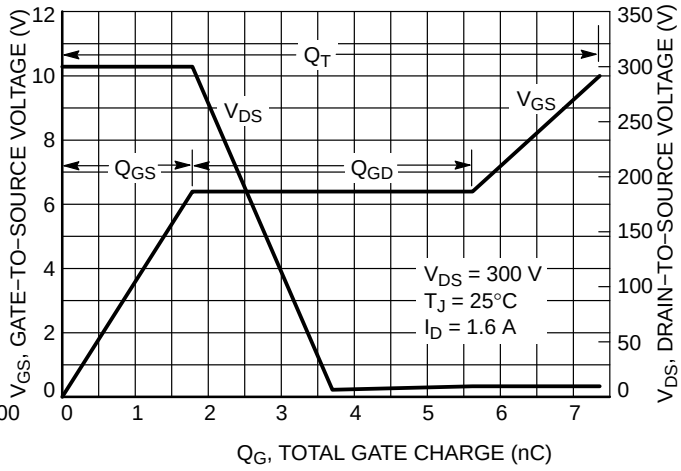


Figure 10. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

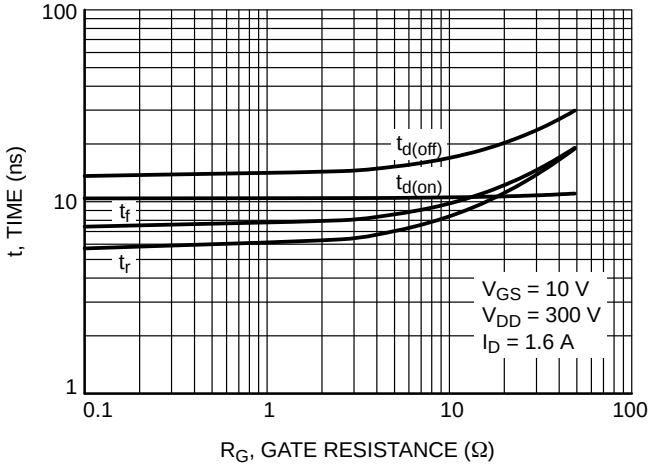


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

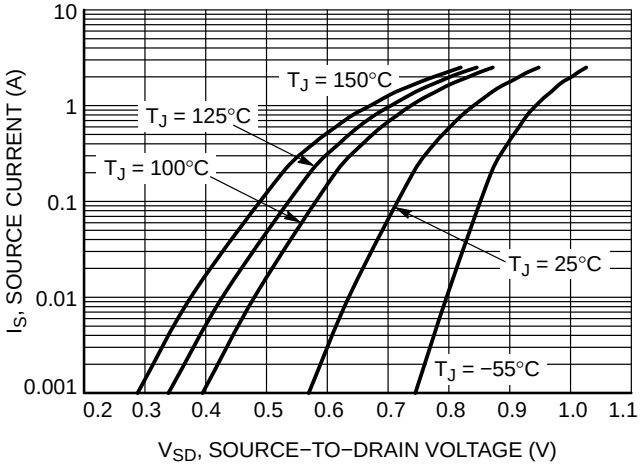


Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

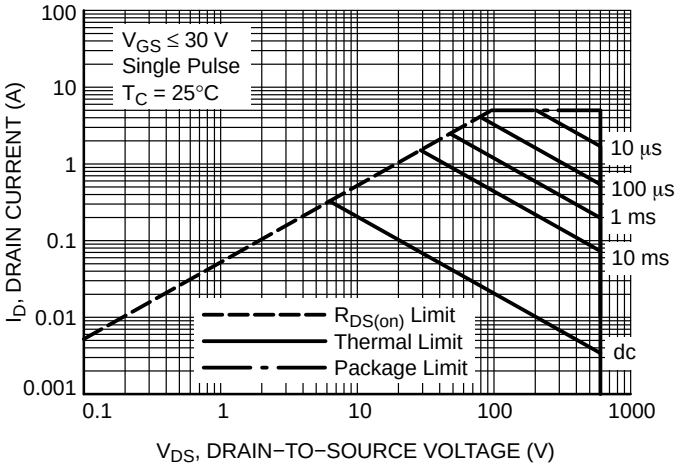


Figure 13. Maximum Rated Forward Biased Safe Operating Area

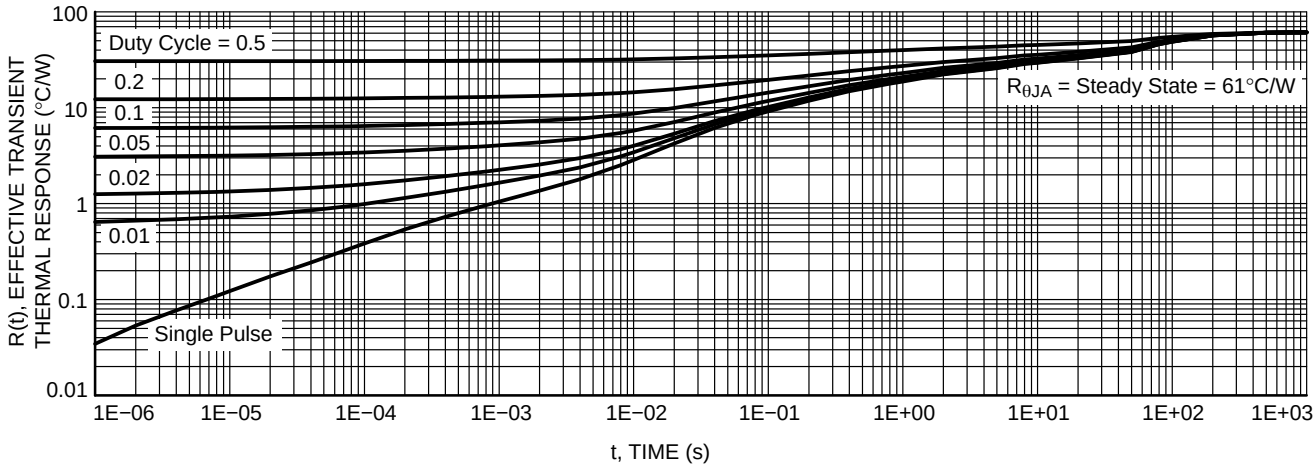


Figure 14. Thermal Impedance (Junction−to−Ambient)

ORDERING INFORMATION

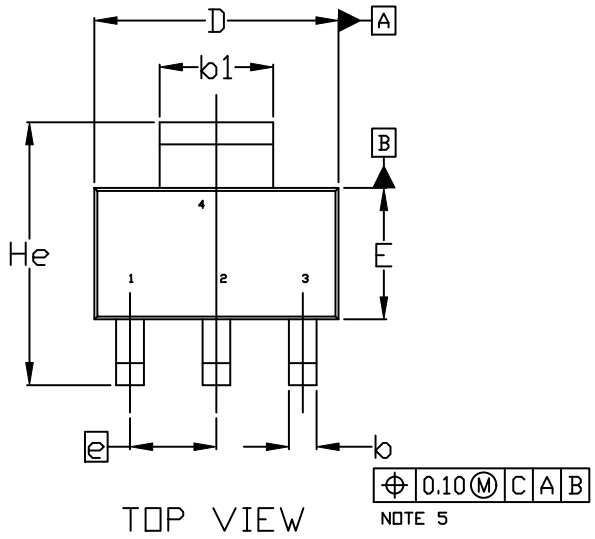
Device	Package	Shipping†
NDT02N60ZT1G	SOT−223 (Pb−Free, Halogen Free)	1000 / Tape & Reel
NDT02N60ZT3G		4000 / Tape & Reel

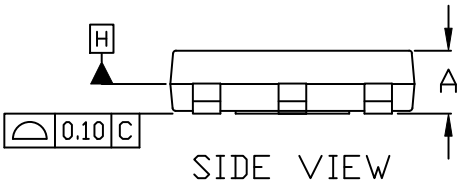
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

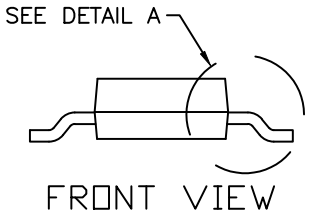
SCALE 1:1

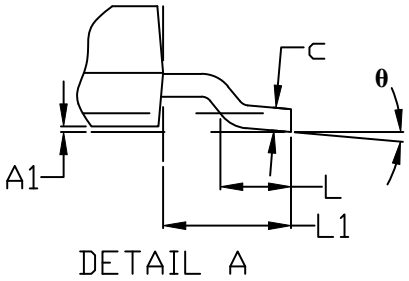
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



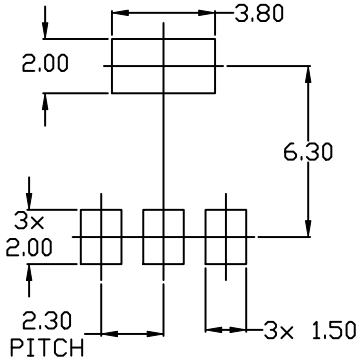






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

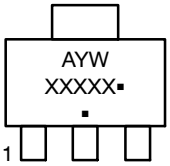
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
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