# onsemi

### **Intelligent Power Module (IPM)**

### 650 V, 30 A

## NFAM3065L4BTL

#### **General Description**

The NFAM3065L4BTL is a fully-integrated inverter power module consisting of an independent High side gate driver, LVIC, six IGBT's and a temperature sensor (VTS or Thermistor (T)), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a three-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has undervoltage lockout protection (UVP). Internal boost diodes are provided for high side gate boost drive.

#### Features

- Three-phase 650 V, 30 A IGBT Module with Independent Drivers
- Active Logic Interface
- Built-in Undervoltage Protection (UVP)
- Integrated Bootstrap Diodes and Resistors
- Separate Low-side IGBT Emitter Connections for Individual Current Sensing of Each Phase
- Temperature Sensor (VTS or Thermistor (T))
- UL1557 Certified (File No.339285)
- This Device is Pb-Free and RoHS Compliant

#### **Typical Applications**

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation



**Figure 1. Application Schematic** 



DIP39 54.5 x 31.0 CASE MODGC

#### MARKING DIAGRAM



Device marking is on package top side

ZZZ	= Assembly Lot Code
A	= Assembly Location
Т	= Test Location

= Year

= Work Week

Υ

WW

#### **ORDERING INFORMATION**

Device	Package	Shipping
NFAM3065L4BTL	DIP39 54.5 x 31.0 (Pb-Free)	90 / Box

#### **APPLICATION SCHEMATIC**



Figure 2. Application Schematic – Adjustable Option

#### **BLOCK DIAGRAM**





#### **PIN FUNCTION DESCRIPTION**

Pin	Name	Description
1	VS(U)	High-Side Bias Voltage GND for U phase IGBT Driving
(2)	-	Dummy
3	VB(U)	High-Side Bias Voltage for U phase IGBT Driving
4	VDD(UH)	High-Side Bias Voltage for U phase IC
(5)	-	Dummy
6	HIN(U)	Signal Input for High-Side U Phase
7	VS(V)	High-Side Bias Voltage GND for V phase IGBT Driving
(8)	-	Dummy
9	VB(V)	High-Side Bias Voltage for V phase IGBT Driving
10	VDD(VH)	High-Side Bias Voltage for V phase IC
(11)	-	Dummy
12	HIN(V)	Signal Input for High-Side V Phase
13	VS(W)	High-Side Bias Voltage GND for W phase IGBT Driving
(14)	-	Dummy
15	VB(W)	High-Side Bias Voltage for W phase IGBT Driving
16	VDD(WH)	High-Side Bias Voltage for W phase IC
(17)	_	Dummy
18	HIN(W)	Signal Input for High-Side W Phase
(19)	-	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low-Side U Phase
22	LIN(V)	Signal Input for Low-Side V Phase
23	LIN(W)	Signal Input for Low-Side W Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Current Protection
27	VSS	Low-Side Common Supply Ground
28	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
(29)	-	Dummy
(30)	-	Dummy
31	NW	Negative DC-Link Input for U Phase
32	NV	Negative DC-Link Input for V Phase
33	NU	Negative DC-Link Input for W Phase
34	W	Output for U Phase
35	V	Output for V Phase
36	U	Output for W Phase
37	Р	Positive DC-Link Input
38	VTH	Thermistor Bias Voltage (T) / Not connection
39	RTH	Series Resister for Thermistor (Temperature Detection) *optional for T

1. Pins of () are the dummy for internal connection. These pins should be no connection.

#### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C) (Note 2)

Symbol	Rating	Conditions	Value	Unit
VPN	Supply Voltage	P–NU, NV, NW	450	V
VPN(surge)	Supply Voltage (Surge)	P-NU, NV, NW (Note 3)	550	V
VPN(PROT)	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD = VBS = 13.5 V to 16.5 V, Tj = 150°C, VCES < 650 V, Non-Repetitive, < 2 μs	400	V
Vces	Collector-emitter Voltage		650	V
VRRM	Maximum Repetitive Revers Voltage		650	V
±lc	Each IGBT Collector Current		±30	Α
±lcp	Each IGBT Collector Current (Peak)	Under 1ms Pulse Width	±60	Α
VDD	Control Supply Voltage	VDD(UH,VH,WH), VDD(L)-VSS	–0.3 to 20	V
VBS	High-Side Control Bias voltage	VB(U)–VS(U), VB(V)–VS(V), VB(W)–VS(W)	-0.3 to 20	V
VIN	Input Signal Voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)–VSS	–0.3 to VDD	V
VFO	Fault Output Supply Voltage	VFO-VSS	-0.3 to VDD	V
IFO	Fault Output Current	Sink Current at VFO pin	2	mA
VCIN	Current Sensing Input Voltage	CIN-VSS	–0.3 to VDD	V
Pc	Corrector Dissipation	Per One Chip	113	W
Tj	Operating Junction Temperature		-40 to +150	°C
Tstg	Storage Temperature		-40 to +125	°C
Тс	Module Case Operation Temperature		-40 to +125	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V rms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 2. Refer to <u>ELECTRICAL CHARACTERISTICS</u>, <u>RECOMMENDED OPERATING RANGES</u> and/or APPLICATION INFORMATION for Safe

Operating parameters.

3. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.

#### **THERMAL CHARACTERISTICS**

Symbol	Rating	Conditions Min T		Тур	Max	Unit
R <sub>th(j-c)Q</sub>	Junction-to-Case Thermal	Inverter IGBT Part (per 1/6 module)	-	-	1.1	°C/W
R <sub>th(j-c)F</sub>	nesisiance	Inverter FWD Part (per 1/6 module)	-	-	2.2	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Rating	Conditions		Min	Тур	Max	Unit
VPN	Supply Voltage	P-NU, NV, NW		-	300	400	V
VDD	Gate Driver Supply	VDD(UH,VH,WH)	, VDD(L)-VSS	13.5	15	16.5	V
VBS	voitages	VB(U)-VS(U), VB VB(W)-VS(W)	(V)-VS(V),	13.0	15	18.5	V
dVDD / dt, dVBS / dt	Supply Voltage Variation			-1	-	1	V/µs
f <sub>PWM</sub>	PWM Frequency			1	-	20	kHz
DT	Dead Time	Turn-off to Turn-on (external)		1.5	-	-	μs
lo	lo Allowable r.m.s. Current VPN = 300 V, VDD = 15 V, P.F. = 0.8		f <sub>PWM</sub> = 5 kHz	-	-	21.2	A rms
		Tc ≤ 125°C, Tj ≤ 150°C (Note 5)	f <sub>PWM</sub> = 15 kHz	-	-	17.2	
PWIN (on)	Allowable Input Pulse Width	$\begin{array}{c} 200 \text{ V} \leq \text{VPN} \leq 40\\ 13.5 \text{ V} \leq \text{VDD} \leq 10 \end{array}$	0 V 6.5 V	1.0	-	-	μs
PWIN (off)		$13.0 \text{ V} \le \text{VBS} \le 18$ $-20^{\circ}\text{C} \le \text{Tc} \le 100^{\circ}$	3.5 V °C	1.5	_	_	
	Package Mounting Torque	M3 type screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability. 5. Allowable r.m.s current depends on the actual conditions.

6. Flatness tolerance of the heatsink should be within  $-50 \ \mu m$  to  $+100 \ \mu m$ .

#### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C, VDD = 15 V, VBS = 15 V, unless otherwise specified.) (Note 7)

Symbol	Parameter		Test Conditions	Min	Тур	Мах	Unit
INVERTER SE	CTION						
lces	Ices Collector-Emitter Leakage Current		Vce = Vces, Tj = 25°C	-	-	1	mA
			Vce = Vces, Tj = 150°C	-	-	10	mA
VCE(sat)	Collector-Emitter Sa Voltage	aturation	VDD = VBS = 15 V, IN = 5 V Ic = 30 A, Tj = 25°C	-	1.60	2.30	V
	FWDi Forward Voltage		VDD = VBS = 15 V, IN = 5 V Ic = 30 A, Tj = 150°C	-	1.80	-	V
VF			IN = 0 V, Ic = 30 A, Tj = 25°C	-	2.00	2.40	V
			IN = 0 V, Ic = 30 A, Tj = 150°C	-	2.00	-	V
ton	Switching Times	High Side	h Side VPN = 300 V, VDD(H) = VDD(L) = 15 V Ic = 30 A, Tj = 25°C, IN = 0 $\Leftrightarrow$ 5 V Inductive Load	1.00	1.60	2.20	μs
tc(on)		riigh olde		-	0.50	1.00	μs
toff				-	1.60	2.20	μs
tc(off)				-	0.25	0.75	μs
trr				-	0.15	-	μs
ton		Low Side	VPN = 300 V, VDD(H) = VDD(L) = 15 V	1.10	1.70	2.30	μs
tc(on)			Inductive Load $(1) = 25^{\circ}$ ( $10 = 0 \Leftrightarrow 5^{\circ}$ ( $10 = 0 \Leftrightarrow 5^{\circ}$	-	0.50	1.00	μs
toff				-	1.60	2.20	μs
tc(off)				_	0.25	0.75	μs
trr				-	0.15	-	μs

<b>ELECTRICAL CHARACTERISTICS</b>	(T	= 25°C, VDD = 15 V, VBS = 15 V, unless otherwise	specified	) (Note :	7)	(continued)
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Symbol	Parameter	Test Conditions		Min	Тур	Max	Unit
DRIVER SECTION	ON						
IQDDH	Quiescent VDD Supply Current	VDD(UH,VH,WH) = 15 V, HIN(U,V,W) = 0 V	VDD(UH)-VSS VDD(VH)-VSS VDD(WH)-VSS	-	-	0.30	mA
IQDDL		VDD(L) = 15 V, LIN(U,V,W) = 0 V	VDD(L)-VSS	-	-	3.50	mA
IPDDH	Operating VCC Supply Current	VDD(UH,VH,WH) = 15 V, f <sub>PWM</sub> = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High-Side	VDD(UH)-VSS VDD(VH)-VSS VDD(WH)-VSS	_	_	0.40	mA
IPDDL		VDD(L) = 15 V, f <sub>PWM</sub> = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for Low-Side	VDD(L)-VSS	-	_	6.00	mA
IQBS	Quiescent VBS Supply Current	VBS = 15 V, HIN(U,V,W) = 0 V	VB(U)-VS(U) VB(V)-VS(V) VB(W)-VS(W)	_	-	0.30	mA
IPBS	Operating VBS Supply Current	$\begin{array}{l} VDD = VBS = 15 \text{ V}, \\ f_{PWM} = 20 \text{ kHz}, \text{ Duty} = \\ 50\%, \text{ Applied to one PWM} \\ \text{Signal Input for High-Side} \end{array}$	VB(U)-VS(U) VB(V)-VS(V) VB(W)-VS(W)	-	_	5.00	mA
VIN(ON)	ON Threshold Voltage	HIN(U,V,W)-VSS, LIN(U,V,V	V)-VSS	-	-	2.6	V
VIN(OFF)	OFF Threshold Voltage			0.8	-	-	V
VCS(ref)	Short Circuit Trip Level	VDD = 15 V, CIN-VSS		0.46	0.48	0.50	V
UVDDD	Supply Circuit	Detection Level		10.3	-	12.5	V
UVDDR	Onder-voltage Flotection	Reset Level		10.8	I	13.0	V
UVBSD		Detection Level		10.0	I	12.0	V
UVBSR		Reset Level	Reset Level		I	12.5	V
VTS	Voltage Output for LVIC Temperature Sensing Unit	VTS-VSS = 10 nF, Temp. = 25°C		0.905	1.030	1.155	V
VFOH	Fault Output Voltage	VDD = 0 V, CIN = 0 V, VFO Circuit: 10 k $\Omega$ to 5 V Pull-up		4.9	-	-	V
VFOL		VDD = 0 V, CIN = 1 V, VFO Circuit: $10 \text{ k}\Omega$ to 5 V Pu	ıll-up	-	-	0.95	V
t <sub>FOD</sub>	Fault-Output Pulse Width	CFOD = 22 nF		1.6	2.4	-	ms

**BOOTSTRAP SECTION** 

VF	Bootstrap Diode Forward Voltage	lf = 0.1 A	3.4	4.6	5.8	V
RBOOT	Built-in Limiting Resistance		30	38	46	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^{\circ}$ C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. The fault-out pulse width  $t_{FOD}$  depends on the capacitance value of CFOD according to the following approximate equation:  $t_{FOD} = 0.11 \times 10^6 \times CFOD$  (s). 9. Values based on design and/or characterization.

#### Temperature of LVIC versus VTS Characteristics



Figure 4. Temperature of LVIC versus VTS Characteristics

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Resistance	R <sub>25</sub>	Tc = 25°C	46.530	47	47.47	kΩ
Resistance	R <sub>125</sub>	$Tc = 100^{\circ}C$	1.344	1.406	1.471	kΩ
B-Constant (25–50°C)	-	В	4009.5	4050	4090.5	К
Temperature range	-	-	-40	-	+125	°C

Table 1. THERMISTOR CHARACTERISTICS (INCLUDED ONLY IN NFAM3060L4BT)



Figure 5. Thermistor Resistance versus Case Temperature



#### DIP39, 54.50x31.00x5.60, 1.78P CASE MODGC ISSUE C DATE 05 MAY 2025 NOTES MILLIMETERS MILLIMETERS DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009. CONTROLLING DIMENSION: MILLIMETERS DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE 1. 2. 3. MIN. NOM. MAX. MIN. NOM. MAX. DIM DIM 12.20 12.7 13.2 30.90 31.00 31.10 А Е 33.50 REF MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP A1 1.00 1.50 2.00 E1 POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY 4. 5.60 26.14 REF 5.70 A2 5.50 E2 12.35 REF A3 2.00 RE E3 AREA FOR 2D BAR CODE SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29 AND 30 A4 1.55 REF E4 8.00 REF 6. 7. 35.40 35.90 36.40 DIMENSIONS "D" AND "E" DO NOT INCLUDE THE SIDE FLASH PROTRUSION WHICH IS ~0.12 FOR EACH SIDE A5 3.10 REF E5 0.90 1.00 1.10 2.81 REF b е 1.90 2.10 2.00 7.62 BSC b1 e1 0.60 0.50 6.60 BSC (e6) b2 0.40 e2 DETAIL C 1.40 1.50 1.60 3.30 BSC b3 e3 (e4) 0.50 RE 5.35 REF с e4 54.50 54.60 D e5 6.10 BSC 54.40 A2 39.25 REF 8.02 REF D3 e6 7x (L1) D4 8.00 REF e7 1.78 BSC C SEATING D5 22.00 REF 10.35 REF e8 D6 24.00 REF 10.25 REF e9 e7 e5 (L) 21.85 REF 3.60 REF D7 e10 9x e7 23.85 REF 1.00 REF D8 e11 0.89 BSC SIDE VIEW e12 DETAIL D 3.30 3.40 F 3.20 DETAIL D 1.40 1.50 1.60 F1 DETAIL A (D5) (D6) (D3) L 5.60 REF (c) 0.10 REF L1 ለለጽ Þ $\cap$ 2x ØF В (E1) (E2) $\cap$ е E5 (D4) (E3) Ð 0 2x ØF1 e8 (e11) -(e10) -Retractable $\bigcirc$ (F4 Pin NOTE 5 5656 ដូដ បស់ជ 'n ч ն £ 5 'n 31 3 (e9) EXPOSED CU AREA END VIEW BOTTOM VIEW (D8) (D7 TOP VIEW e2 (e) e12 ---e3 A1 30x h2 F 2x b3 (A3 C SEATING (A4) DETAIL B (A5) DETAIL C 2x e3 e1 DETAIL A DETAIL B 4x e' SIDE VIEW GENERIC **MARKING DIAGRAM\*** ZZZATYWW 2D CODE XXXXX = Specific Device Code = Assembly Lot Code 777 \*This information is generic. Please refer to device data AT = Assembly & Test Location sheet for actual part marking. Pb-Free indicator, "G" or = Year microdot "•", may or may not be present. Some products ww = Work Week may not follow the Generic Marking. Electronic versions are uncontrolled except when accessed directly from the Document Repository. **DOCUMENT NUMBER:** 98AON91300G Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. **DESCRIPTION:** DIP39, 54.50x31.00x5.60, 1.78P PAGE 1 OF 1

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