# NL17SH34

## Single Buffer

The NL17SH34 MiniGate™ is an advanced high−speed CMOS Buffer in ultra−small footprint.

The NL17SH34 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

### Features

- High Speed: $t_{PD}$ = 3.5 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 1.0 μA (Max) at $T_A$ = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra−Small Package
- These are Pb−Free and Halide−Free Devices

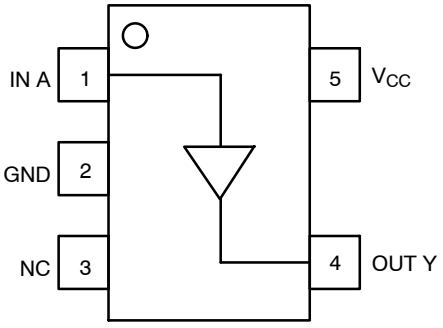


**Figure 1. Pinout** (Top View)

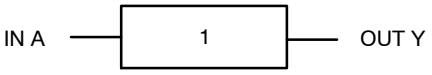


**Figure 2. Logic Symbol**

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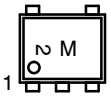
**MARKING DIAGRAM**

**SOT−953**
**CASE 527AE**




2 = Specific Device Code (Rotated 90°)
M = Month Code

| PIN ASSIGNMENT | |
|---|---|
| 1 | IN A |
| 2 | GND |
| 3 | NC |
| 4 | OUT Y |
| 5 | $V_{CC}$ |

**FUNCTION TABLE**

| A Input | Y Output |
|---|---|
| L | L |
| H | H |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | $V_{IN}$ = 0<br>High or Low State | −0.5 to +7.0<br>−0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | DC Input Diode Current | $V_{IN}$ < GND | −20 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_{OUT}$ < GND, $V_{OUT}$ > $V_{CC}$ | ±20 | mA |
| $I_{OUT}$ | DC Output Source/Sink Current | | ±25 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | 50 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4) | >2000<br>>200<br>N/A | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 5) | ±100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | 1.65 | 5.5 | V |
| $V_{IN}$ | Digital Input Voltage | | 0.0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage | | 0.0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $\Delta t / \Delta V$ | Input Transition Rise or Fail Rate | $V_{CC}$ = 3.3 V ± 0.3 V<br>$V_{CC}$ = 5.0 V ± 0.5 V | 0<br>0 | 100<br>20 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \leq$ 85°C Min | $T_A \leq$ 85°C Max | −55°C to 125°C Min | −55°C to 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High−Level Input Voltage | | 1.65 to 2.0 | 0.75 x $V_{CC}$ | | | 0.75 x $V_{CC}$ | | | | V |
| | | | 2.3 to 5.5 | 0.70 x $V_{CC}$ | | | 0.70 x $V_{CC}$ | | | | |
| $V_{IL}$ | Low−Level Input Voltage | | 1.65 to 2.0 | | | 0.25 x $V_{CC}$ | | 0.25 x $V_{CC}$ | | 0.25 x $V_{CC}$ | V |
| | | | 2.3 to 5.5 | | | 0.30 x $V_{CC}$ | | 0.30 x $V_{CC}$ | | 0.30 x $V_{CC}$ | |
| $V_{OH}$ | High−Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50\ \mu A$ | 2.0<br>3.0<br>4.5 | 1.9<br>2.9<br>4.4 | 2.0<br>3.0<br>4.5 | | 1.9<br>2.9<br>4.4 | | 1.9<br>2.9<br>4.4 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4$ mA $I_{OH} = -8$ mA | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | 2.34<br>3.66 | | |
| $V_{OL}$ | Low−Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50\ \mu A$ | 2.0<br>3.0<br>4.5 | | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 4$ mA $I_{OL} = 8$ mA | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | | 0.52<br>0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.0 | | 10 | | 40 | μA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns)

| Symbol | Parameter | $V_{CC}$ (V) | Test Conditions | $T_A$ = 25°C Min | $T_A$ = 25°C Typ | $T_A$ = 25°C Max | $T_A \leq$ 85°C Min | $T_A \leq$ 85°C Max | −55°C to 125°C Min | −55°C to 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, A to Y | 3.0 to 3.6 | $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 4.5<br>6.4 | 7.1<br>10.6 | | 8.5<br>12.0 | | 10.0<br>14.5 | ns |
| | | 4.5 to 5.5 | $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 3.5<br>4.5 | 5.5<br>7.5 | | 6.5<br>8.5 | | 8.0<br>10.0 | |
| $C_{IN}$ | Input Capacitance | | | | 4.0 | 10 | | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | 5.0 | | | 8.0 | | | | | | pF |

6. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

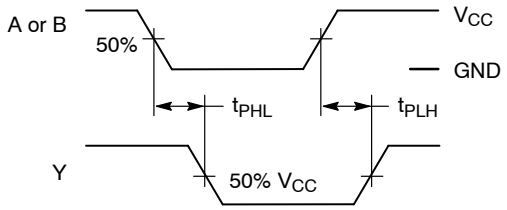
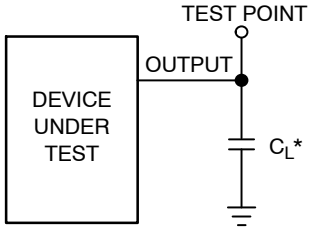



**Figure 3. Switching Waveforms**




*Includes all probe and jig capacitance.

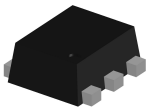
**Figure 4. Test Circuit**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NL17SH34P5T5G | SOT−953<br>(Pb−Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

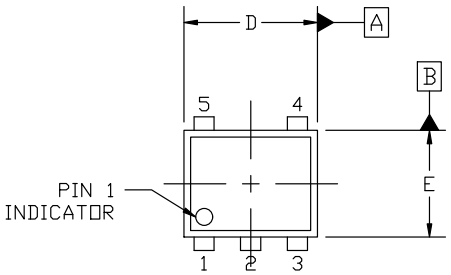


**SOT−953 1.00x0.80x0.37, 0.35P**
CASE 527AE
ISSUE F

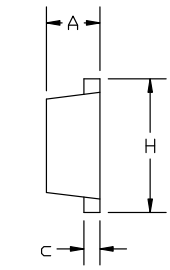
DATE 17 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

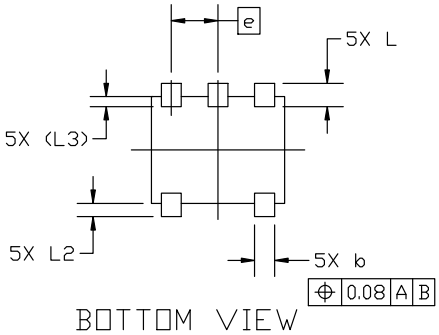
| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| C | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.125 | 0.175 | 0.225 |
| L2 | 0.05 | 0.10 | 0.15 |
| L3 | 0.075 (REF) | | |



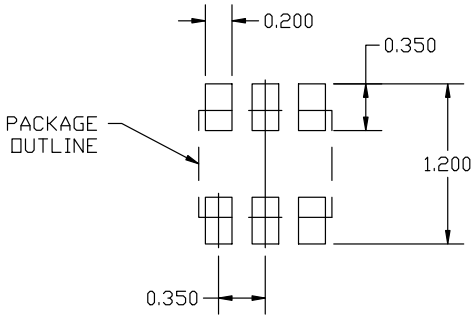

TOP VIEW




SIDE VIEW



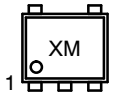

BOTTOM VIEW




RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
| DESCRIPTION: | SOT−953 1.00x0.80x0.37, 0.35P | PAGE 1 OF 1 |

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