1-Bit Dual-Supply Level Translator

NL3V1T244, NL3V1T240, NL3V1T34

The NL3V1T244 / NL3V1T240 / NL3V1T34 are 1-bit configurable dual−supply level translators with 3-state outputs. The A− and B− ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 3.6 V allowing universal voltage level translation between the A− to B− ports.

The NL3V1T244 / NL3V1T34 are 1-bit level translators that allows non-inverting translations from A to B ports. The NL3V4T240 is a 1-bit level translator that allows inverting translations from A to B ports.

The output enable pin ($\overline{OE}$), when High, disables all the output ports by putting them in 3-state. The $\overline{OE}$ pin is designed to track V_{CCA}. The NL3V1T34 does not have an $\overline{OE}$ pin.

Features

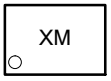
- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 3.6 V
- Balanced Output Drive: ±24 mA @ 3.0 V
- High-Speed w/ Balanced Propagation Delay: 2.8 ns max at 3.0 to 3.6 V
- Inputs Pins OVT to 3.6 V
- Non-preferential V_{CC} Sequencing
- Outputs at 3-State until Active V_{CC} is Reached
- Partial Power-Off Protection
- Outputs Switch to 3-State with either V_{CC} at GND
- Typical Max Data Rates:
  - 380 Mbps (≥1.8−V to 3.3−V Translation)
  - 200 Mbps (≥1.1−V to [1.8−V, 2.5−V, 3.3−V] Translation)
  - 150 Mbps (≥1.1−V to 1.5−V Translation)
  - 100 Mbps (≥1.1−V to 1.2−V Translation)
- Small Pb-Free Packaging: SC-88A, UDFN6
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices
- Automotive
- Industrial

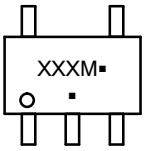
MARKING DIAGRAMS

UDFN6
MU SUFFIX
CASE 517AA



UDFN6
MU SUFFIX
CASE 517AQ

SC−88A
(SOT−353/SC−70)
DF SUFFIX
CASE 419A



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

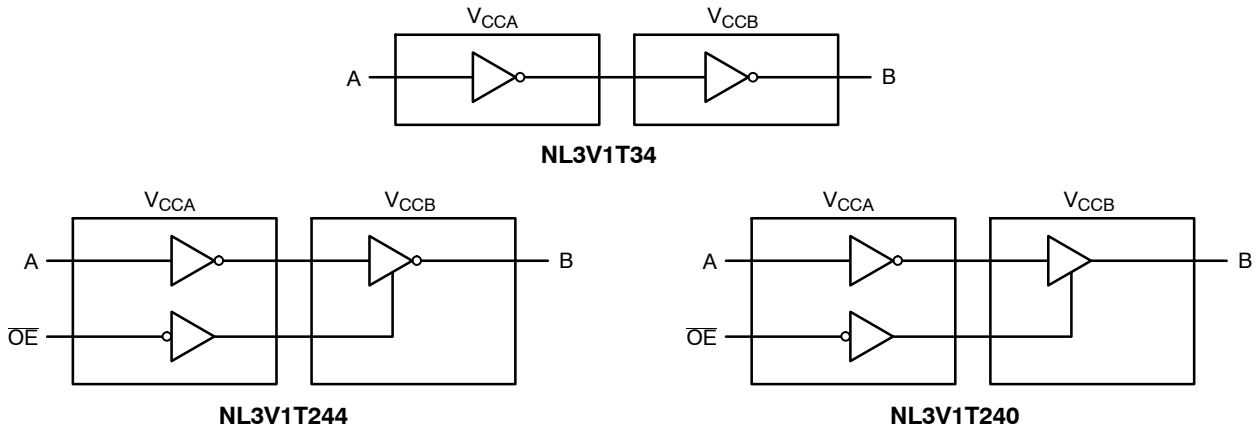


Figure 1. Logic Diagrams

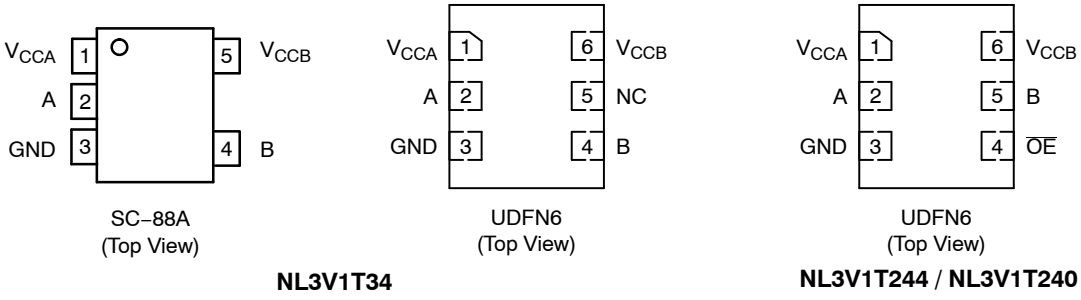


Figure 2. Pin Assignments (Top View)

FUNCTION TABLE

INPUTS		OUTPUT		
		NL3V1T34	NL3V1T244	NL3V1T240
$\overline{OE}$	A	B	B	B
L	L	L	L	H
L	H	H	H	L
H	X	n/a	3−State	3−State

PIN NAMES

PINS	DESCRIPTION
V_{CCA}	A Port DC Supply
V_{CCB}	B Port DC Supply
GND	Ground
A	Input Port
B	Output Port
$\overline{OE}$	Output Enable (Not available for NL3V1T34)

Application Recommendations

During power-up and power-down, it is recommended that the $\overline{OE}$ pin be connected to V_{CC} through pull-up resistors to ensure high impedance at the I/O ports.

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +4.3		V
V_I	DC Input Voltage		−0.5 to +4.3		V
V_O	DC Output Voltage	(Power Down Mode)	−0.5 to +4.3	V_{CCA} = V_{CCB} = 0	V
		(3-State Mode)	−0.5 to +4.3		
		(Active Mode)	−0.5 to V_{CCB}+0.5		
I_{IK}	DC Input Diode Current		−50	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature Range		−65 to +150		°C
θ_{JA}	Thermal Resistance (Note 1)	SC-88A UDFN6		377 154	°C/W
P_D	Power Dissipation in Still Air	SC-88A UDFN6		332 812	mW
MSL	Moisture Sensitivity Level			Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model		2 1	kV
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 25°C (Note 3)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	3.6	V
V_I	Input Voltage		GND	3.6	V
V_{IO}	Output Voltage	(Power Down Mode)	GND	3.6	V
		(3-State Mode)	GND	3.6	
		(Active Mode)	GND	V_{CCB}	
T_A	Operating Temperature Range		−40	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate		0	5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS – INPUT VOLTAGES

Symbol	Parameter	Test Conditions	Port	V_{CCA} (V)	V_{CCB} (V)	–40 °C to +85 °C			–40 °C to +125 °C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
V_{IH}	Input HIGH Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	2.0	–	–	2.0	–	V
				2.3 – 2.7		1.6	–	–	1.6	–	
				1.65–1.95		0.65 V_{CCA}	–	–	0.65 V_{CCA}	–	
				1.1 – 1.6		0.7 V_{CCA}	–	–	0.7 V_{CCA}	–	
				0.9		–	0.9 V_{CCA}	–	–	–	
V_{IL}	Input LOW Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	–	–	0.8	–	0.8	V
				2.3 – 2.7		–	–	0.7	–	0.7	
				1.65–1.95		–	–	0.35 V_{CCA}	–	0.35 V_{CCA}	
				1.1 – 1.6		–	–	0.3 V_{CCA}	–	0.3 V_{CCA}	
				0.9		–	0.1 V_{CCA}	–	–	–	

4. All typical values are at T_A = 25°C.

DC ELECTRICAL CHARACTERISTICS – OUTPUT VOLTAGES

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	–40 °C to +85 °C			–40 °C to +125 °C		Unit
					Min	Typ (Note 4)	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_I = V_{IH} or V_{IL}:								V
		I_{OH} = –100 μA	0.9	0.9	–	V_{CCB} – 0.1	–	–	–	
			1.1 – 3.6	1.1 – 3.6	V_{CCB} – 0.1	–	–	V_{CCB} – 0.1	–	
		I_{OH} = –2 mA	1.1	1.1	0.85	–	–	0.85	–	
		I_{OH} = –6 mA	1.4	1.4	1.05	–	–	1.05	–	
		I_{OH} = –8 mA	1.65	1.65	1.2	–	–	1.2	–	
		I_{OH} = –12 mA	2.3	2.3	1.8	–	–	1.8	–	
			2.7	2.7	2.2	–	–	2.2	–	
		I_{OH} = –18 mA	2.3	2.3	1.7	–	–	1.7	–	
			3.0	3.0	2.4	–	–	2.4	–	
		I_{OH} = –24 mA	3.0	3.0	2.2	–	–	2.2	–	
V_{OL}	Output LOW Voltage	V_I = V_{IH} or V_{IL}:								V
		I_{OL} = 100 μA	0.9	0.9	–	0.1	–	–	–	
			1.1 – 3.6	1.1 – 3.6	–	–	0.1	–	0.1	
		I_{OL} = 2 mA	1.1	1.1	–	–	0.25	–	0.25	
		I_{OL} = 6 mA	1.4	1.4	–	–	0.35	–	0.35	
		I_{OL} = 8 mA	1.65	1.65	–	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.3	2.3	–	–	0.4	–	0.4	
			2.7	2.7	–	–	0.4	–	0.4	
		I_{OL} = 18 mA	2.3	2.3	–	–	0.4	–	0.4	
			3.0	3.0	–	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	3.0	–	–	0.55	–	0.55	

DC ELECTRICAL CHARACTERISTICS – LEAKAGE AND SUPPLY CURRENTS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	–40 °C to +85 °C		–40 °C to +125 °C		Unit
					Min	Max	Min	Max	
I_I	Input Leakage Current	V_I = 3.6 V or GND	0.9 – 3.6	0.9 – 3.6	–	±1.0	–	±5.0	μA
I_{OZ}	3–State Output Leakage	$\overline{OE}$ = V_{IH} ; V_O = GND to 3.6 V	3.6	3.6	–	±1.0	–	±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_I or V_O = 0 to 3.6 V A	0	0.9 – 3.6	–	±1.0	–	±5.0	μA
		B	0.9 – 3.6	0	–	±1.0	–	±5.0	
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	5.0	–	10	μA
			0	0.9 – 3.6	–	–1.0	–	–5.0	
			0.9 – 3.6	0	–	5.0	–	10	
I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	5.0	–	10	μA
			0	0.9 – 3.6	–	5.0	–	10	
			0.9 – 3.6	0	–	–1.0	–	–5.0	

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power-up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS (Notes 5 and 6)

Symbol	Parameter	V_{CCA} (V)	T_A = –40 °C to +85 °C					T_A = –40 °C to +125 °C					Unit
			V_{CCB} (V)					V_{CCB} (V)					
			3.3	2.5	1.8	1.5	1.2	3.3	2.5	1.8	1.5	1.2	
			Max	Max	Max	Max	Max	Max	Max	Max	Max	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to B	3.3	2.9	3.3	4.5	5.6	9.3	3.3	3.8	5.0	6.2	9.5	nS
		2.5	3.6	3.7	4.6	5.7	9.4	4.0	4.0	5.1	6.3	9.6	
		1.8	3.9	4.0	4.9	6.0	9.6	4.3	4.3	5.4	6.6	9.8	
		1.5	4.2	4.3	5.2	6.3	9.8	4.7	4.7	5.8	7.0	10.0	
		1.2	5.1	5.2	6.2	7.1	11.0	5.7	5.8	6.9	7.9	11.2	
t_{PZH}, t_{PZL}	Output Enable, $\overline{OE}$ to B	3.3	3.8	4.7	6.8	8.7	11.3	4.2	5.2	7.5	9.6	12.4	nS
		2.5	4.0	4.8	7.0	8.8	11.3	4.4	5.3	7.7	9.7	12.4	
		1.8	4.6	5.3	7.4	9.2	11.7	5.1	5.9	8.2	10.2	12.9	
		1.5	5.6	5.8	7.7	9.6	12.1	6.2	6.4	8.5	10.6	13.3	
		1.2	7.7	7.9	8.9	10.0	13.5	8.5	8.7	9.8	11.0	14.7	
t_{PHZ}, t_{PLZ}	Output Disable, $\overline{OE}$ to B	3.3	6.2	6.4	8.1	9.3	10.2	6.9	7.1	9.0	10.3	11.3	nS
		2.5	5.2	6.2	8.2	8.8	10.4	5.8	6.9	9.1	10.4	11.5	
		1.8	6.9	6.9	8.7	9.9	10.9	7.6	7.6	9.6	10.9	12.0	
		1.5	7.6	7.4	9.1	10.3	11.3	8.2	8.4	10.1	11.4	12.5	
		1.2	8.1	8.1	9.5	9.6	12.4	9.0	10.1	10.5	10.6	13.7	

5. Propagation delays defined per Figure 3.
6. These parameters are guaranteed by characterization and are not production tested.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 4)	Unit
C_{IN}	Control Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}	2.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}	5.0	pF
C_{PD} (Note 7)	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}, f = 10 MHz	12	pF

7. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

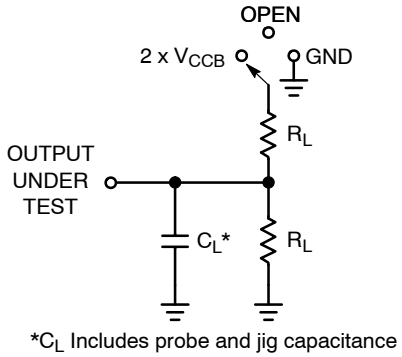


Figure 3. AC Test Circuit

Test	Switch	C_L	R_L
t_{PLH}, t_{PHL}	OPEN	15 pF	2 kΩ
t_{PLZ}, t_{PZL}	2 x V_{CCB}		
t_{PHZ}, t_{PZH}	GND		
C_L includes probe and jig capacitance Pulse generator Z_O = 50 Ω Input f = 1.0 MHz; t_W = 500 ns			

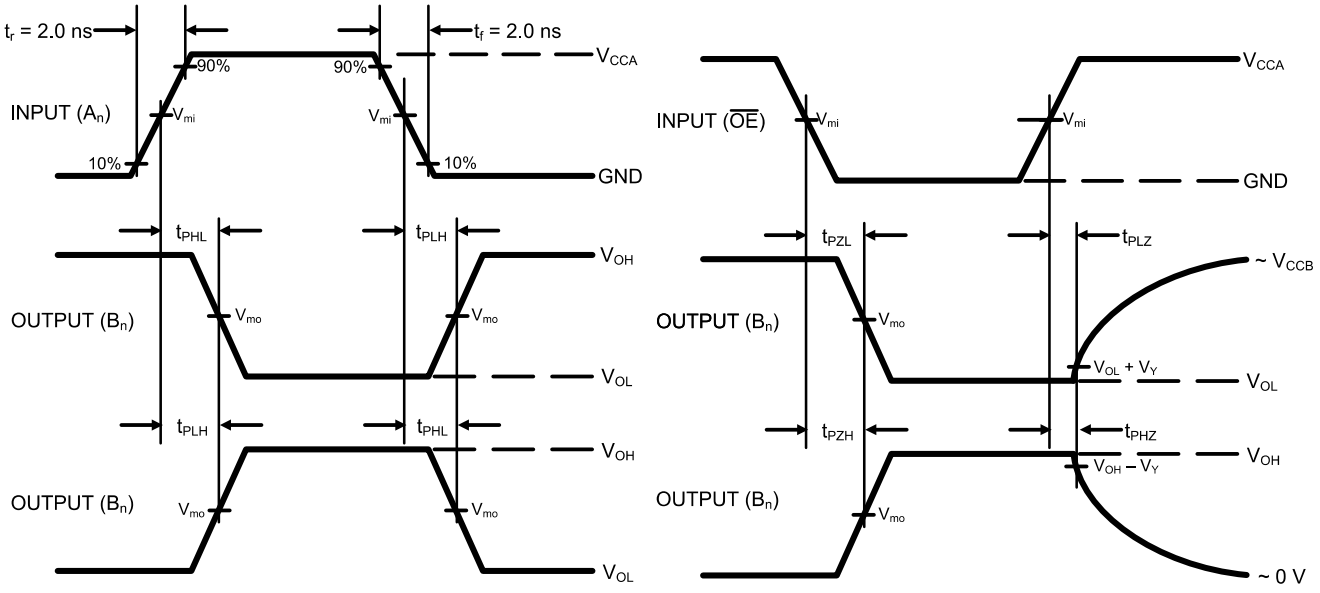


Figure 4. AC Waveforms

Symbol	V_{CC}				
	3.0 V – 3.6 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	1.1 V – 1.3 V
V_{mi}	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2	V_{CCA}/2
V_{mo}	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2	V_{CCB}/2
V_Y	0.3 V	0.15 V	0.15 V	0.1 V	0.1 V

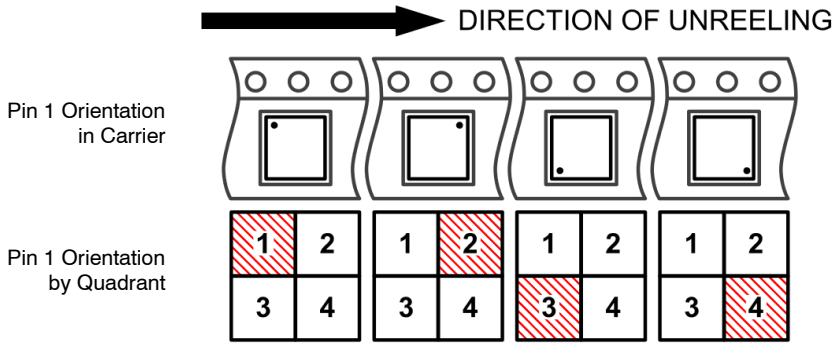
ORDERING INFORMATION

Device	Marking	Package	Pin 1 Quadrant	Shipping†
NL3V1T34DFT2G	AFR	SC−88A	3	3000 Units / Tape & Reel
NL3V1T34DFT2G−Q*	AFR	SC−88A	3	3000 Units / Tape & Reel
NL3V1T34MU1TAG	AD	UDFN6, 1.45x1, 0.5P	1	3000 Units / Tape & Reel
NL3V1T34MU1TCG	AD	UDFN6, 1.45x1, 0.5P	3	3000 Units / Tape & Reel
NL3V1T34MU2TBG	EQ	UDFN6, 1.2x1, 0.4P	2	3000 Units / Tape & Reel
NL3V1T244MU2TBG	AQ	UDFN6, 1.2x1, 0.4P	2	3000 Units / Tape & Reel
NL3V1T244MU2TBG−Q*	AQ	UDFN6, 1.2x1, 0.4P	2	3000 Units / Tape & Reel
NL3V1T240MU2TBG	A3	UDFN6, 1.2x1, 0.4P	2	3000 Units / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



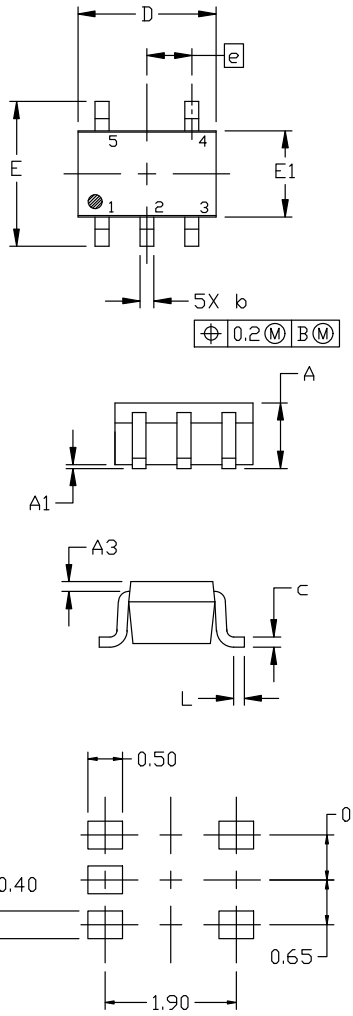
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	8/20/2025

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

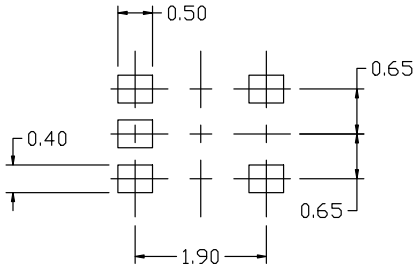
DATE 11 APR 2023

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

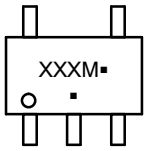
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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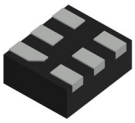
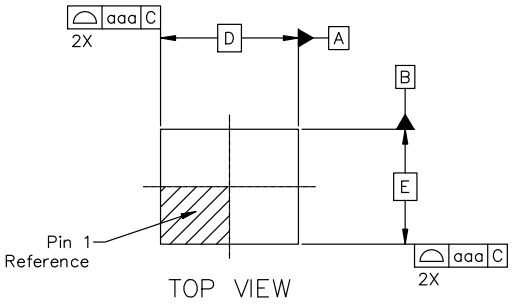
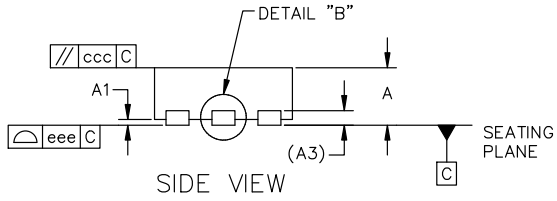
DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

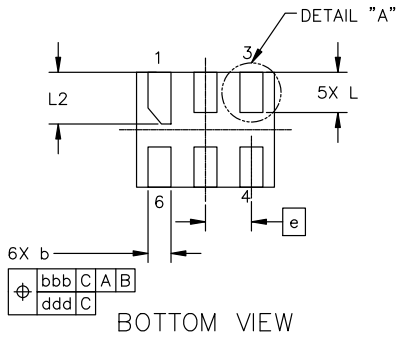


UDFN6, 1.20x1.00x0.50, 0.40P
CASE 517AA
ISSUE E

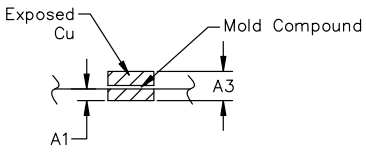
DATE 09 MAY 2025



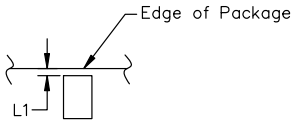




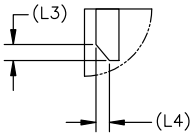
NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO TH EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL "B"
Scale 2:1
Side View
(Optional)



DETAIL "A"
Scale 2:1
Bottom View
(Optional)



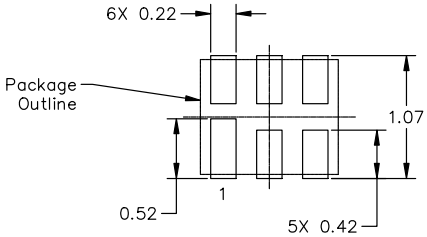
PIN 1
Chamfer Dimension

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3		0.127 REF	
b	0.15	0.20	0.25
D		1.20 BSC	
E		1.00 BSC	
e		0.40 BSC	
L	0.30	0.35	0.40
L1	0.00	---	0.15
L2	0.40	0.45	0.50
L3		0.14 REF	
L4		0.116 REF	
TOLERANCE FORM & POSITION			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

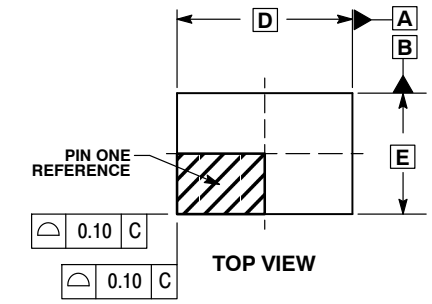
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

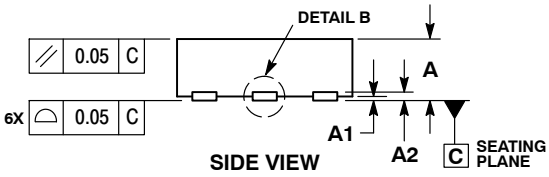
DOCUMENT NUMBER:	**98AON22068D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**UDFN6, 1.20x1.00x0.50, 0.40P**		**PAGE 1 OF 1**

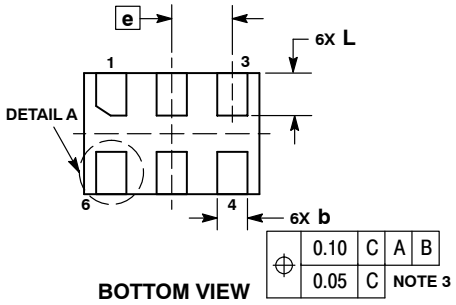
SCALE 4:1

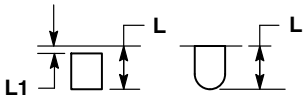
UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

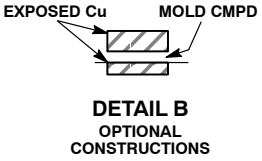
DATE 15 MAY 2008







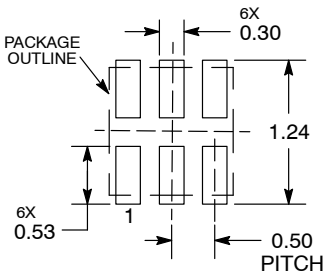




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON30313E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN6, 1.45x1.0, 0.5P**		**PAGE 1 OF 1**

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