

Configurable Multifunction Gate

NLV7SZ58

The NLV7SZ58 is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions AND, OR, NAND, NOR, XOR, INVERT and BUFFER.

Features

- $\bullet\,$ Designed for 1.65 V to 5.5 V V_{CC} Operation
- 3.3 ns t_{PD} at $V_{CC} = 5 \text{ V (Typ)}$
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Available in SC-88 Package
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS



SC-88 CASE 419B-02



XXX = Specific Device Code

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location or may not be present)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

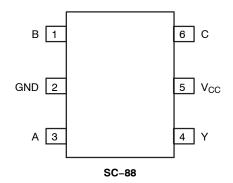


Figure 1. Pinout (Top View)

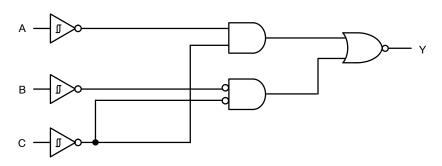


Figure 2. Function Diagram

PIN ASSIGNMENT

Pin	Function
1	В
2	GND
3	А
4	Υ
5	V _{CC}
6	С

FUNCTION TABLE*

	Output		
Α	В	С	Υ
L	L	L	L
L	L	Н	Н
L	Н	L	L
L	Н	Н	L
Н	L	L	Н
Н	L	Н	Н
Н	Н	L	Н
Н	Н	Н	L

 $[\]mbox{\ensuremath{^{\star}}}\mbox{To}$ select a logic function, please refer to "Logic Configurations section".

LOGIC CONFIGURATIONS

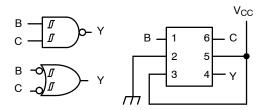


Figure 3. 2-Input NAND (When A = "H")

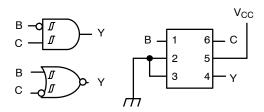


Figure 4. 2-Input AND with Input B Inverted (When A = "L")

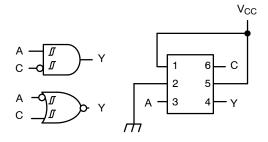


Figure 5. 2-Input AND with Input C Inverted (When B = "H")

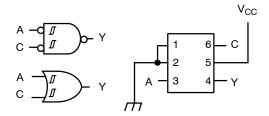


Figure 6. 2-Input OR (When B = "L")

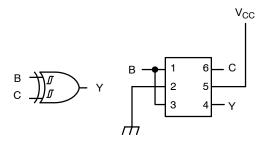


Figure 7. 2-Input XOR (When A = B)

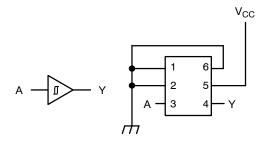


Figure 8. Buffer (When B = C = "L")

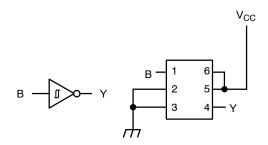


Figure 9. Inverter (When A = "L" and C = "H")

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage Active–Mode (High or Low State Tri–State Mode (Note Power–Down Mode ($V_{\rm CC}$ = 0 \	–0.5 to +7.0	٧
I _{IK}	DC Input Diode Current V _{IN} < GN	O –50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GN	O -50	mA
I _{OUT}	DC Output Source/Sink Current	±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Secs	260	°C
TJ	Junction Temperature Under Bias	+150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 2) SC-8	8 377	°C/W
P_{D}	Power Dissipation in Still Air SC-8	8 332	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Oxygen Index: 28 to 3	4 UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Mod Charged Device Mod Charged Device Mod	el >200	٧
I _{LATCHUP}	Latchup Performance (Note 4)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Applicable to devices with outputs that may be tri-stated.
- Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
 CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued
- per JEDEC/JEP172A.
 4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Para	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage		1.65	5.5	V
V _{IN}	DC Input Voltage		0	5.5	V
V _{OUT}	DC Output Voltage	Active–Mode (High or Low State) Tri–State Mode (Note 1) Power–Down Mode ($V_{CC} = 0 \text{ V}$)	0	5.5	V
T _A	Operating Free-Air Temperature		-55	+125	°C
t _r , t _f	Input Rise or Fall Rate	$\begin{array}{c} V_{CC} = 1.65 \ V \ to \ 1.95 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 3.0 \ V \ to \ 3.6 \ V \\ V_{CC} = 4.5 \ V \ to \ 5.5 \ V \end{array}$	0 0 0	No Limit No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	-	Γ _A = 25°(D		≤ T _A ≤ °C		≤ T _A ≤ 5°C	
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{T+}	Positive Input		1.65	0.79	-	1.16	-	1.16	-	1.16	V
	Threshold Voltage		2.3	1.11	_	1.56	-	1.56	-	1.56	
			3.0	1.5	-	1.87	-	1.87	-	1.87	
			4.5	2.16	_	2.74	-	2.74	-	2.74	
			5.5	2.61	-	3.33	-	3.33	-	3.33	
V_{T-}	Negative Input		1.65	0.35	_	0.62	0.35	-	0.35	_	V
	Threshold Voltage		2.3	0.58	_	0.87	0.58	-	0.58	_	
			3.0	0.84	-	1.19	0.84	-	0.84	-	
			4.5	1.41	-	1.9	1.41	-	1.41	-	
			5.5	1.78	-	2.2	1.78	-	1.78	-	
V _H	Negative Input		1.65	0.3	-	0.62	0.3	0.62	0.3	0.62	V
	Threshold Voltage		2.3	0.4	-	0.8	0.4	0.8	0.4	0.8	
			3.0	0.53	-	0.87	0.53	0.87	0.53	0.87	
			4.5	0.71	-	1.04	0.71	1.04	0.71	1.04	
			5.5	0.8	-	1.2	0.8	1.2	0.8	1.2	
V _{OH}	High-Level Output Voltage	I _{OH} = -50 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}	-	V _{CC} - 0.1	-	V _{CC} - 0.1	-	V
	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -4 \text{ mA}$	1.65	1.20	1.52	-	1.20	-	1.20	-	
		I _{OH} = -8 mA	2.3	1.9	2.1	_	1.9	-	1.9	-	
		I _{OH} = -16 mA	3	2.4	2.7	-	2.4	-	2.4	-	
		I _{OH} = -24 mA	3	2.3	2.5	-	2.3	-	2.3	-	
		I _{OH} = -32 mA	4.5	3.8	4	_	3.8	-	3.8	-	
V _{OL}	Low-Level Output Voltage	I _{OL} = 100 μA	1.65 to 5.5	-	-	0.1	_	0.1	-	0.1	V
	$V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 4 mA	1.65	_	0.08	0.45	-	0.45	-	0.45	
		I _{OL} = 8 mA	2.3	_	0.2	0.3	-	0.3	-	0.4	
		I _{OL} = 16 mA	3	-	0.28	0.4	-	0.4	-	0.5	
		I _{OL} = 24 mA	3	-	0.38	0.55	-	0.55	-	0.55	
		I _{OL} = 32 mA	4.5	-	0.42	0.55	-	0.55	-	0.65	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	+0.1	-	+1.0	-	+1.0	μΑ
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	-	-	1.0	-	10	-	10	μΑ
Icc	Quiescent Supply Current	V _{IN} = 5.5 V or GND	5.5	_	-	1.0	-	10	_	10	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

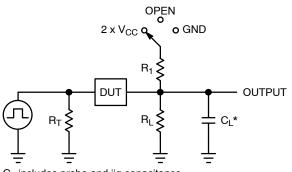
AC ELECTRICAL CHARACTERISTICS

				7	Γ _A = 25°0	C	-40°C 85	≤ T _A ≤ °C		≤ T _A ≤ 5°C	
Symbol	Parameter	Condition	V _{CC} (V)	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL} Propagation Delay, (A or B or C) to Y (Figures 10 and 11)	$R_L = 1 \text{ k}\Omega,$ $C_L = 30 \text{ pF}$	1.65 to 1.95	_	8.6	14.4	-	14.4	-	14.4	ns	
	ures 10 and 11)	$R_L = 500 \Omega$, $CL = 30 pF$	2.3 to 2.7	_	5.1	8.3	-	8.3	-	8.3	
		$R_L = 500 \Omega,$ $C_L = 50 pF$	3.0 to 3.6	-	3.9	6.3	-	6.3	-	6.3	
	C _L = 50 pF 4.5 to 5.5	4.5 to 5.5	-	3.3	5.1	_	5.1	-	5.1		

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C _{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_{IN} = 0 V or V_{CC} 10 MHz, V_{CC} = 5.0 V, V_{IN} = 0 V or V_{CC}	16 19.5	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC} \cdot C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.



Test	Switch Position	C _L , pF	R_L, Ω	R ₁ , Ω		
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table				
t _{PLZ} / t _{PZL}	2 x V _{CC}	50	500	500		
t _{PHZ} / t _{PZH}	GND	50	500	500		

X = Don't Care

 C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 $\Omega)$ f = 1 MHz

Figure 10. Test Circuit

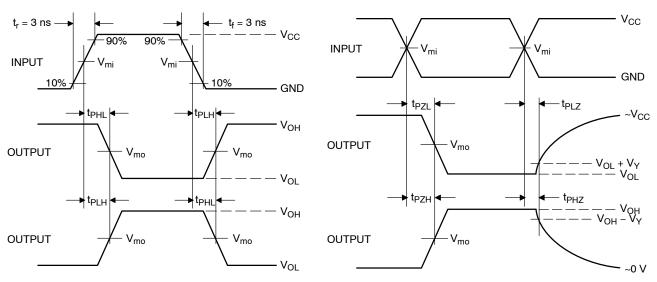


Figure 11. Switching Waveforms

		,		
V _{CC} , V	V _{mi} , V	t _{PLH} , t _{PHL}	t _{PZL} , t _{PLZ} , t _{PZH} , t _{PHZ}	V _Y , V
1.65 to 1.95	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.15
2.3 to 2.7	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.15
3.0 to 3.6	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.3
4.5 to 5.5	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.3

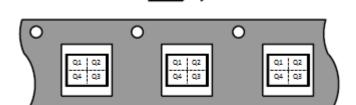
ORDERING INFORMATION

Device	Package	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
NLV7SZ58DFT2G*	SC-88 (Pb-Free)	MM	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN 1 ORIENTATION IN TAPE AND REEL

Direction of Feed

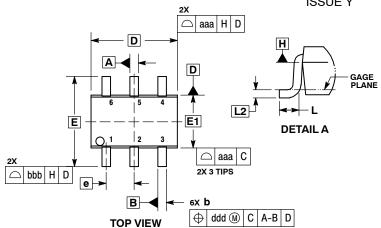


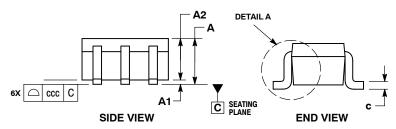
^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC-88/SC70-6/SOT-363

CASE 419B-02 **ISSUE Y**



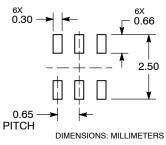


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 - CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH. PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU-SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H. DATUMS A AND B ARE DETERMINED AT DATUM H.

- DIMENSIONS 6 AND 6 APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION.
 ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 5 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α			1.10			0.043	
A1	0.00		0.10	0.000		0.004	
A2	0.70	0.90	1.00	0.027	0.035	0.039	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.08	0.15	0.22	0.003	0.006	0.009	
D	1.80	2.00	2.20	0.070	0.078	0.086	
E	2.00	2.10	2.20	0.078	0.082	0.086	
E1	1.15	1.25	1.35	0.045	0.049	0.053	
е		0.65 BS	С	0.026 BSC			
L	0.26	0.36	0.46	0.010	0.014	0.018	
L2		0.15 BS	C	(0.006 BS	SC	
aaa	0.15				0.006		
bbb	0.30				0.012		
ccc	0.10				0.004		
ddd		0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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