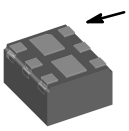
Bias Resistor Transistors (BRT)

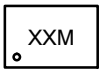
Dual NPN/NPN, R1 = 22 Ω, R2 = 47 Ω

NSBC124XD



WDFNW6
CASE 515AT

MARKING DIAGRAM

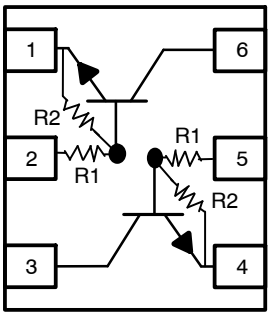


XX = Specific Device Code
M = Month Code

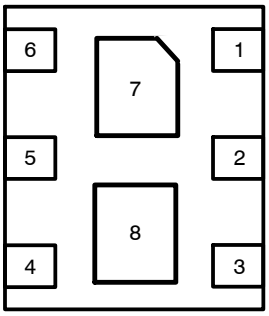
The series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor contains a single transistor with a monolithic bias network consisting of two resistors: a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. They are housed in the WDF1412-6 package offering superior thermal performance. The transistor is ideal for surface mount applications where board space and reliability are at a premium.

Features

- Built in Bias Resistors
- Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



Top



Bottom

MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Min	Max	Unit
Collector-Emitter Voltage	V_{CEO}		50	V
Collector-Base Voltage	V_{CBO}		50	V
Input Voltage	V_I	−8	+40	V
Collector Current	I_C		100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PIN CONNECTIONS

Pin	Description
1	Emitter (ground) T1
2	Base (input) T1
3	Collector (output) T2
4	Emitter (ground) T2
5	Base (input) T2
6	Collector (output) T1
7	Collector (output) T1
8	Collector (output) T2

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL CHARACTERISTICS

Characteristic (Per Transistor)	Symbol	Max	Unit
Total Power Dissipation @ T_A = 25 °C (Note 1) Derate above 25 °C	P_D	310 2.5	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	400	°C/W
Characteristic (Per Device)	**Symbol**	**Max**	**Unit**
Total Power Dissipation @ T_A = 25 °C (Note 1) Derate above 25 °C	P_D	417 3.3	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	300	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. Per JESD51-7 with standard PCB footprint and 2 oz. Cu.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nA
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nA
Emitter-Base Cutoff Current (V_{EB} = 6 V, I_C = 0)		I_{EBO}	–	–	0.13	mA
DC Current Gain (V_{CE} = 10 V, I_C = 5 mA)		h_{FE}	80	150	–	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.5 mA)		$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (off) (V_{CE} = 5.0 V, I_C = 100 μA)		$V_{I(off)}$	–	0.9	0.5	V
Input Voltage (on)	(V_{CE} = 0.3 V, I_C = 2 mA)	$V_{I(on)}$	2.0	1.2	–	V
Output Voltage (n) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)		V_{OL}	–	–	0.2	V
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	–	–	V
Bias Resistor (R1)		R1	15.4	22	28.6	kΩ
Resistor Ratio		R1/R2	0.38	0.47	0.56	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Device-Automotive*	R1	R2	Part Marking	Package†	Shipping†
NSBC124XDMTWTBG	NSVBC124XDMTWTBG	22	47	AC	WDFNW6 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

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TYPICAL CHARACTERISTICS (NSBC124X)

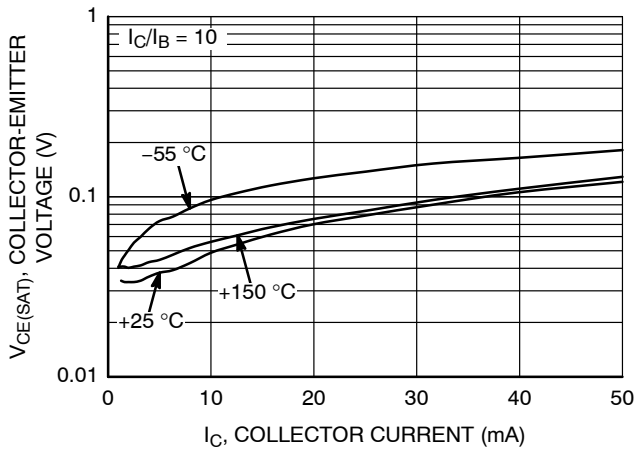


Figure 1. $V_{CE(sat)}$ vs. I_C

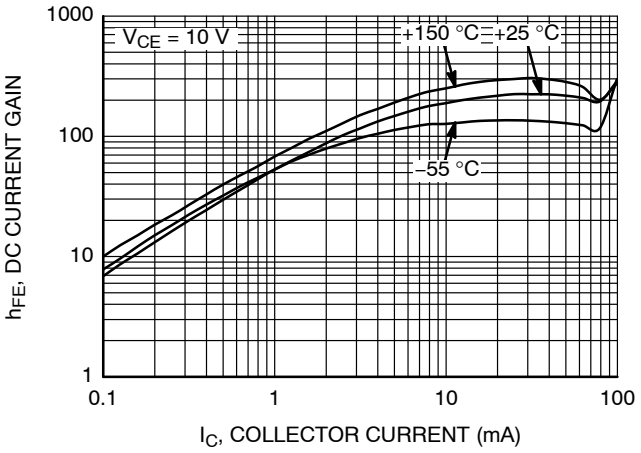


Figure 2. DC Current Gain

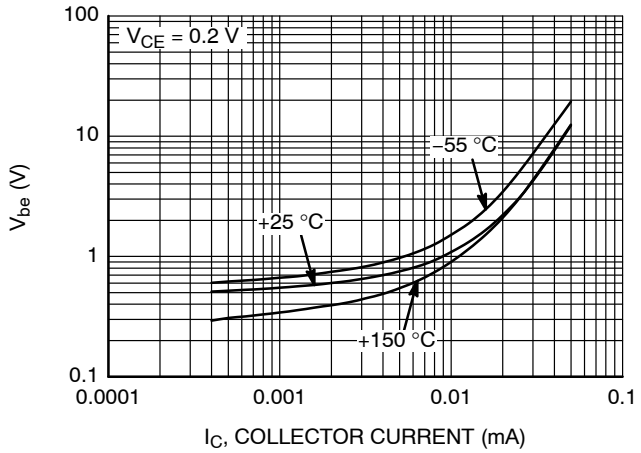


Figure 3. (Onstate) Input Voltage vs. Output Current

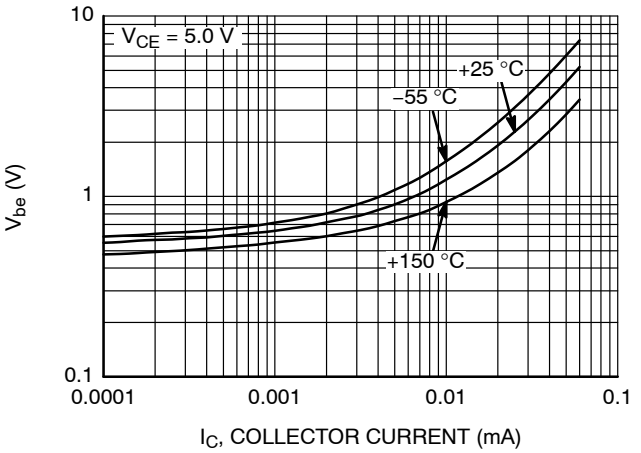


Figure 4. (Offstate) Input Voltage vs. Output Current

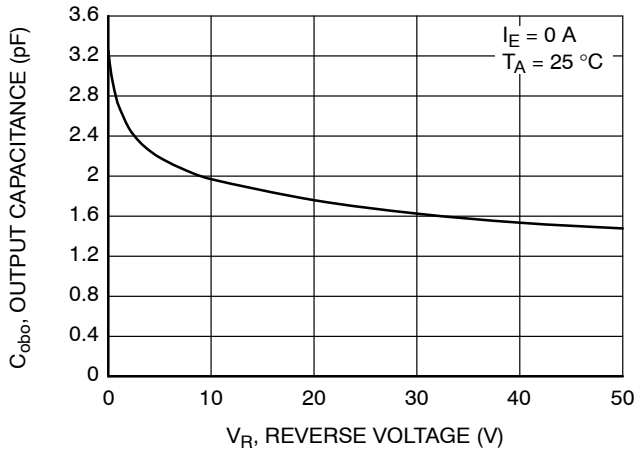


Figure 5. Output Capacitance, f = 1 MHz

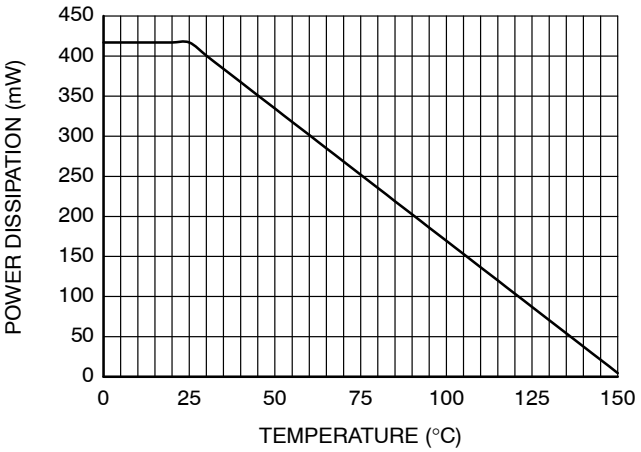


Figure 6. Derating Curve

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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial Production Datasheet Release.	10/26/2026

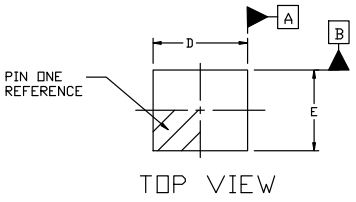
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

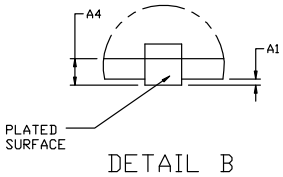


WDFNW6 1.4x1.2, 0.5P (DUAL)
CASE 515AT
ISSUE O

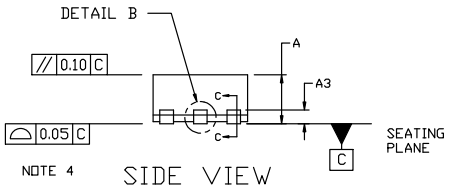
DATE 04 OCT 2022



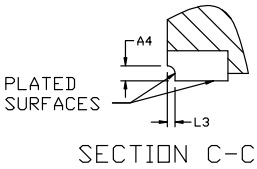
TOP VIEW



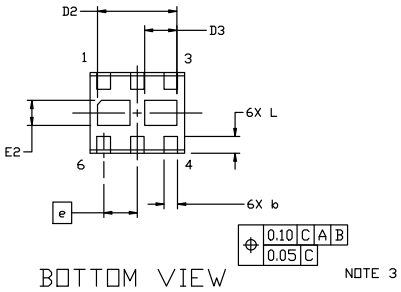
DETAIL B



SIDE VIEW



SECTION C-C

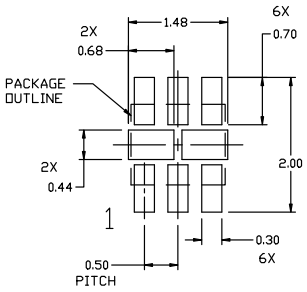


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

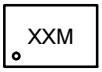
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.65	0.75	0.80
A1	0.00	-----	0.05
A3		0.20 REF	
A4	0.10	-----	-----
b	0.15	0.20	0.25
D	1.30	1.40	1.50
D2	1.13	1.18	1.23
D3	0.43	0.48	0.53
E	1.10	1.20	1.30
E2	0.32	0.37	0.42
e		0.50 BSC	
L	0.15	0.25	0.35
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFNW6 1.4x1.2, 0.5P (DUAL)**	**PAGE 1 OF 1**

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