

# MOSFET – Power, Single N-Channel, D<sup>2</sup>PAK7

**100 V, 4.1 mΩ, 203 A**

## NTBGS004N10G

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Wide SOA
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Hot Swap in 48 V Systems

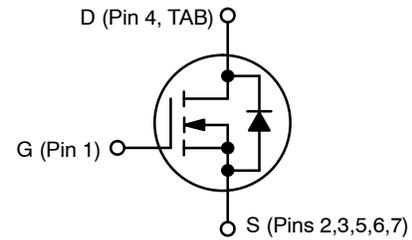
### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	100	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	203	A
			$P_D$	340	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	21	A
			$P_D$	3.7	W
Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}$ , $t_p = 10\text{ }\mu\text{s}$		$I_{DM}$	2983	A
Operating Junction and Storage Temperature			$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			$I_S$	283	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 106\text{ A}_{pk}$ , $L = 0.1\text{ mH}$ )			$E_{AS}$	561	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^\circ\text{C}$

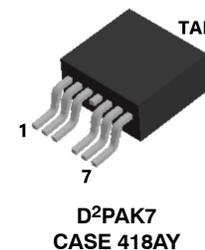
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
100 V	4.1 mΩ @ 10 V	203 A



**N-CHANNEL MOSFET**



### MARKING DIAGRAM

AYWWZZ
NTBG
S004N10G

A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code  
 NTBGS004N10G = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBGS004N10G	D <sup>2</sup> PAK7 (Pb-Free)	800 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.44	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25\text{ }^\circ\text{C}$		81.3		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125\text{ }^\circ\text{C}$		100	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 500\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 500\text{ }\mu\text{A}$ , ref to $25\text{ }^\circ\text{C}$		-9.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		3.0	4.1	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 100\text{ A}$		71		S
Gate-Resistance	$R_G$	$T_A = 25\text{ }^\circ\text{C}$		0.42		$\Omega$

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		12100		pF
Output Capacitance	$C_{OSS}$			1170		
Reverse Transfer Capacitance	$C_{RSS}$			165		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 100\text{ A}$		178		nC
Threshold Gate Charge	$Q_{G(TH)}$			79		
Gate-to-Source Charge	$Q_{GS}$			66		
Gate-to-Drain Charge	$Q_{GD}$			43		
Plateau Voltage	$V_{GP}$			6.0		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 100\text{ A}, R_G = 4.7\text{ }\Omega$		44		ns
Rise Time	$t_r$			41		
Turn-Off Delay Time	$t_{d(OFF)}$			81		
Fall Time	$t_f$			29		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 100\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$		0.88	1.2	V
			$T_J = 125\text{ }^\circ\text{C}$		0.77		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		74		ns	
Charge Time	$t_a$			46			
Discharge Time	$t_b$			29			
Reverse Recovery Charge	$Q_{RR}$			151			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

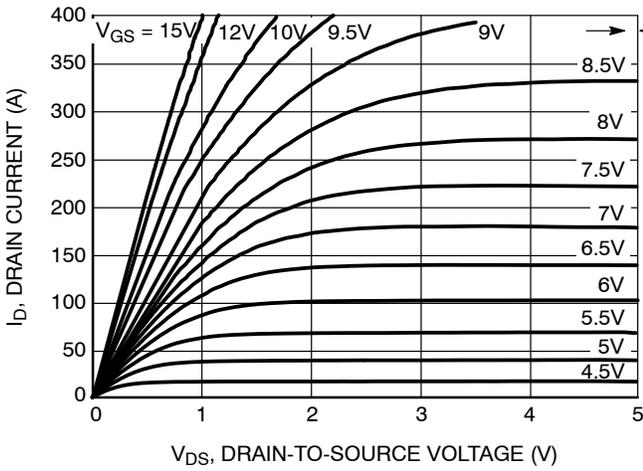


Figure 1. On-Region Characteristics

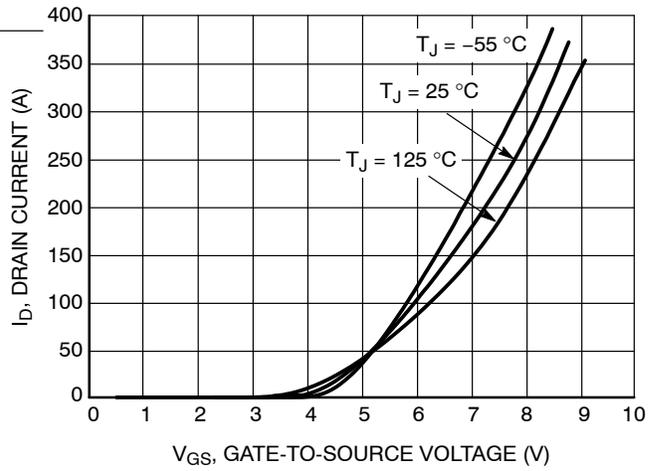


Figure 2. Transfer Characteristics

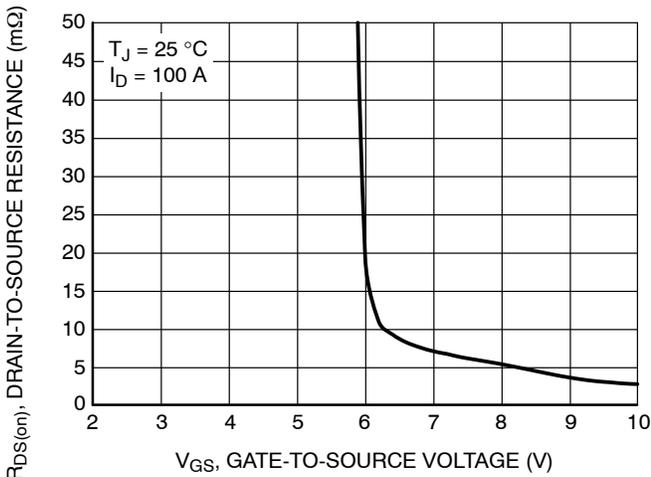


Figure 3. On-Resistance vs. Gate-to-Source Voltage

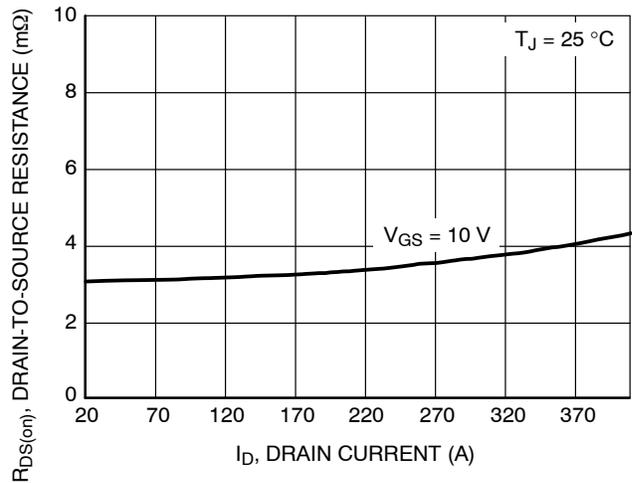


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

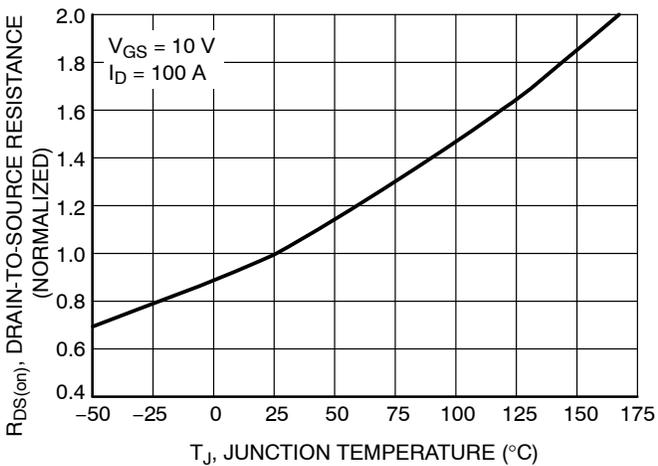


Figure 5. On-Resistance Variation with Temperature

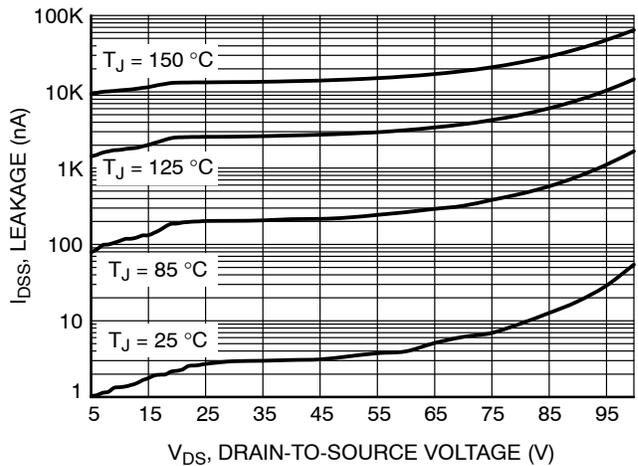
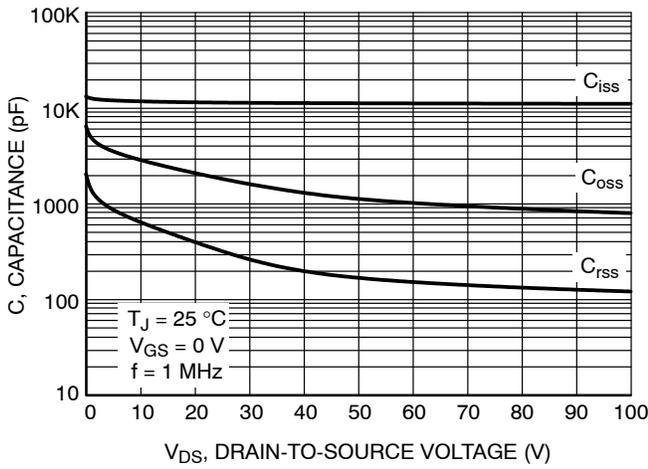


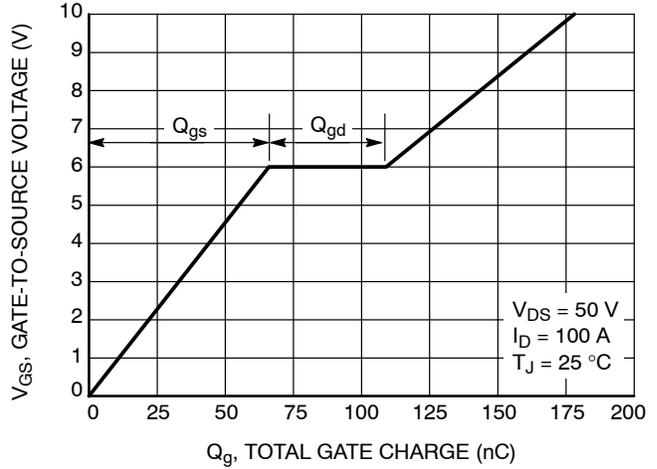
Figure 6. Drain-to-Source Leakage Current vs. Voltage

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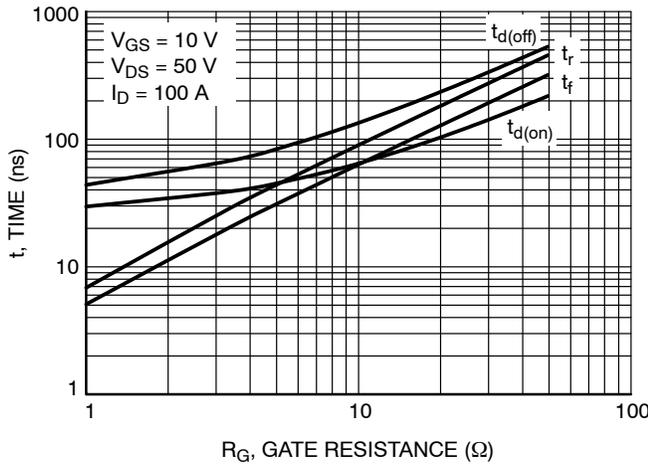
## TYPICAL CHARACTERISTICS



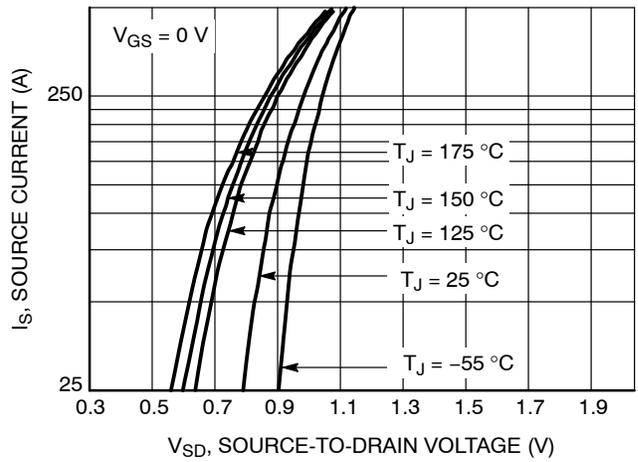
**Figure 7. Capacitance Variation**



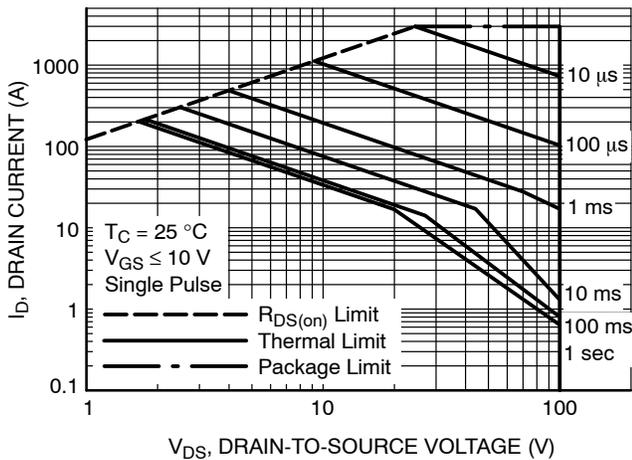
**Figure 8. Gate-to-Source vs. Total Charge**



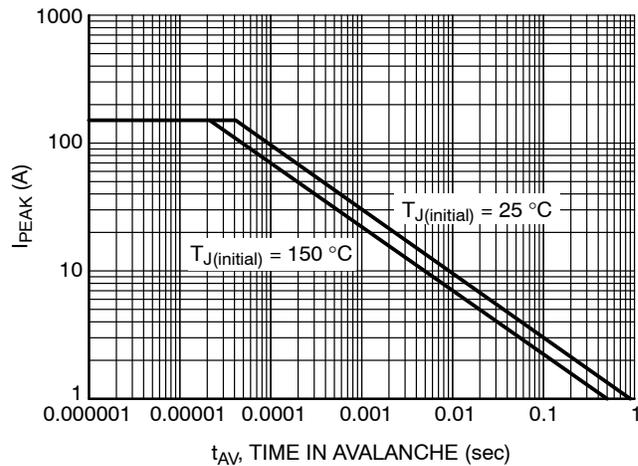
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Drain Current vs. Time in Avalanche**

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## TYPICAL CHARACTERISTICS

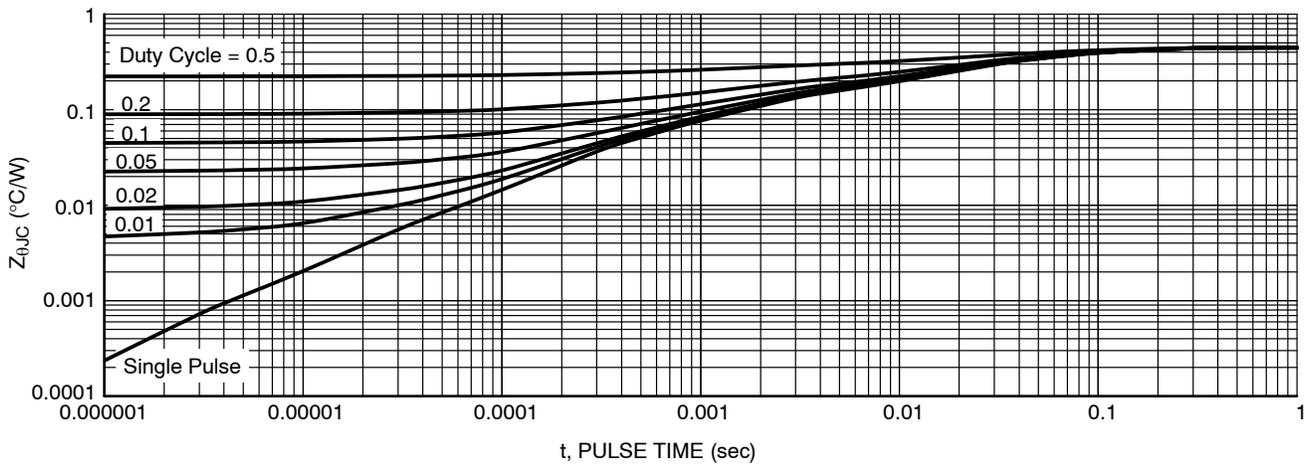


Figure 13. Transient Thermal Impedance

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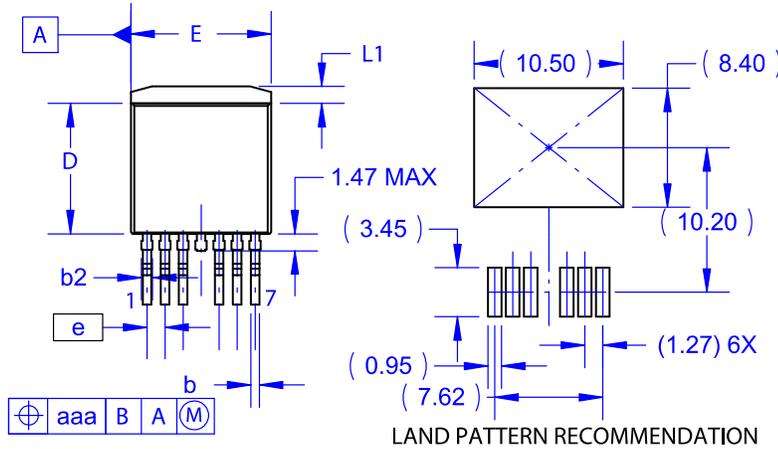
## REVISION HISTORY

Revision	Description of Changes	Date
1	Rebranded the Data Sheet to <b>onsemi</b> format and corrected curves in Figure 11 ( $R_{ds(on)}$ , thermal, package limits).	1/28/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

**D2PAK7 (TO-263 7 LD)**  
**CASE 418AY**  
**ISSUE C**

DATE 15 JUL 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC, TO127P1524X465-8N.

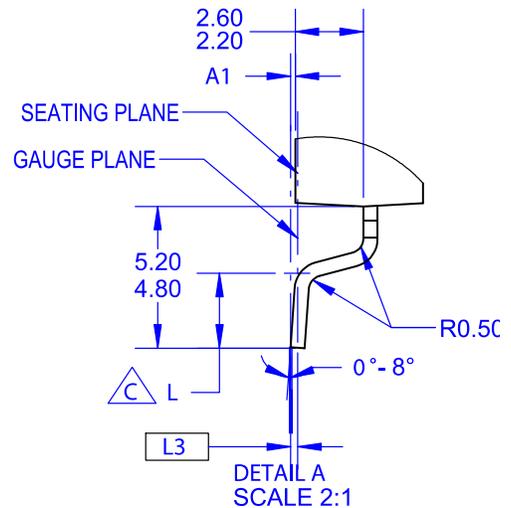
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.70	0.80	0.90
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.70	~	~
E	9.70	9.90	10.20
E1	8.38	8.58	8.78
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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<b>DESCRIPTION:</b>	<b>D2PAK7 (TO-263 7 LD)</b>	<b>PAGE 1 OF 1</b>

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