

Enhancement Mode Gallium Nitride (GaN) HEMT

650 V, 27 mΩ, 64 A, TOLL 10x12

Preliminary Document NTBL035N65GN1

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM- $Q_G = 378 \text{ nC} \cdot \text{m}\Omega$
- Small Footprint for High Density PCB Design
- Pb-Free, Halogen Free and RoHS Compliant

Typical Applications

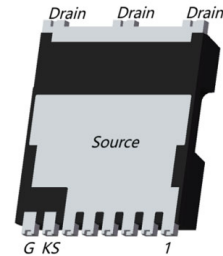
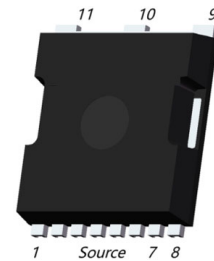
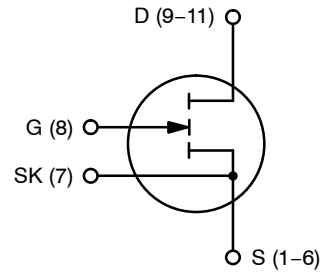
- High Density Power Modules
- High Frequency AC-DC and DC-DC Converters
- High Performance PSU for Datacenter and Industrial
- Resonant Conversion

MAXIMUM RATINGS ($T_J = 25 \text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Drain-to-Source Transient Voltage, $t_p < 200 \text{ } \mu\text{s}$	$V_{DS(TRAN)}$	800	V
Gate-to-Source Voltage	V_{GS}	-6 to 7	V
Gate-to-Source Transient Voltage, $t_p = 50 \text{ ns}$, $f_p = 100 \text{ kHz}$, open drain	$V_{GS(PULSE)}$	-20 to 10	V
Continuous Drain Current, $T_{CASE} = 25 \text{ }^\circ\text{C}$ $T_{CASE} = 100 \text{ }^\circ\text{C}$	I_{DS}	64 45	A
Pulsed Drain Current, $t_p < 10 \text{ } \mu\text{s}$, $T_J = 25 \text{ }^\circ\text{C}$ $T_J = 125 \text{ }^\circ\text{C}$	$I_{DS(PULSE)}$	127 64	A
Power Dissipation, $V_{GS} = 6 \text{ V}$, $T_{CASE} = 25 \text{ }^\circ\text{C}$	P_{TOT}	367	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_{DS} MAX
650 V	27 mΩ	64 A



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

NTBL035N65GN1

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Case	$R_{\theta JC}$	0.34	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	56	$^{\circ}\text{C}/\text{W}$
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	$^{\circ}\text{C}$

1. Device on 1 in², 2 oz copper pad on single layer FR-4 PCB

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	650			V
Drain-to-Source Leakage Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$		11	TBD	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_J = 125^{\circ}\text{C}$		29		
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}$		358	TBD	μA
		$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$		TBD		μA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_{DS} = 18\text{ A}$		27	35	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_{DS} = 18\text{ A}, T_J = 125^{\circ}\text{C}$		51		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_{DS} = 67.4\text{ mA}, T_J = 25^{\circ}\text{C}$		1.7		V
		$V_{DS} = V_{GS}, I_{DS} = 67.4\text{ mA}, T_J = 125^{\circ}\text{C}$		1.6		

DYNAMIC CHARACTERISTICS

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		488		pF
Output Capacitance	C_{OSS}			180		
Reverse Transfer Capacitance	C_{RSS}			2.2		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		271		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			381		
Output Charge	Q_{OSS}			155		nC
Output Capacitance Stored Energy	E_{OSS}			21.7		μJ
Gate Resistance	R_G		$f = 5\text{ MHz}$		1.8	
Gate Charge	Q_G	$V_{DS} = 400\text{ V}, I_{DS} = 18\text{ A}, V_{GS} = 0/6\text{ V}$		14		nC
Gate-to-Source Charge	Q_{GS}			1.3		
Gate-to-Drain Charge	Q_{GD}			5.7		
Gate Plateau Voltage	V_{PLAT}			2.3		V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{D(ON)}$	$V_{DS} = 400\text{ V}, I_{DS} = 18\text{ A}, V_{GS} = 0/6\text{ V}, R_{G,ON} = 10\ \Omega, R_{G,OFF} = 2.2\ \Omega$		TBD		ns
Turn-Off Delay Time	$t_{D(OFF)}$			TBD		ns
Turn-On Rise Time	t_R			TBD		ns
Turn-Off Fall Time	t_F			TBD		ns

REVERSE CONDUCTION CHARACTERISTICS

Source-to-Drain Reverse Voltage	V_{SD}	$V_{GS} = -2\text{ V}, I_{SD} = 18\text{ A}$		4.6		V
		$V_{GS} = 0\text{ V}, I_{SD} = 18\text{ A}$		2.6		
		$V_{GS} = 6\text{ V}, I_{SD} = 18\text{ A}$		0.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NTBL035N65GN1

Gate Drive Guidelines

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of

6 V is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

ORDERING INFORMATION

Device Order Number	Package Type	Shipping
ENGNTBL035N65GN1TXG	TOLL 10.0 x 12.0	TBD

NTBL035N65GN1

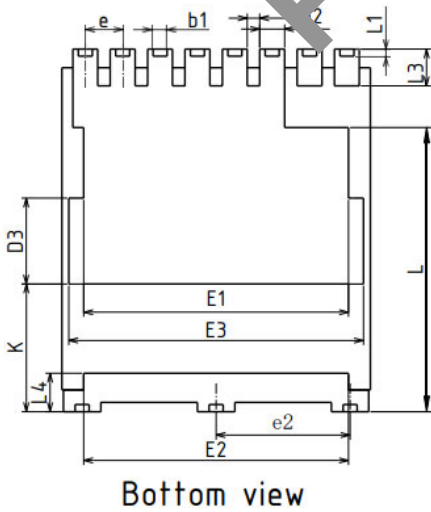
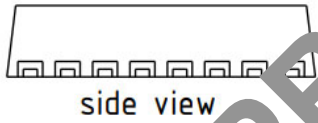
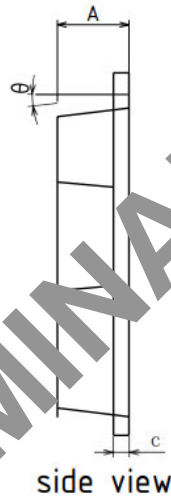
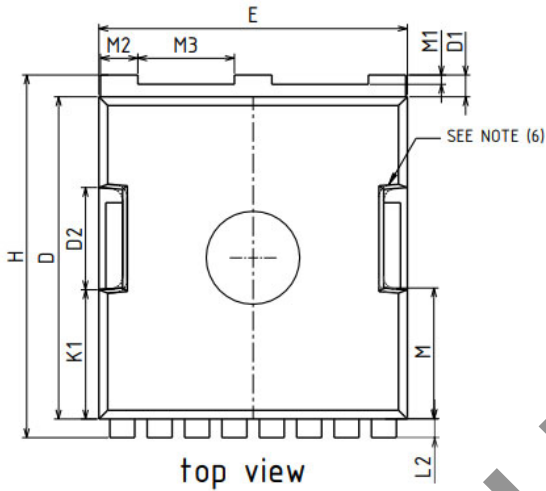
REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary Document release.	5/4/2026

NTBL035N65GN1

PACKAGE DIMENSIONS

TOLL 10 x 12 mm
CASE TBD
ISSUE O



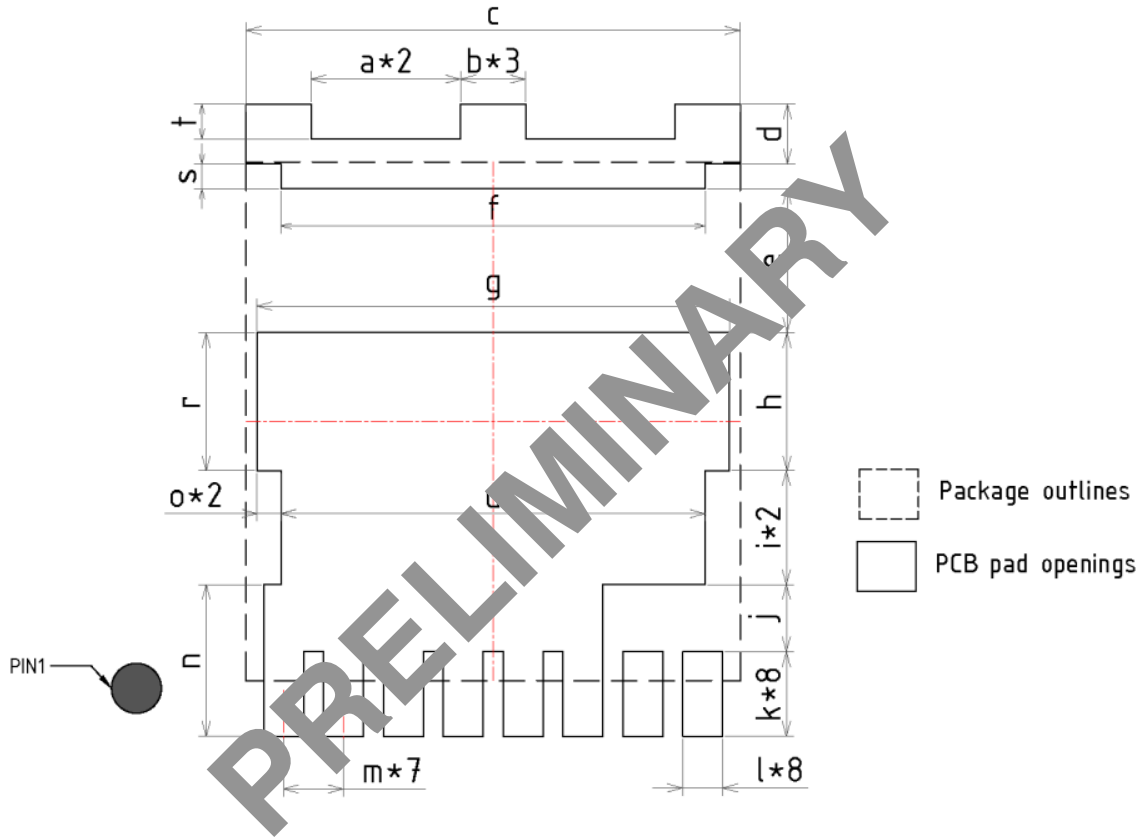
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
	2.15	2.30	2.45
b	0.30	0.40	0.50
b1	0.31	0.43	0.55
b2	0.65	0.80	0.90
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	3.30REF		
D3	2.77REF		
E	9.70	9.90	10.10
E1	8.50REF		
E2	8.50REF		
E3	9.46REF		
e	1.10	1.20	1.30
e2	4.20	4.30	4.40
H	11.48	11.68	11.88
K	4.08REF		
K1	4.18REF		
L	9.13REF		
L1	0.23REF		
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	1.00	1.20	1.40
M	4.18REF		
M1	0.26REF		
M2	1.10	1.20	1.30
M3	3.10REF		
θ	10.00REF		

All Dimensions in mm

NTBL035N65GN1

PACKAGE DIMENSIONS

LAND PATTERN



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	3.00	k	1.70
b	1.30	l	0.80
c	9.90	m	1.20
d	1.20	n	3.05
e	2.88	o	0.48
f	8.50	r	2.77
g	9.46	s	0.50
h	2.77	t	0.70
i	2.28	u	8.50
j	1.35	/	/

All Dimensions in mm

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales