MOSFET - Power, Single N-Channel, TOLL

80 V, 1.1 mΩ, 299 A

Product Preview

NTBLS1D1N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	1.1 mΩ @ 10 V	299 A

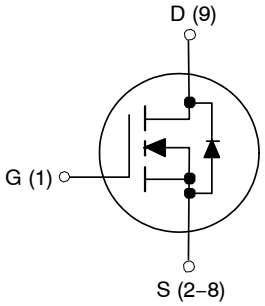
Features

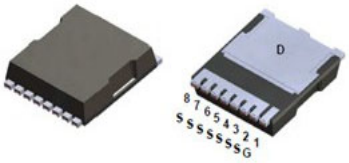
- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC−DC and AC−DC
- Primary Switch in Isolated DC−DC Converter
- Motor Drives

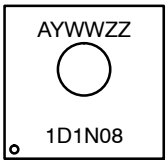
N−CHANNEL MOSFET





H−PSOF8L
CASE 100CU

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
1D1N08 = Specific Device Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	80	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	299	A
	T_C = 100°C		211	
Power Dissipation	T_C = 25°C	P_D	197	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	1925	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Continuous Source−Drain Current (Body Diode)		I_S	332	A
Single Pulse Avalanche Energy (I_{PK} = 94 A)		E_{AS}	441	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using a 1 in^2, 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 441 mJ is based on started T_J = 25°C, I_{AS} = 94 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	Package	Shipping†
NTBLS1D1N08X	H−PSOF8L (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.76	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	43	

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		33		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			1.0	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 95 A, T_J = 25°C		0.95	1.1	mΩ
		V_{GS} = 6 V, I_D = 47 A, T_J = 25°C		1.4		
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 475 μA, T_J = 25°C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 475 μA		−7		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 95 A		294		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		8620		pF
Output Capacitance	C_{OSS}			2460		
Reverse Transfer Capacitance	C_{RSS}			37		
Output Charge	Q_{OSS}			175		nC
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 40 V, I_D = 95 A, V_{GS} = 10 V		120		
Threshold Gate Charge	$Q_{G(th)}$			26		
Gate−to−Source Charge	Q_{GS}			40		
Gate−to−Drain Charge	Q_{GD}			19		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 MHz		0.67		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(on)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 95 A, R_G = 2.5 Ω		22		ns
Rise Time	t_r			118		
Turn−Off Delay Time	$t_{d(off)}$			40		
Fall Time	t_f			152		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 95 A, V_{GS} = 0 V, T_J = 25°C		0.83	1.2	V
		I_S = 95 A, V_{GS} = 0 V, T_J = 125°C		0.67		
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, I_S = 95 A dI/dt = 1000 A/μs, V_{DD} = 40 V		32		ns
Charge Time	t_a			17		
Discharge Time	t_b			15		
Reverse Recovery Charge	Q_{RR}			297		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

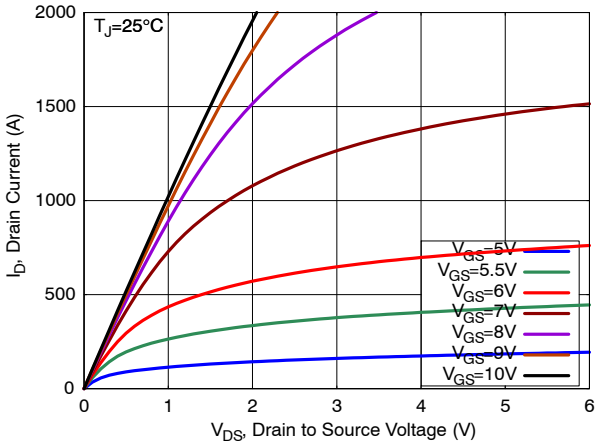


Figure 1. On−Region Characteristics

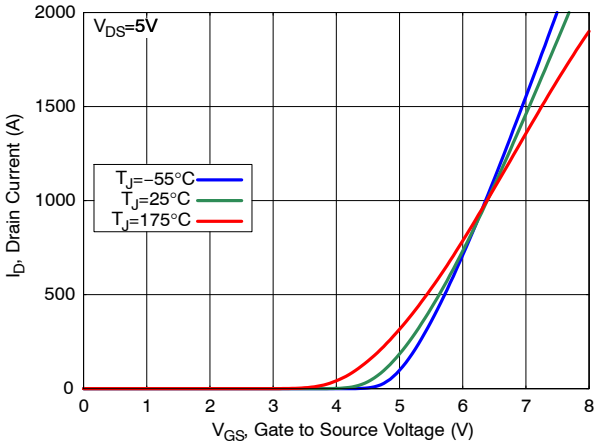


Figure 2. Transfer Characteristics

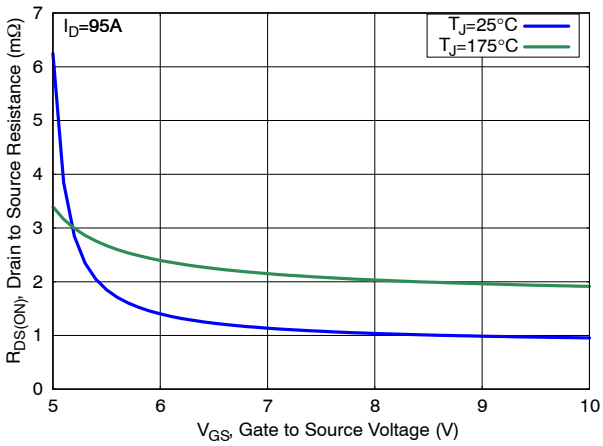


Figure 3. On−Resistance vs. Gate Voltage

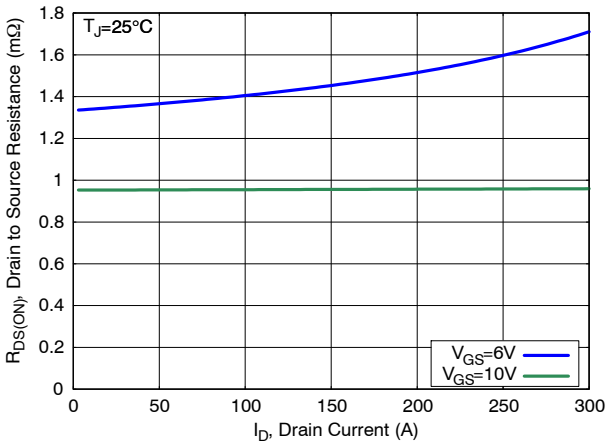


Figure 4. On−Resistance vs. Drain Current

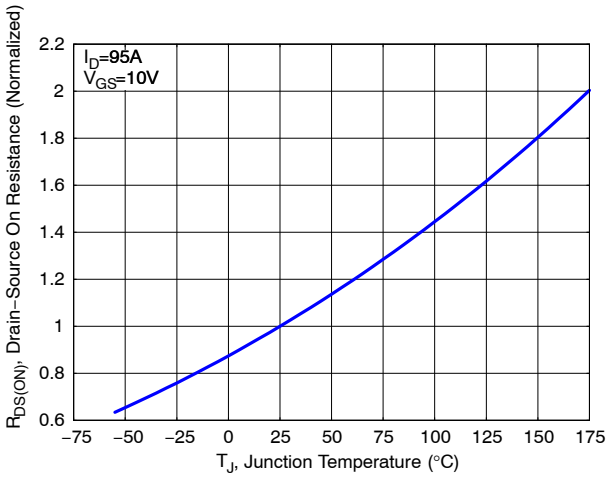


Figure 5. Normalized On−Resistance vs. Junction Temperature

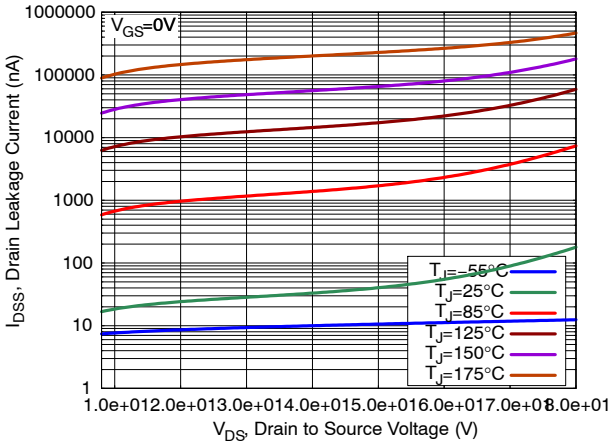


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

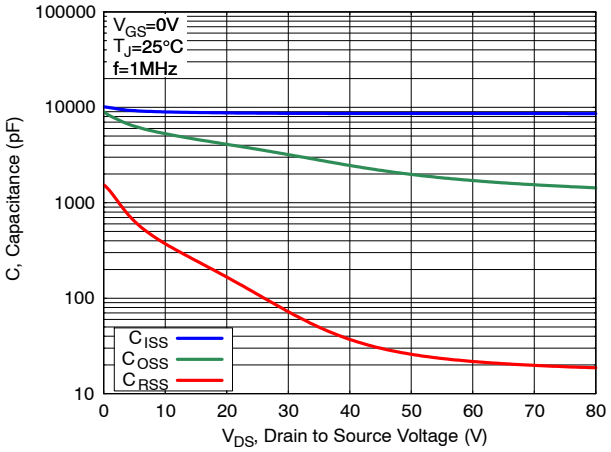


Figure 7. Capacitance Characteristics

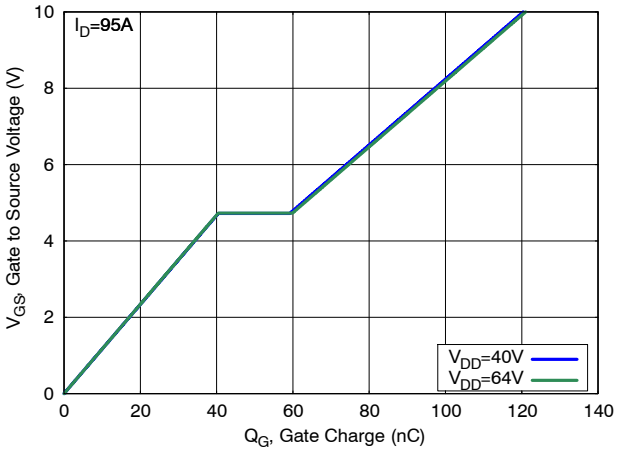


Figure 8. Gate Charge Characteristics

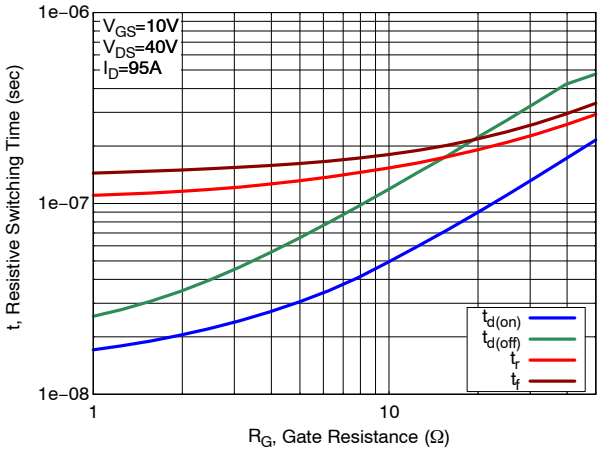


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

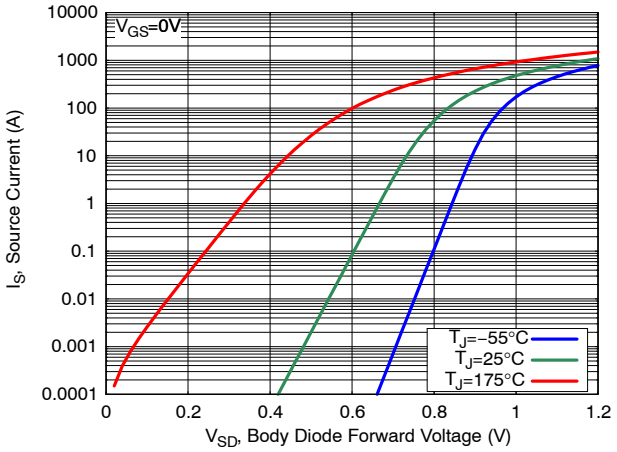


Figure 10. Diode Forward Characteristics

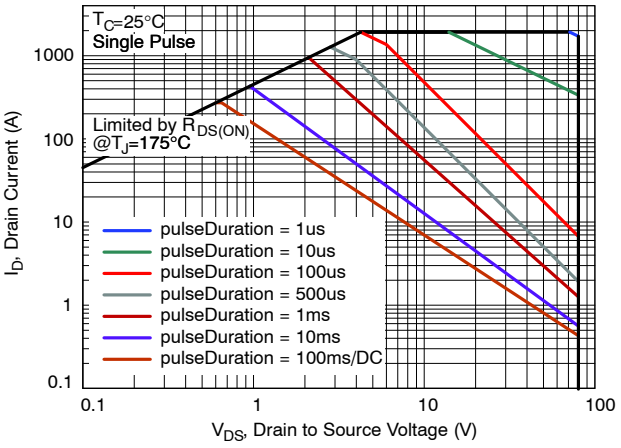


Figure 11. Safe Operating Area (SOA)

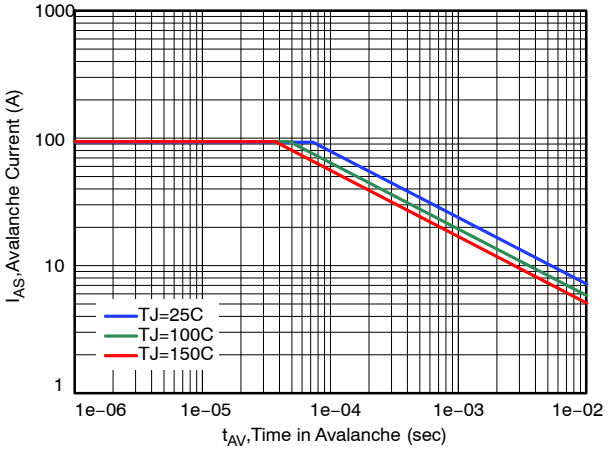


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

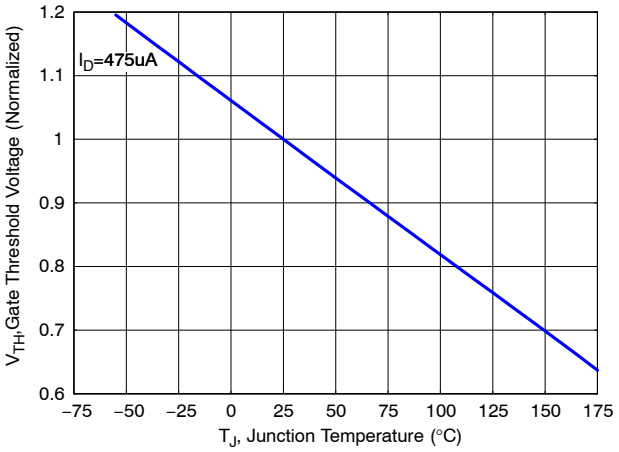


Figure 13. Gate Threshold Voltage vs. Junction Temperature

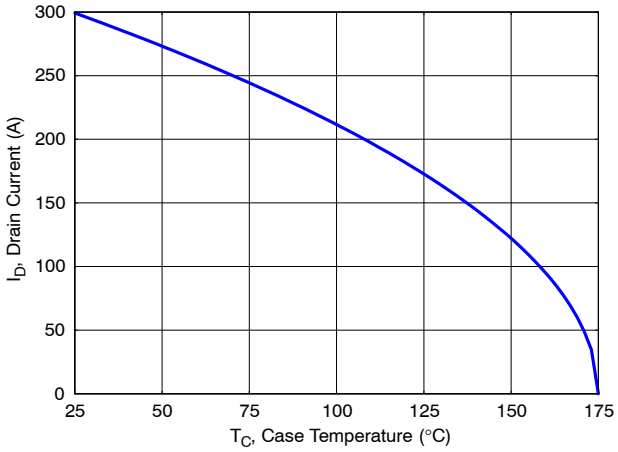


Figure 14. Maximum Current vs. Case Temperature

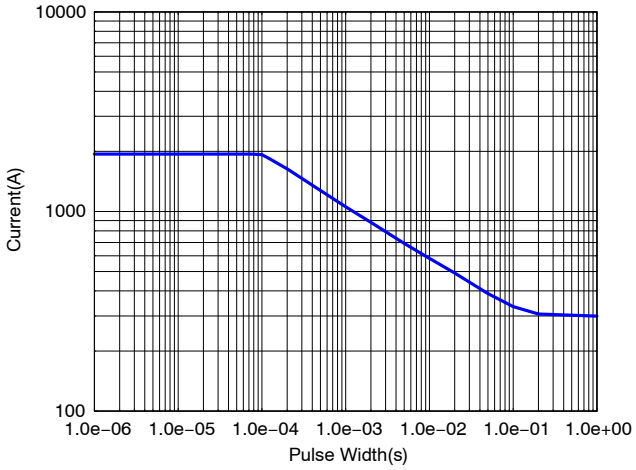


Figure 15. IDM vs. Pulse Width

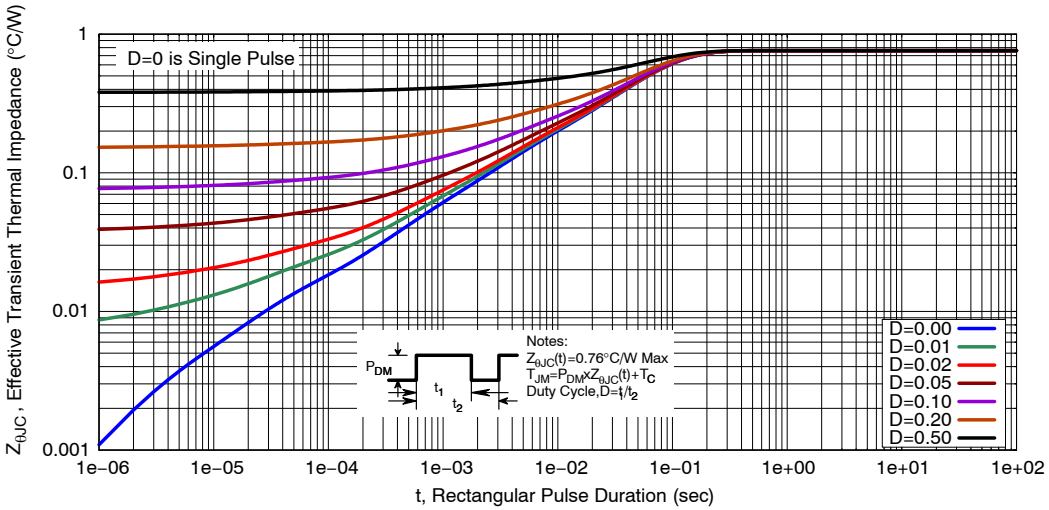
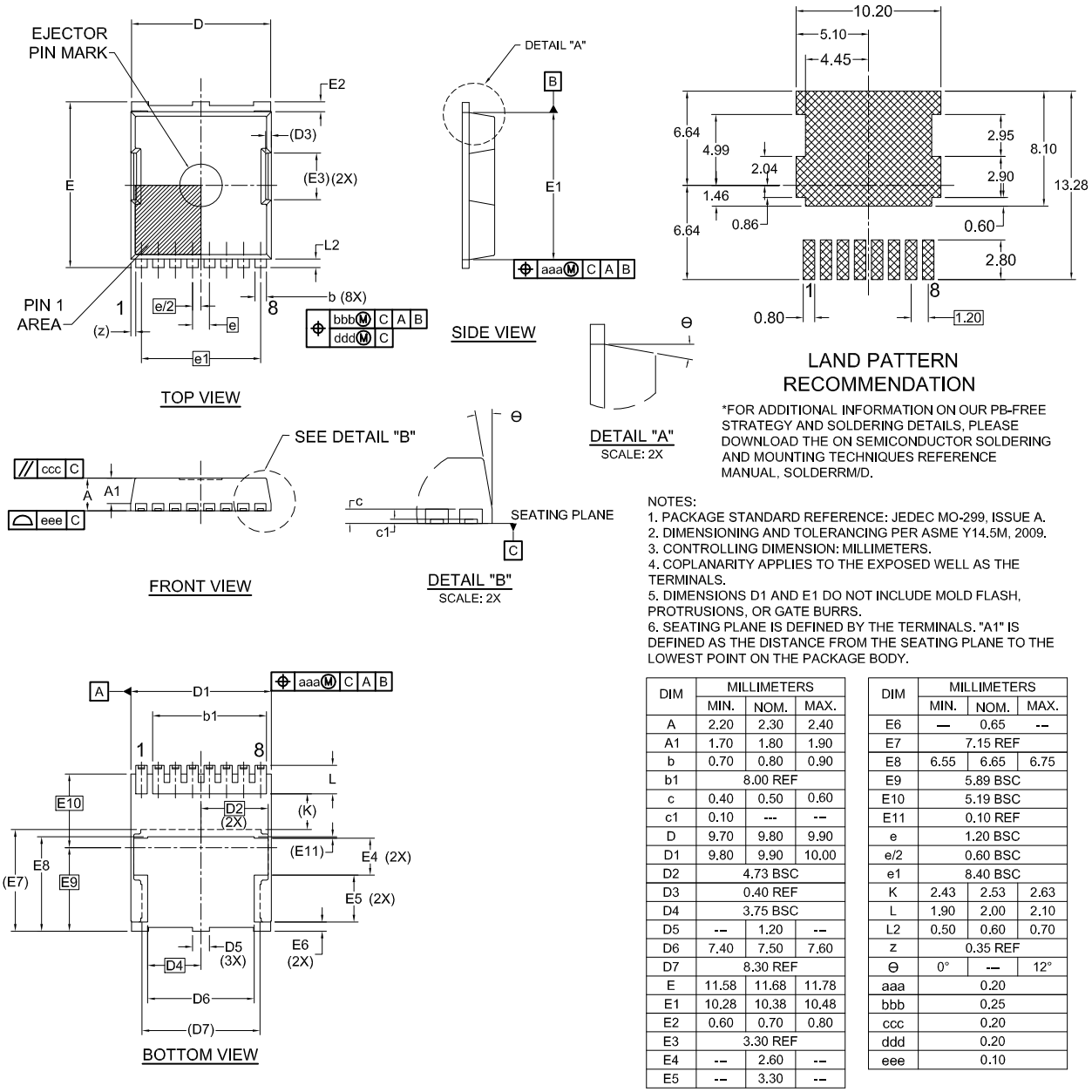


Figure 16. Transient Thermal Response

PACKAGE DIMENSIONS

H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE B



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1		8.00 REF	
c	0.40	0.50	0.60
c1	0.10	---	--
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2		4.73 BSC	
D3		0.40 REF	
D4		3.75 BSC	
D5	--	1.20	--
D6	7.40	7.50	7.60
D7		8.30 REF	
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3		3.30 REF	
E4	--	2.60	--
E5	--	3.30	--

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	—	0.65	--
E7		7.15 REF	
E8	6.55	6.65	6.75
E9		5.89 BSC	
E10		5.19 BSC	
E11		0.10 REF	
e		1.20 BSC	
e/2		0.60 BSC	
e1		8.40 BSC	
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z		0.35 REF	
Θ	0°	---	12°
aaa		0.20	
bbb		0.25	
ccc		0.20	
ddd		0.20	
eee		0.10	

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