

# Enhancement Mode Gallium Nitride (GaN) HEMT

700 V, 132 mΩ, 12 A, PDSO-E3 (DPAK)

## Preliminary Document NTD170N70GN1

### Features

- Low  $R_{DS(ON)}$  to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM- $Q_G = 280 \text{ nC}^* \text{ m}\Omega$
- Small Footprint for High Density PCB Design
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Typical Applications

- High Density Power Modules
- High Frequency AC-DC and DC-DC Converters
- High Performance PSU for Consumer and Industrial
- Resonant Conversion

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	700	V
Drain-to-Source Transient Voltage, $t_p < 200 \mu\text{s}$	$V_{DS(TRAN)}$	800	V
Pulsed Drain-to-Source Voltage, $T_J = 25^\circ\text{C}$ ( $t_{TOTAL} < 10\text{h}$ ) / $T_J = 125^\circ\text{C}$ ( $t_{TOTAL} < 1\text{h}$ )	$V_{DS(PULSE)}$	750	V
Gate-to-Source Voltage	$V_{GS}$	-6 to 7	V
Gate-to-Source Transient Voltage, $t_p = 50 \text{ ns}$ , $f_p = 100 \text{ kHz}$ , Open Drain	$V_{GS(PULSE)}$	-20 to 10	V
Continuous Drain Current, $T_{CASE} = 25^\circ\text{C}$	$I_{DS}$	12	A
Pulsed Drain Current, $t_p < 10 \mu\text{s}$ , $T_C = 25^\circ\text{C}$ , $T_C = 125^\circ\text{C}$	$I_{DS(PULSE)}$	24 13	A
Power Dissipation, $V_{GS} = 6 \text{ V}$ , $T_{CASE} = 25^\circ\text{C}$	$P_{TOT}$	64	W
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 to 150	$^\circ\text{C}$

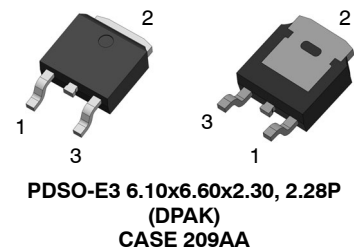
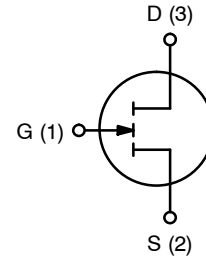
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

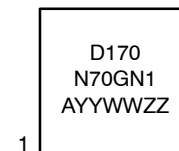
Parameter	Symbol	Value	Unit
Junction-to-Case	$R_{\theta JC}$	1.94	$^\circ\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	55.5	$^\circ\text{C}/\text{W}$
Maximum Soldering Temperature (MSL3)	$T_{SLD}$	260	$^\circ\text{C}$

1. Device on 1 in<sup>2</sup>, 2 oz copper pad on single layer FR-4 PCB

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
700 V	132 mΩ	12 A



### MARKING DIAGRAM



D170N70GN1 = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZ = Assembly Lot Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTD170N70GN1TXG	PDSO-E3 (DPAK)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	700			V
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}$		0.5	28	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 700\text{ V}, T_J = 125\text{ }^\circ\text{C}$		5.3		
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}$		26		$\mu\text{A}$

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_{DS} = 0.5\text{ A}$		132	170	m $\Omega$
		$V_{GS} = 6\text{ V}, I_{DS} = 4\text{ A}$		132		
		$V_{GS} = 6\text{ V}, I_{DS} = 4\text{ A}, T_J = 125\text{ }^\circ\text{C}$		254		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_{DS} = 10.7\text{ mA}, T_J = 25\text{ }^\circ\text{C}$	1.2	1.6	2.5	V
		$V_{DS} = V_{GS}, I_{DS} = 10.7\text{ mA}, T_J = 125\text{ }^\circ\text{C}$		1.5		

### DYNAMIC CHARACTERISTICS

Input Capacitance	$C_{ISS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ kHz}$		78		pF
Output Capacitance	$C_{OSS}$			27		
Reverse Transfer Capacitance	$C_{RSS}$			0.3		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		38.6		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			51.1		
Output Charge	$Q_{OSS}$			20.4		nC
Output Capacitance Stored Energy	$E_{OSS}$			3.1		$\mu\text{J}$
Gate Resistance	$R_G$	$f = 5\text{ MHz}$		11		$\Omega$
Gate Charge	$Q_G$	$V_{DS} = 400\text{ V}, I_{DS} = 4\text{ A}, V_{GS} = 0/6\text{ V}$		2.1		nC
Gate-to-Source Charge	$Q_{GS}$			0.2		
Gate-to-Drain Charge	$Q_{GD}$			0.8		
Gate Plateau Voltage	$V_{PLAT}$			2.1		

### REVERSE CONDUCTION CHARACTERISTICS

Source-to-Drain Reverse Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_{SD} = 4\text{ A}$		2.4		V
Pulsed Reverse Current	$I_{SD(PULSE)}$	$V_{GS} = 6\text{ V}, t_{PULSE} = 10\text{ }\mu\text{s}$			24	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)

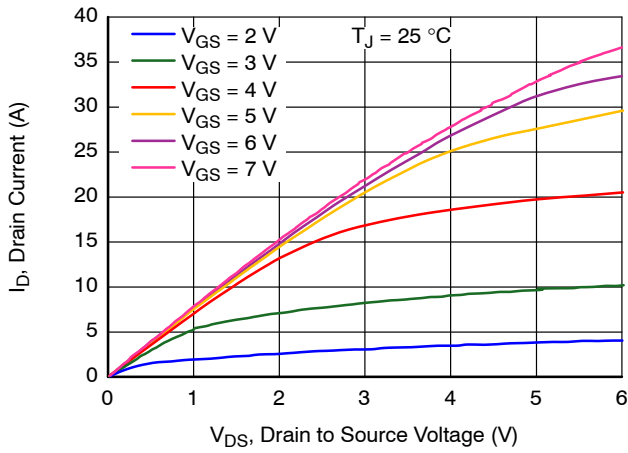


Figure 1. Output Characteristics at  $T_J = 25\text{ }^\circ\text{C}$

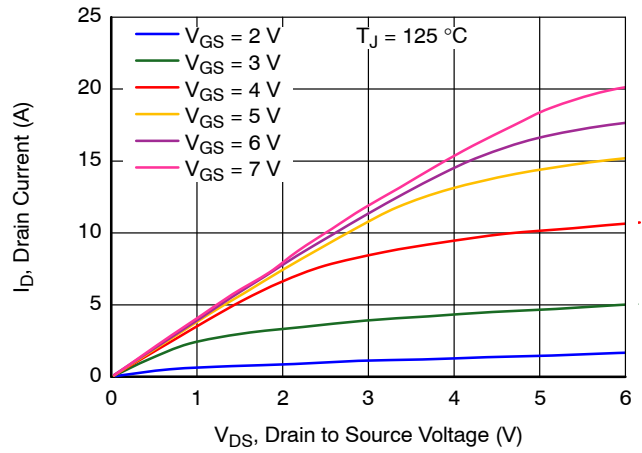


Figure 2. Output Characteristics at  $T_J = 125\text{ }^\circ\text{C}$

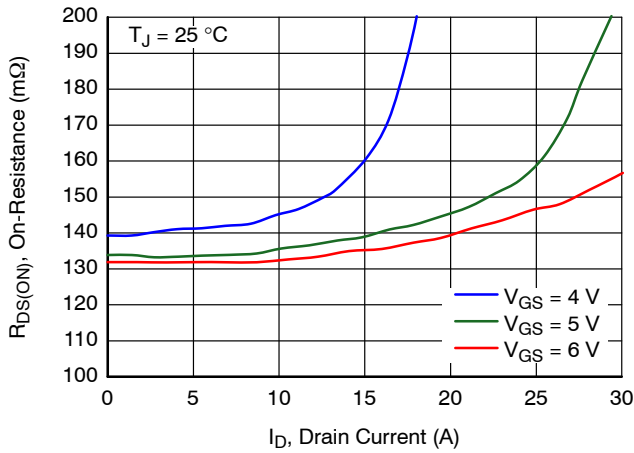


Figure 3. On-Resistance vs. Drain Current at  $T_J = 25\text{ }^\circ\text{C}$

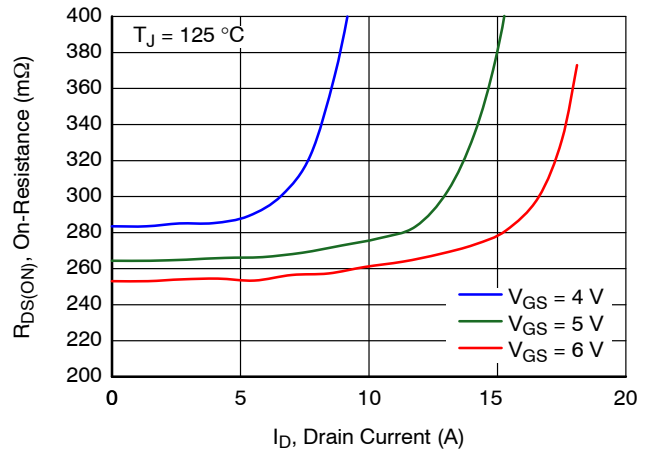


Figure 4. On-Resistance vs. Drain Current at  $T_J = 125\text{ }^\circ\text{C}$

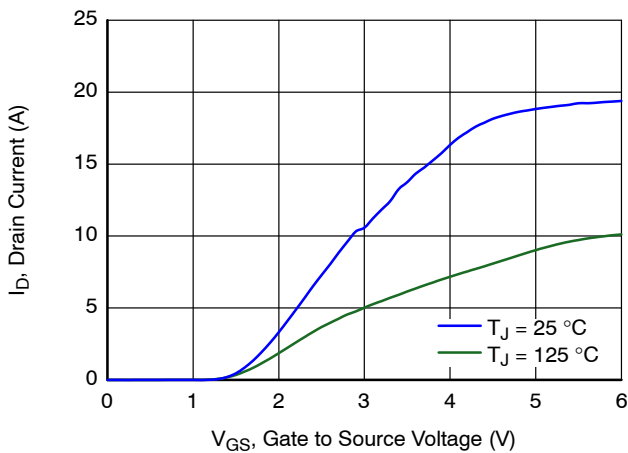


Figure 5. Transfer Characteristics at  $V_{DS} = 3\text{ V}$

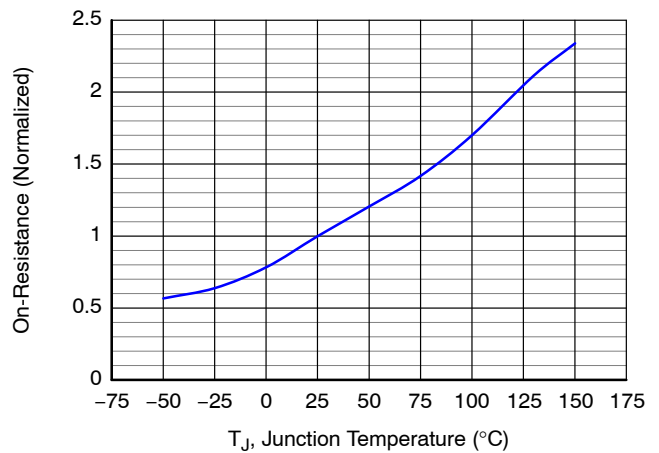
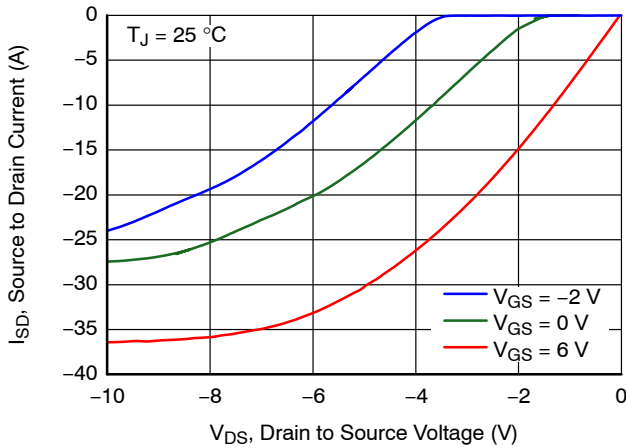


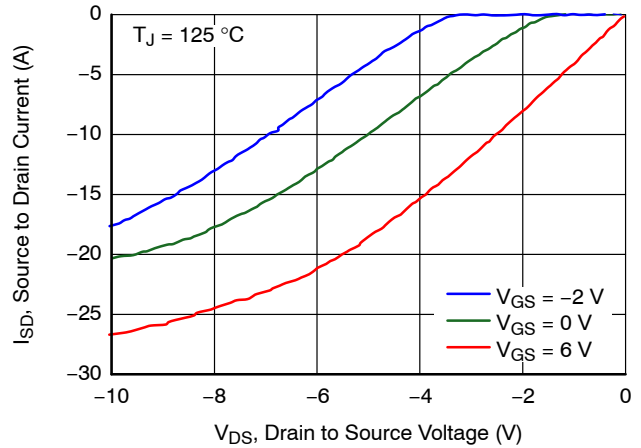
Figure 6. Normalized On-Resistance vs. Temperature at  $V_{GS} = 6\text{ V}$

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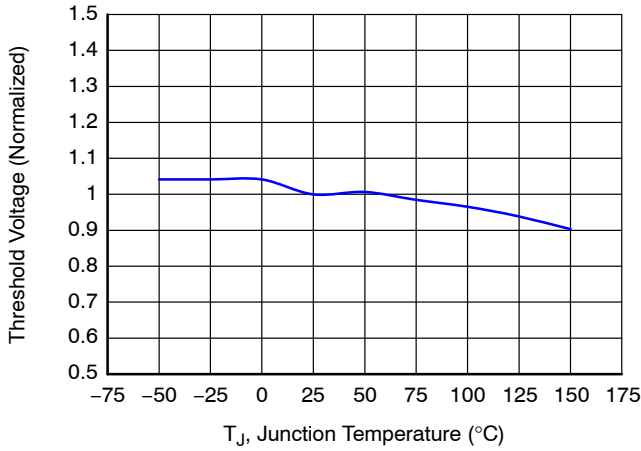
## TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) (CONTINUED)



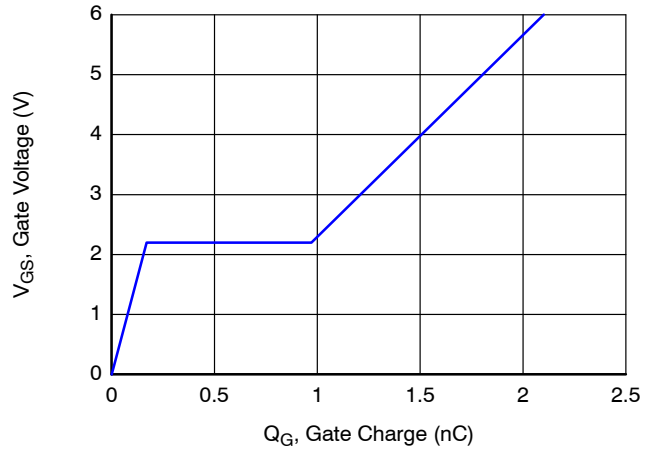
**Figure 7. Reverse Conduction Characteristics at  $T_J = 25\text{ }^\circ\text{C}$**



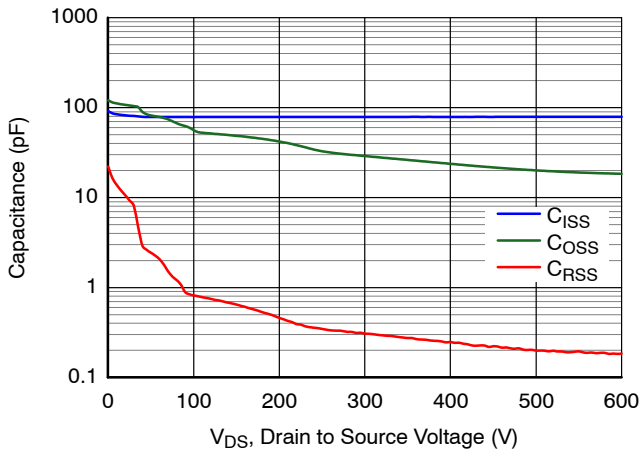
**Figure 8. Reverse Conduction Characteristics at  $T_J = 125\text{ }^\circ\text{C}$**



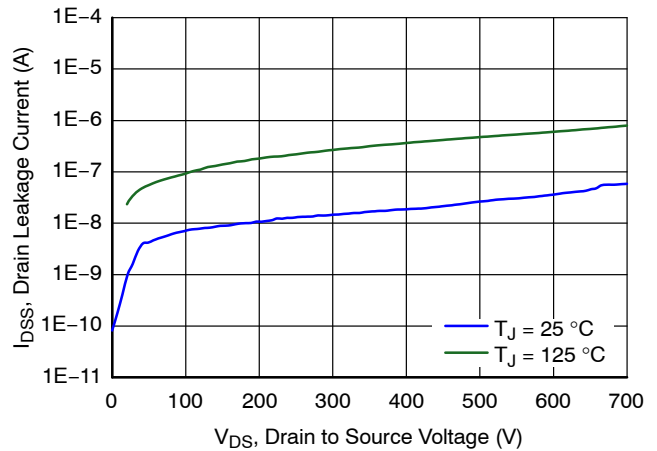
**Figure 9. Normalized Threshold Voltage vs. Temperature**



**Figure 10. Gate Charge Characteristics at  $I_{DS} = 20\text{ A}$**



**Figure 11. Capacitance Characteristics**



**Figure 12. Drain Leakage Characteristics**

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## TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) (CONTINUED)

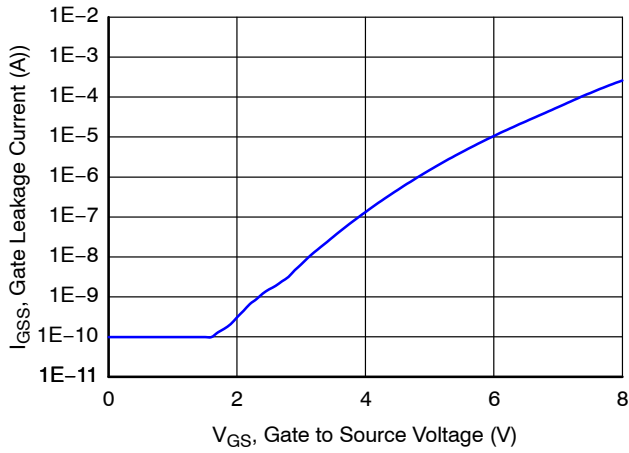


Figure 13. Gate Leakage Characteristics

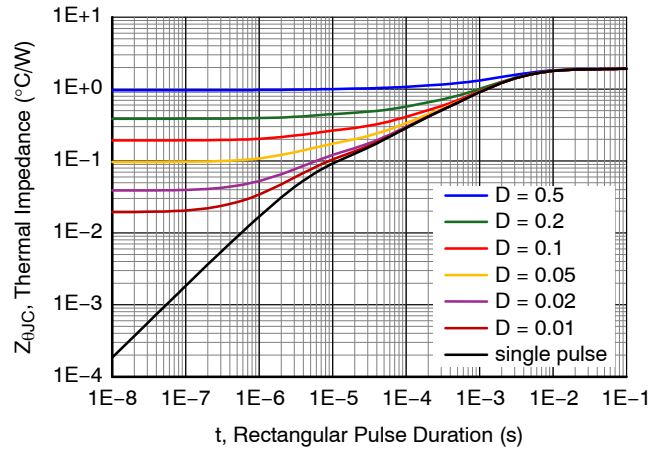


Figure 14. Transient Thermal Impedance

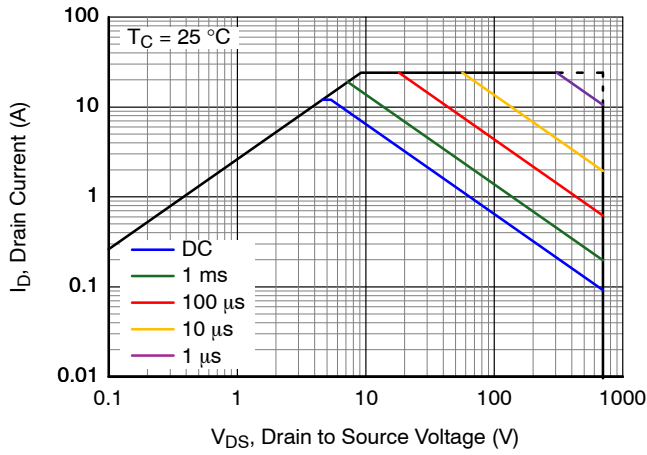


Figure 15. Safe Operating Area at  $T_C = 25\text{ }^\circ\text{C}$

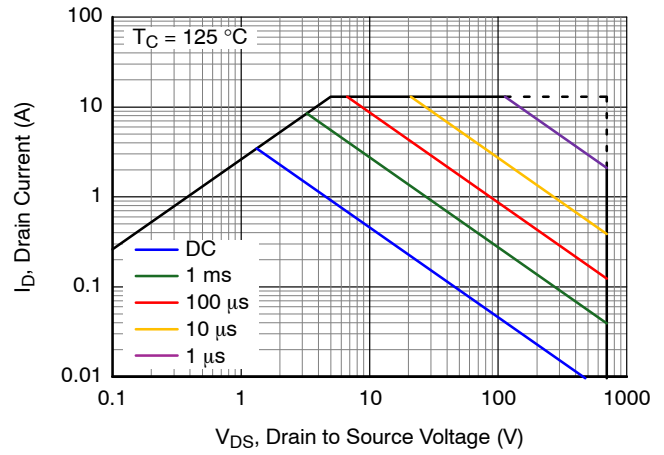


Figure 16. Safe Operating Area at  $T_C = 125\text{ }^\circ\text{C}$

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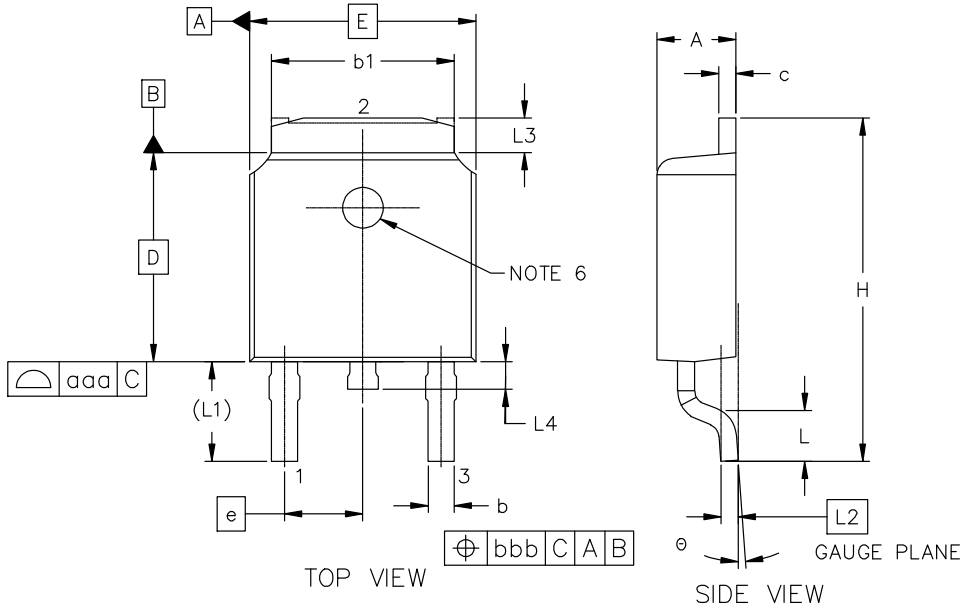
## REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	5/29/2026
P1	Edit page 1 diagram pin labels	6/5/2026

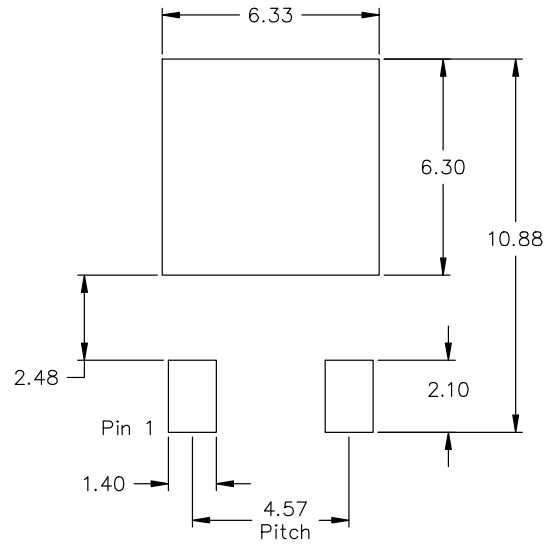
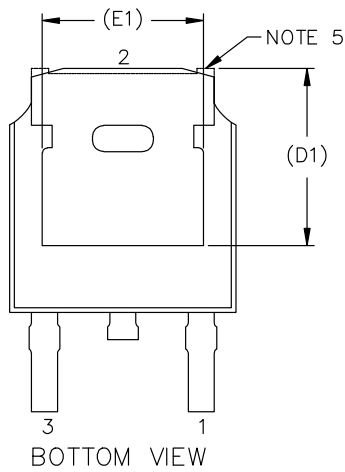
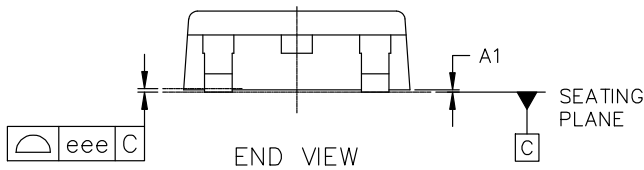
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## PACKAGE DIMENSIONS

PDSO-E3 6.10x6.60x2.30, 2.28P  
CASE 209AA  
ISSUE O



MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	0.07	0.13
b	0.63	0.76	0.90
b1	5.10	5.33	5.46
c	0.43	0.53	0.61
D	6.10 BSC		
D1	5.30 REF		
E	6.60 BSC		
E1	4.83 REF		
e	2.286 BSC		
H	9.40	9.95	10.50
L	1.38	1.50	1.75
L1	2.90 REF		
L2	0.50 BSC		
L3	0.88	1.08	1.28
L4	0.50	0.75	1.00
θ	0°	5°	10°
TOLERANCE FORM & POSITION			
aaa	0.15		
bbb	0.20		
eee	0.10		



### NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. PACKAGE OUTLINE EXCLUSIVE OF METAL BURR DIMENSIONS.
5. SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
6. MOLD EJECTION PIN MARK IS OPTIONAL.

### RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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