

NTD5867NL

MOSFET – Power, N-Channel 60 V, 20 A, 39 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|------------------------|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DS} | 60 | V | |
| Gate-to-Source Voltage – Continuous | V_{GS} | ± 20 | V | |
| Gate-to-Source Voltage – Non-Repetitive ($t_p < 10 \mu\text{s}$) | V_{GS} | ± 30 | V | |
| Continuous Drain Current ($R_{\theta JC}$) | Steady State | $T_C = 25^\circ\text{C}$ | 20 | A |
| | | $T_C = 100^\circ\text{C}$ | 13 | |
| Power Dissipation ($R_{\theta JC}$) | | $T_C = 25^\circ\text{C}$ | 36 | W |
| Pulsed Drain Current | $t_p = 10 \mu\text{s}$ | I_{DM} | 76 | A |
| Operating Junction and Storage Temperature | T_J, T_{stg} | -55 to 150 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 20 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega, I_{L(pk)} = 19 \text{ A}, L = 0.1 \text{ mH}, T_J = 25^\circ\text{C}$) | E_{AS} | 18 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|--------------------|
| Junction-to-Case (Drain) | $R_{\theta JC}$ | 3.5 | $^\circ\text{C/W}$ |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 45 | |

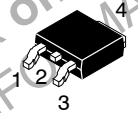
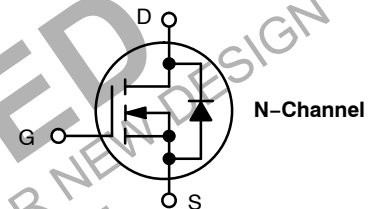
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).



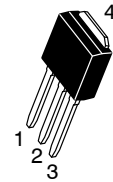
ON Semiconductor®

<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | I_D MAX |
|---------------|------------------|-----------|
| 60 V | 39 mΩ @ 10 V | 20 A |
| | 50 mΩ @ 4.5 V | 18 A |

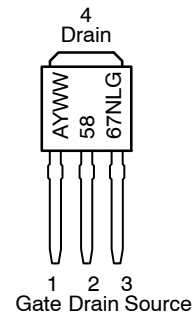
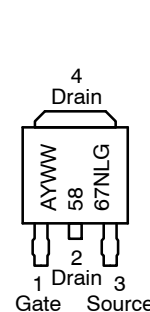


DPAK
CASE 369AA
(Surface Mount)
STYLE 2



IPAK
CASE 369D
(Straight Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5867NL = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NTD5867NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------------------|--|------------------------|-----|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 60 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 1.0 | μA |
| | | | T _J = 125°C | | 100 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | ±100 | nA |

ON CHARACTERISTICS (Note 2)

| | | | | | | |
|--|-------------------------------------|---|-----|-----|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 1.5 | 1.8 | 2.5 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | 5.2 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 10 A | | 26 | 39 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 10 A | | 33 | 50 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 10 A | | 8.0 | | S |

CHARGES, CAPACITANCES AND GATE RESISTANCES

| | | | | | | |
|------------------------------|---------------------|---|--|-----|--|----|
| Input Capacitance | C _{iss} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | | 675 | | pF |
| Output Capacitance | C _{oss} | | | 68 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 47 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V, I _D = 20 A | | 15 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 1.0 | | |
| Gate-to-Source Charge | Q _{GS} | | | 2.2 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 4.3 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 20 A | | 7.6 | | nC |
| Gate Resistance | R _G | | | 1.3 | | Ω |

SWITCHING CHARACTERISTICS (Note 3)

| | | | | | | |
|---------------------|---------------------|--|--|------|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 10 V, V _{DD} = 48 V, I _D = 20 A, R _G = 2.5 Ω | | 6.5 | | ns |
| Rise Time | t _r | | | 12.6 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 18.2 | | |
| Fall Time | t _f | | | 2.4 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-------------------------|-----------------|---|------------------------|------|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 10 A | T _J = 25°C | 0.87 | 1.2 | V |
| | | | T _J = 100°C | 0.78 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 20 A | | 17 | | ns |
| Charge Time | t _a | | | 13 | | |
| Discharge Time | t _b | | | 4.0 | | |
| Reverse Recovery Charge | Q _{RR} | | | | 12 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

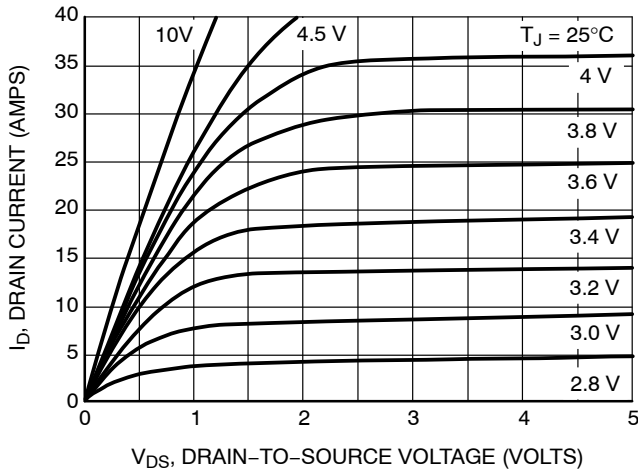


Figure 1. On-Region Characteristics

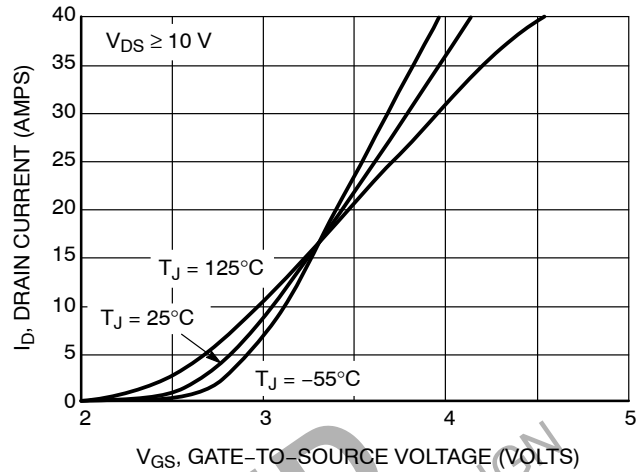


Figure 2. Transfer Characteristics

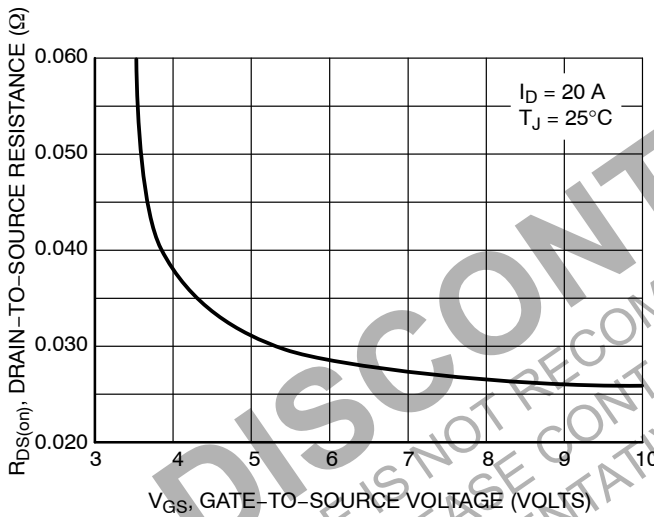


Figure 3. On-Resistance vs. Gate-to-Source Voltage

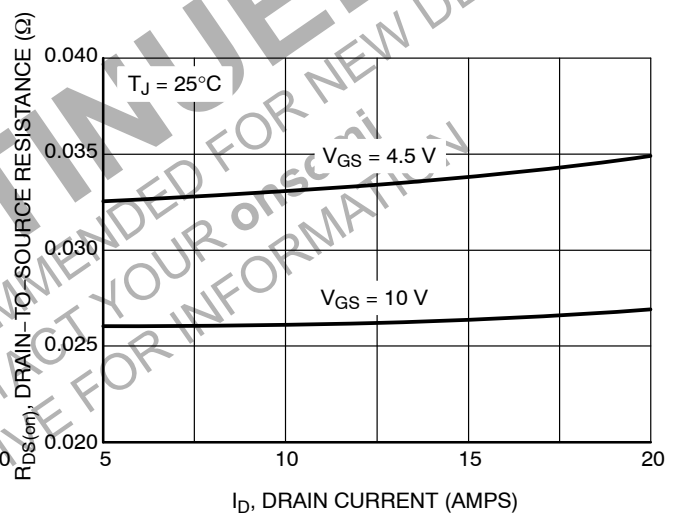


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

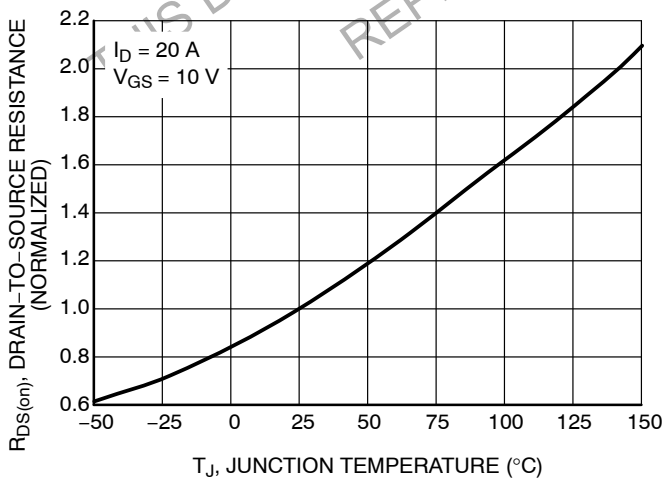


Figure 5. On-Resistance Variation with Temperature

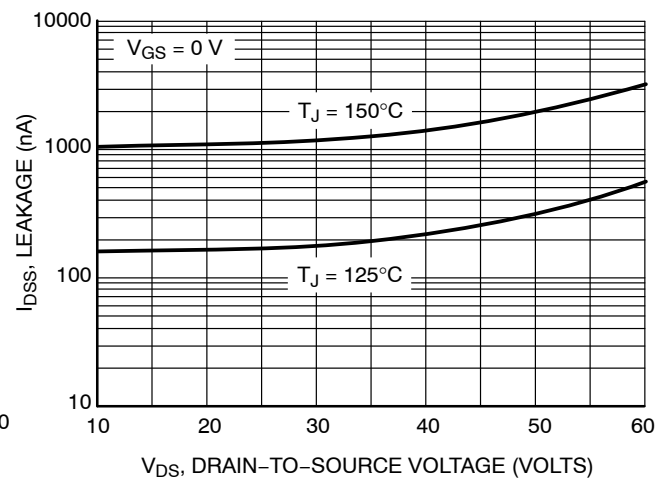


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

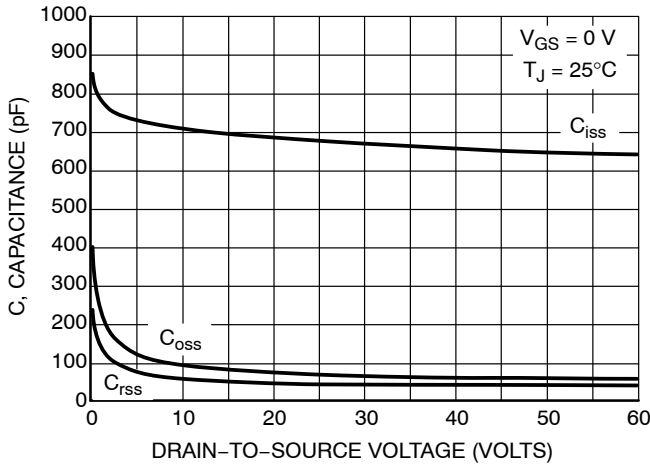


Figure 7. Capacitance Variation

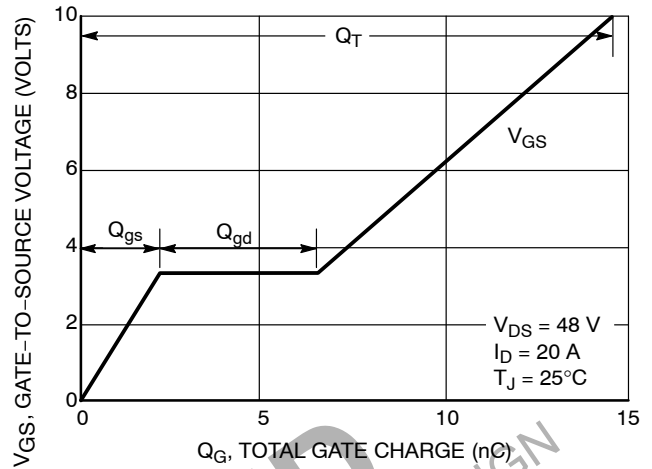


Figure 8. Gate-to-Source Voltage vs. Total Charge

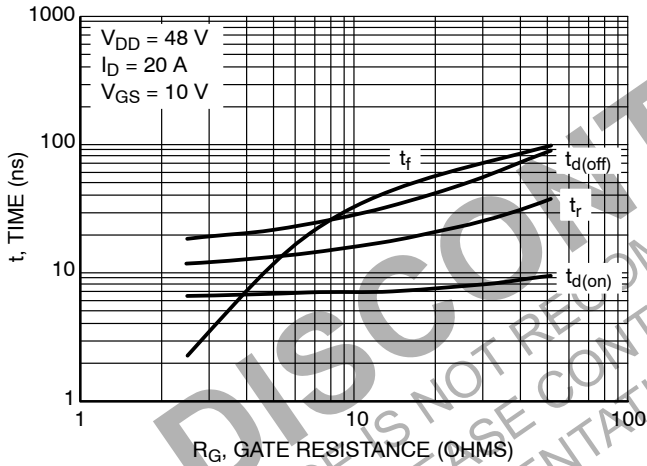


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

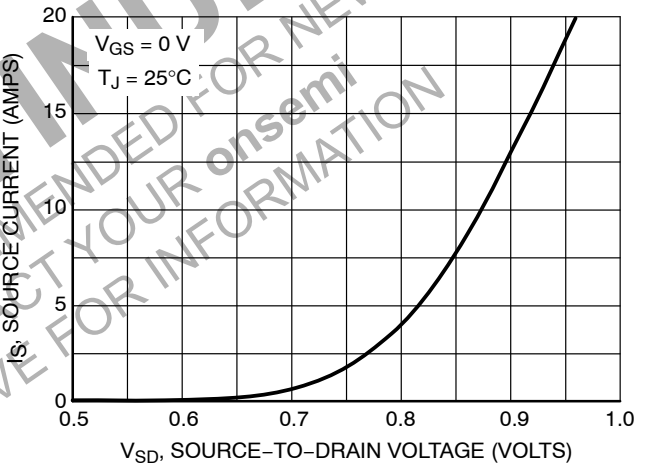


Figure 10. Diode Forward Voltage vs. Current

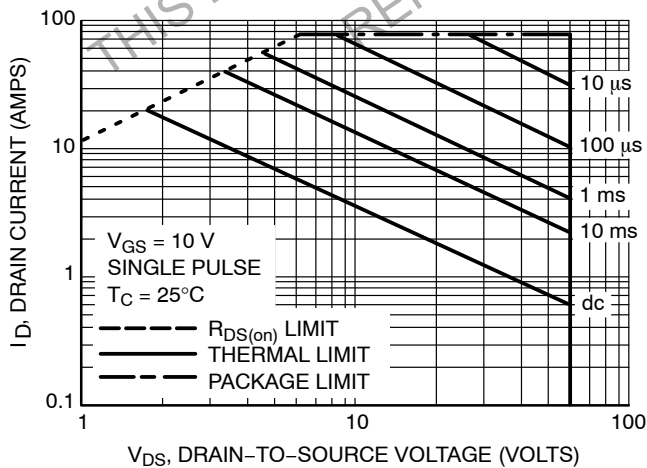


Figure 11. Maximum Rated Forward Biased Safe Operating Area

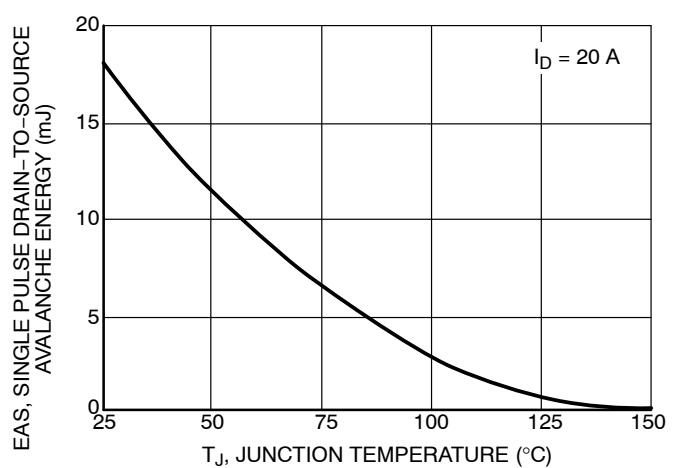


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD5867NL

TYPICAL PERFORMANCE CURVES

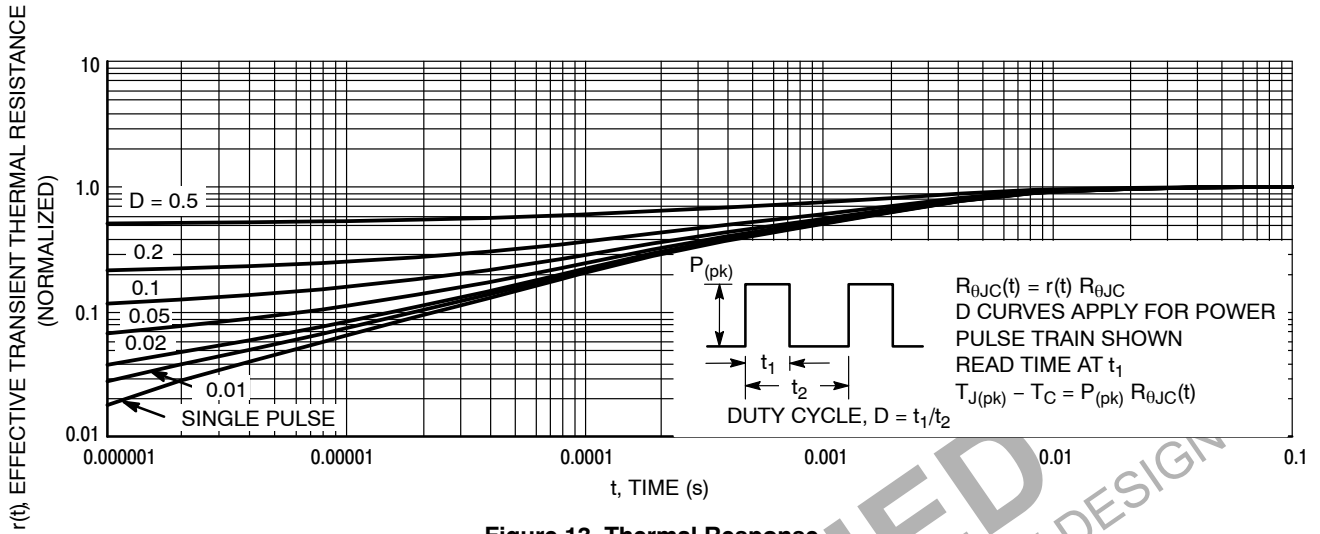
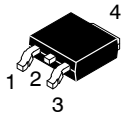


Figure 13. Thermal Response

ORDERING INFORMATION

| Order Number | Package | Shipping [†] |
|--------------|-----------------------------------|-----------------------|
| NTD5867NL-1G | IPAK (Straight Lead) (Pb-Free) | 75 Units / Rail |
| NTD5867NLT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



DPAK-3 6.10x6.54x2.28, 2.29P
CASE 369AA
ISSUE C

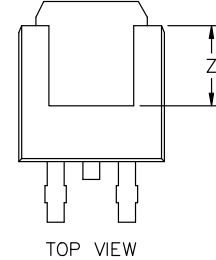
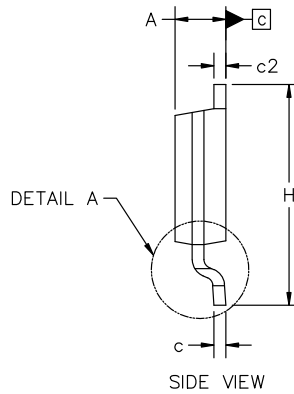
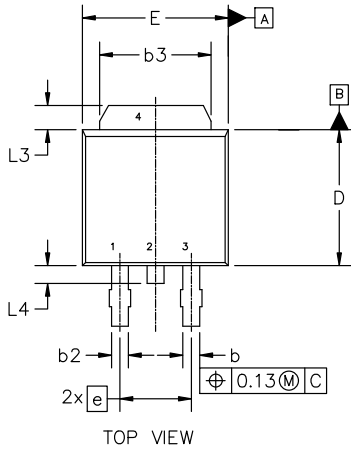
DATE 14 MAY 2026

SCALE 1:1

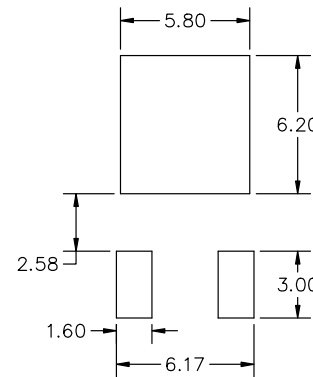
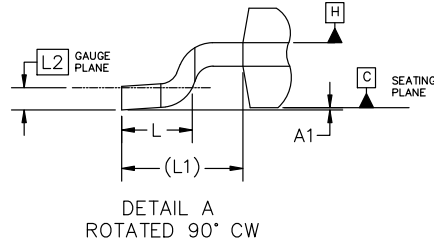
NOTES

1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H

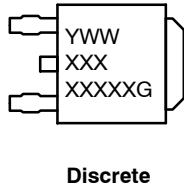
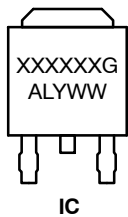
| DIM | MILLIMETERS | | |
|-----|-------------|------|-------|
| | MIN. | NOM. | MAX. |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | --- | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.76 | 0.95 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.74 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | --- | 1.27 |
| L4 | --- | --- | 1.01 |
| Z | 3.93 | --- | --- |



RECOMMENDED MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

| | | |
|-------------------------|-------------------------------------|--|
| DOCUMENT NUMBER: | 98AON13126D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK-3 6.10x6.54x2.28, 2.29P | PAGE 1 OF 1 |

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