

# NTGS3455T1

## MOSFET – P-Channel, TSOP-6

**-3.5 A, -30 V**

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP-6 Surface Mount Package
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-30	Volts
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20.0$	Volts
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_d$	2.0	Watts
Drain Current	$I_D$	-3.5	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	$I_{DM}$	-20	Amps
– Pulsed Drain Current ( $T_p < 10 \mu\text{s}$ )	$P_d$	1.0	Watts
Maximum Operating Power Dissipation	$I_D$	-2.5	Amps
Maximum Operating Drain Current			
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	128	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_d$	1.0	Watts
Drain Current	$I_D$	-2.5	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	$I_{DM}$	-14	Amps
– Pulsed Drain Current ( $T_p < 10 \mu\text{s}$ )	$P_d$	0.5	Watts
Maximum Operating Power Dissipation	$I_D$	-1.75	Amps
Maximum Operating Drain Current			
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

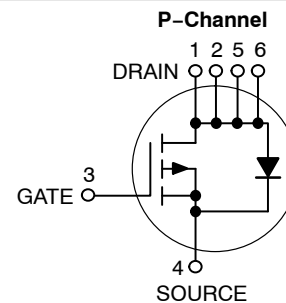
1. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. Cu. 0.06" thick single sided),  $t < 5.0$  seconds.
2. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. Cu. 0.06" thick single sided), operating to steady state.



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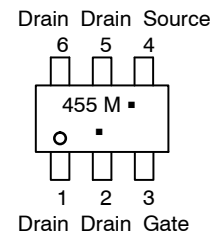
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ Max
-30 V	100 m $\Omega$ @ -10 V	-3.5 A



### MARKING DIAGRAM & PIN ASSIGNMENT



**TSOP-6  
CASE 318G  
STYLE 1**



- 455 = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTGS3455T1	TSOP-6	3000 Tape & Reel
NTGS3455T1G	TSOP-6 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTGS3455T1

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted) (Notes 3 & 4)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -10 μA)	V <sub>(BR)DSS</sub>	-30	-	-	Vdc
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -30 Vdc, T <sub>J</sub> = 25°C) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -30 Vdc, T <sub>J</sub> = 70°C)	I <sub>DSS</sub>	-	-	-1.0 -5.0	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = -20.0 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc
Gate-Body Leakage Current (V <sub>GS</sub> = +20.0 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc)	V <sub>GS(th)</sub>	-1.0	-1.87	-3.0	Vdc
Static Drain-Source On-State Resistance (V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -3.5 Adc) (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -2.7 Adc)	R <sub>DS(on)</sub>	-	0.094 0.144	0.100 0.170	Ω
Forward Transconductance (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -3.5 Adc)	g <sub>FS</sub>	-	6.0	-	mhos

### DYNAMIC CHARACTERISTICS

Total Gate Charge	(V <sub>DS</sub> = -15 Vdc, V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -3.5 Adc)	Q <sub>tot</sub>	-	9.0	13	nC
Gate-Source Charge		Q <sub>gs</sub>	-	2.5	-	
Gate-Drain Charge		Q <sub>gd</sub>	-	2.0	-	
Input Capacitance	(V <sub>DS</sub> = -5.0 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	480	-	pF
Output Capacitance		C <sub>oss</sub>	-	220	-	
Reverse Transfer Capacitance		C <sub>rss</sub>	-	60	-	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	(V <sub>DD</sub> = -20 Vdc, I <sub>D</sub> = -1.0 Adc, V <sub>GS</sub> = -10 Vdc, R <sub>g</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	10	20	ns
Rise Time		t <sub>r</sub>	-	15	30	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	20	35	
Fall Time		t <sub>f</sub>	-	10	20	
Reverse Recovery Time	(I <sub>S</sub> = -1.7 Adc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	30	-	ns

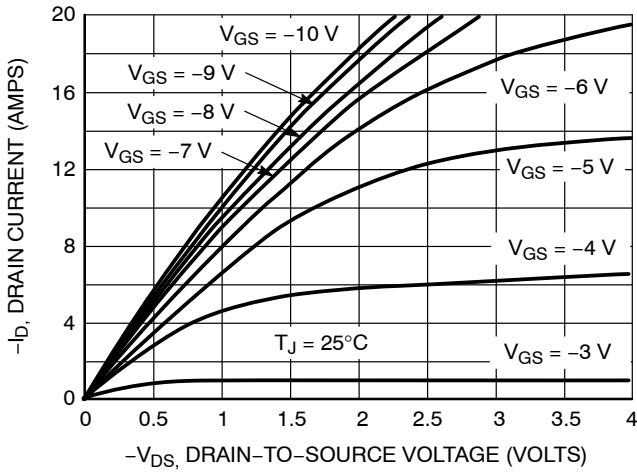
### BODY-DRAIN DIODE RATINGS

Diode Forward On-Voltage	(I <sub>S</sub> = -1.7 Adc, V <sub>GS</sub> = 0 Vdc)	V <sub>SD</sub>	-	-0.90	-1.2	Vdc
Diode Forward On-Voltage	(I <sub>S</sub> = -3.5 Adc, V <sub>GS</sub> = 0 Vdc)	V <sub>SD</sub>	-	-1.0	-	Vdc

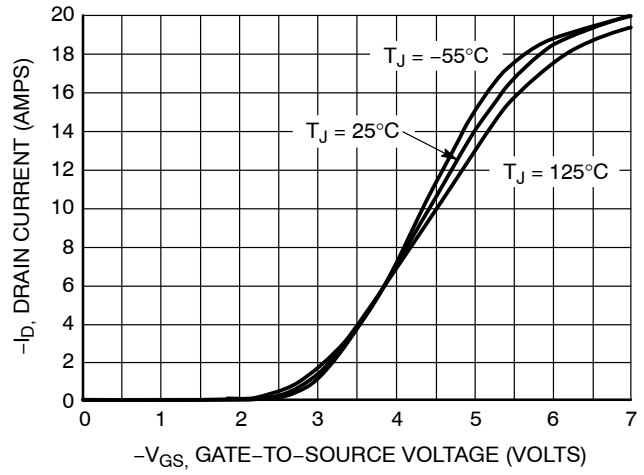
3. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.

4. Class 1 ESD rated - Handling precautions to protect against electrostatic discharge are mandatory.

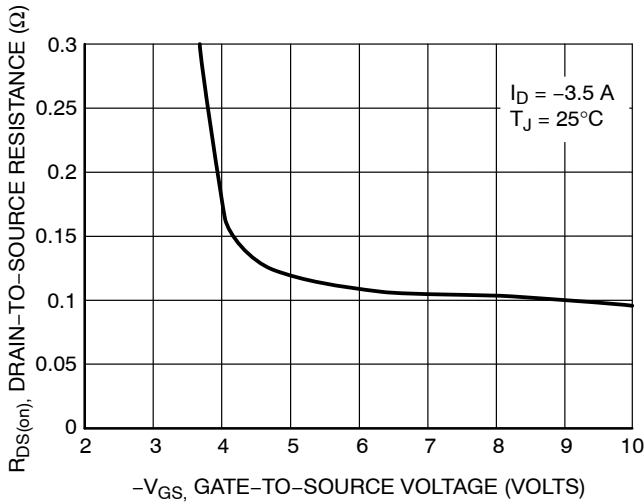
# NTGS3455T1



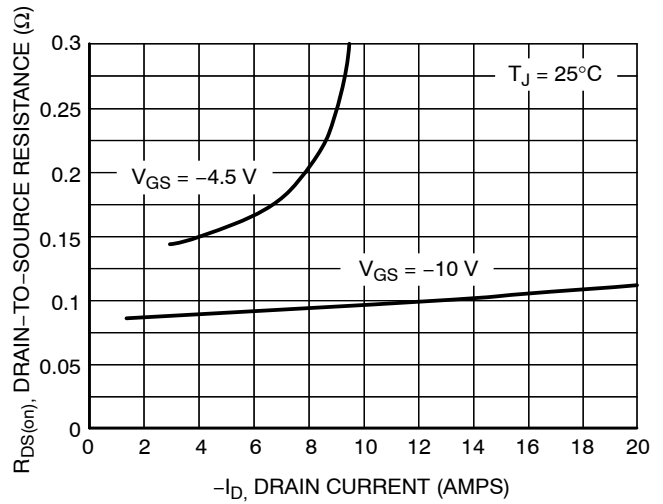
**Figure 1. On-Region Characteristics**



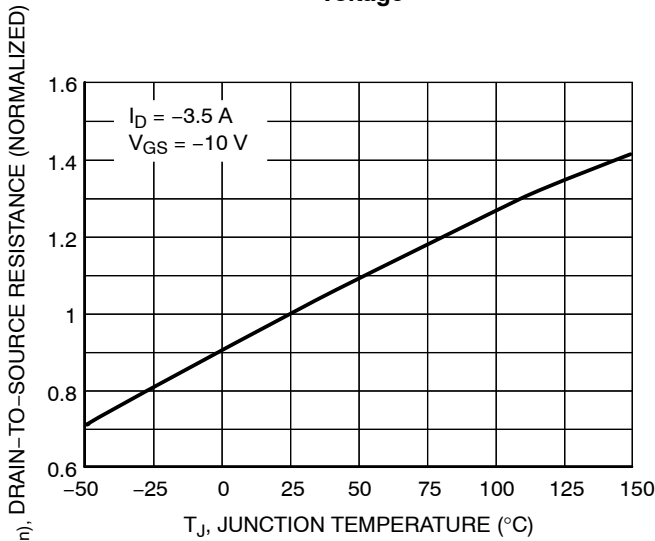
**Figure 2. Transfer Characteristics**



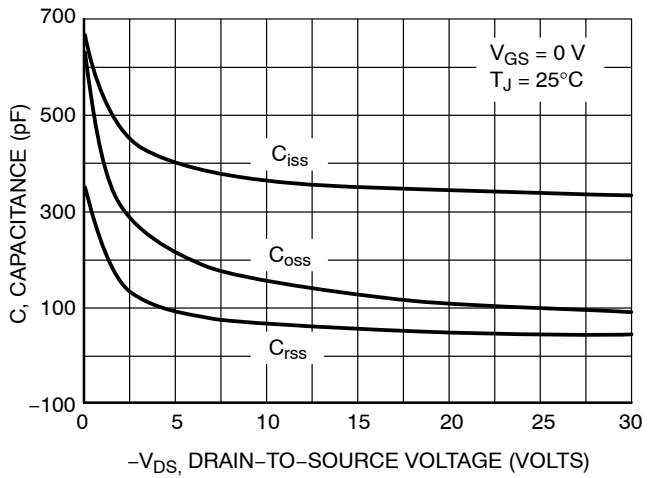
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

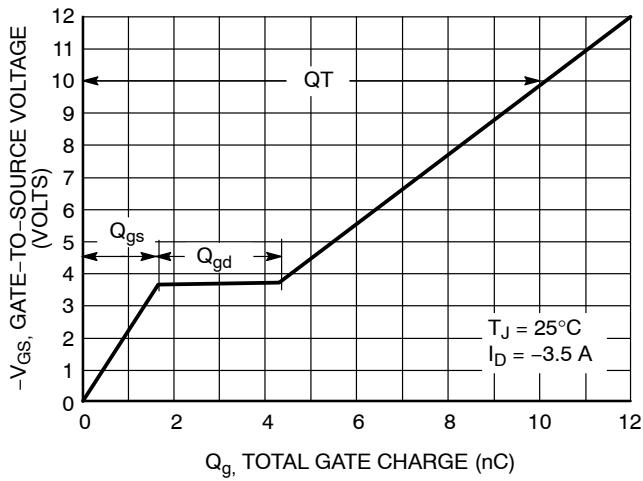


**Figure 5. On-Resistance Variation with Temperature**

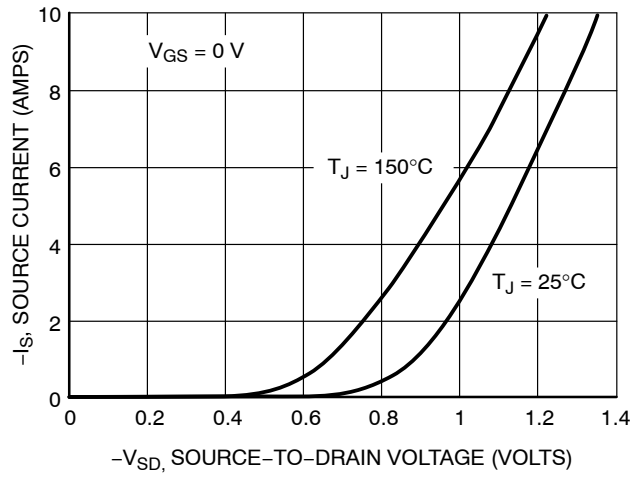


**Figure 6. Capacitance Variation**

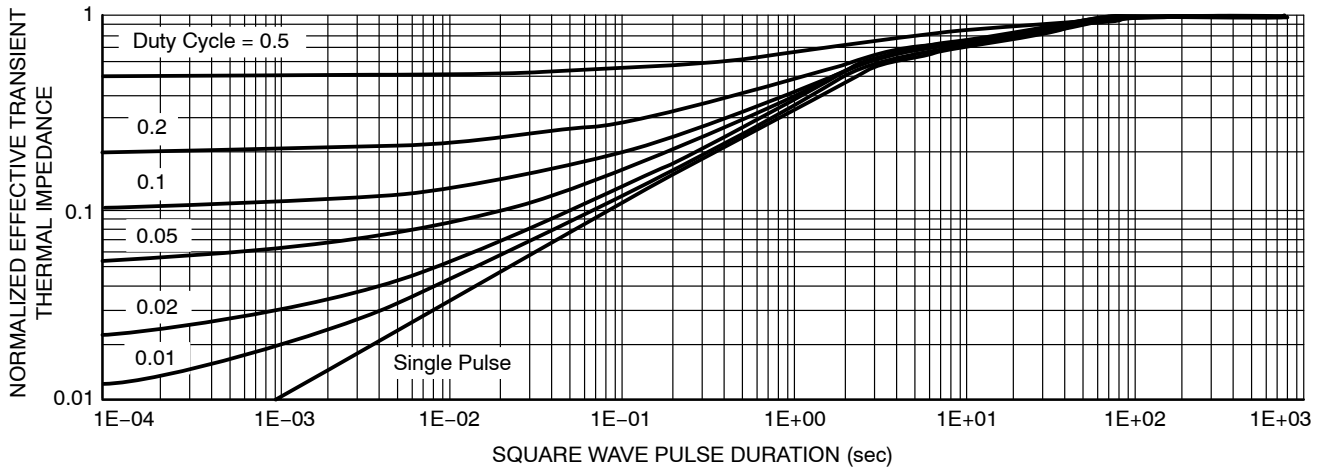
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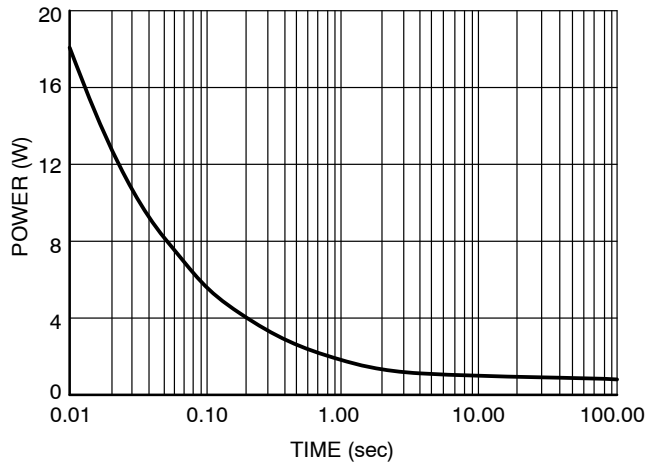
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 8. Diode Forward Voltage vs. Current**



**Figure 9. Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Figure 10. Single Pulse Power**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

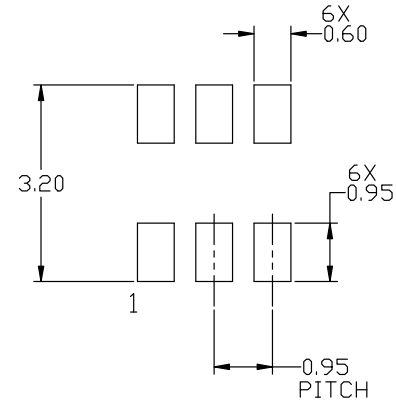
DATE 26 FEB 2024



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



**RECOMMENDED MOUNTING FOOTPRINT**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



TSOP-6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |   |  |
|--|--|---|---|---|--|
| <p>STYLE 1:<br/>PIN 1. DRAIN<br/>2. DRAIN<br/>3. GATE<br/>4. SOURCE<br/>5. DRAIN<br/>6. DRAIN</p>              | <p>STYLE 2:<br/>PIN 1. EMITTER 2<br/>2. BASE 1<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 2<br/>6. COLLECTOR 2</p>    | <p>STYLE 3:<br/>PIN 1. ENABLE<br/>2. N/C<br/>3. R BOOST<br/>4. Vz<br/>5. V in<br/>6. V out</p>                            | <p>STYLE 4:<br/>PIN 1. N/C<br/>2. V in<br/>3. NOT USED<br/>4. GROUND<br/>5. ENABLE<br/>6. LOAD</p>                | <p>STYLE 5:<br/>PIN 1. EMITTER 2<br/>2. BASE 2<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 1<br/>6. COLLECTOR 2</p> | <p>STYLE 6:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. EMITTER<br/>5. COLLECTOR<br/>6. COLLECTOR</p> |
| <p>STYLE 7:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. N/C<br/>5. COLLECTOR<br/>6. EMITTER</p>   | <p>STYLE 8:<br/>PIN 1. Vbus<br/>2. D(in)<br/>3. D(in)+<br/>4. D(out)+<br/>5. D(out)<br/>6. GND</p>                         | <p>STYLE 9:<br/>PIN 1. LOW VOLTAGE GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN<br/>5. DRAIN<br/>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:<br/>PIN 1. D(OUT)+<br/>2. GND<br/>3. D(OUT)-<br/>4. D(IN)-<br/>5. VBUS<br/>6. D(IN)+</p>             | <p>STYLE 11:<br/>PIN 1. SOURCE 1<br/>2. DRAIN 2<br/>3. DRAIN 2<br/>4. SOURCE 2<br/>5. GATE 1<br/>6. DRAIN 1/GATE 2</p>  | <p>STYLE 12:<br/>PIN 1. I/O<br/>2. GROUND<br/>3. I/O<br/>4. I/O<br/>5. VCC<br/>6. I/O</p>                          |
| <p>STYLE 13:<br/>PIN 1. GATE 1<br/>2. SOURCE 2<br/>3. GATE 2<br/>4. DRAIN 2<br/>5. SOURCE 1<br/>6. DRAIN 1</p> | <p>STYLE 14:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. CATHODE/DRAIN<br/>5. CATHODE/DRAIN<br/>6. CATHODE/DRAIN</p> | <p>STYLE 15:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. DRAIN<br/>5. N/C<br/>6. CATHODE</p>                        | <p>STYLE 16:<br/>PIN 1. ANODE/CATHODE<br/>2. BASE<br/>3. EMITTER<br/>4. COLLECTOR<br/>5. ANODE<br/>6. CATHODE</p> | <p>STYLE 17:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. ANODE/CATHODE<br/>4. ANODE<br/>5. CATHODE<br/>6. COLLECTOR</p>       |  |

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