NTHD5903

Power MOSFET

−20 V, −3.0 A, Dual P−Channel ChipFET™

Features

- Low $R_{DS(on)}$ for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space
- Pb−Free Package is Available

Applications

- Power Management in Portable and Battery−Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain−Source Voltage	V_{DS}	−20		V
Gate−Source Voltage	V_{GS}	±12		V
Continuous Drain Current (T_J = 150°C) (Note 1) T_A = 25°C T_A = 85°C	I_D	 ±3.0 ±2.2	 ±2.2 ±1.6	A
Pulsed Drain Current	I_{DM}	±10		A
Continuous Source Current (Diode Conduction) (Note 1)	I_S	−3.0	−2.2	A
Maximum Power Dissipation (Note 1) T_A = 25°C T_A = 85°C	P_D	 2.1 1.1	 1.1 0.6	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

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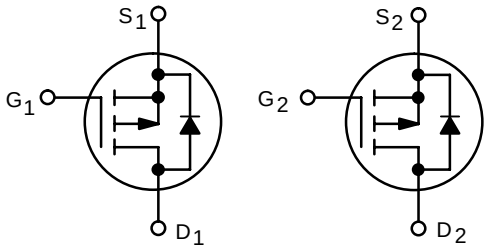
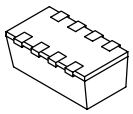
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−20 V	130 mΩ @ −4.5 V	−3.0 A
	215 mΩ @ −2.5 V	

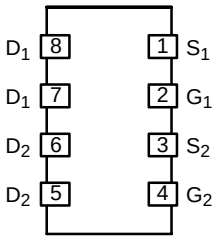


P−Channel MOSFET **P−Channel MOSFET**

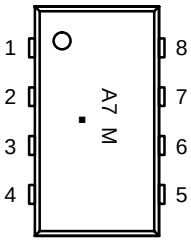


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



A7 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD5903T1	ChipFET	3000/Tape & Reel
NTHD5903T1G	ChipFET (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction−to−Ambient (Note 2) $t \leq 5$ s Steady State	$R_{\theta JA}$	 50 90	 60 110	°C/W
Maximum Junction−to−Foot (Drain) Steady State	$R_{\theta JF}$	30	40	°C/W

2. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μA	−0.6			V
Gate−Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16$ V, $V_{GS} = 0$ V			−1.0	μA
		$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 85$°C			−5.0	
On−State Drain Current (Note 3)	$I_{D(on)}$	$V_{DS} \leq -5.0$ V, $V_{GS} = -4.5$ V	−10			A
Drain−Source On−State Resistance (Note 3)	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.2$ A		0.130	0.155	Ω
		$V_{GS} = -3.6$ V, $I_D = -2.0$ A		0.150	0.180	
		$V_{GS} = -2.5$ V, $I_D = -1.7$ A		0.215	0.260	
Forward Transconductance (Note 3)	g_{fs}	$V_{DS} = -10$ V, $I_D = -2.2$ A		5.0		S
Diode Forward Voltage (Note 3)	V_{SD}	$I_S = -2.2$ A, $V_{GS} = 0$ V		−0.8	−1.2	V
Dynamic (Note 4)						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -2.2$ A		3.7	7.4	nC
Gate−Source Charge	Q_{gs}			0.8		
Gate−Drain Charge	Q_{gd}			1.3		
Turn−On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10$ Ω, $I_D \cong -1.0$ A, $V_{GEN} = -4.5$ V, $R_G = 6$ Ω		13	20	ns
Rise Time	t_r			35	55	
Turn−Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			25	40	
Source−Drain Reverse Recovery Time	t_{rr}	$I_F = -2.2$ A, di/dt = 100 A/μs		40	80	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

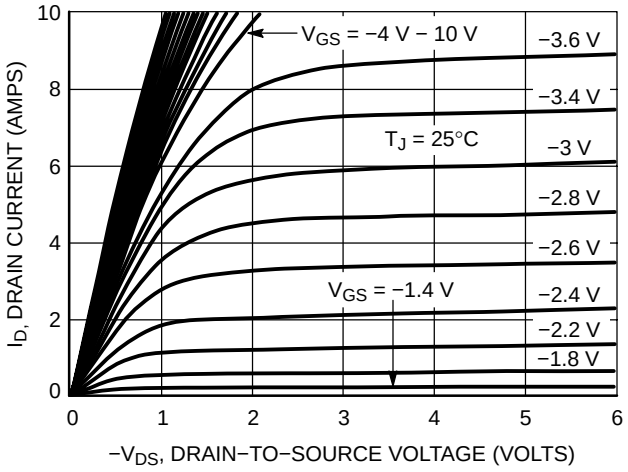


Figure 1. On−Region Characteristics

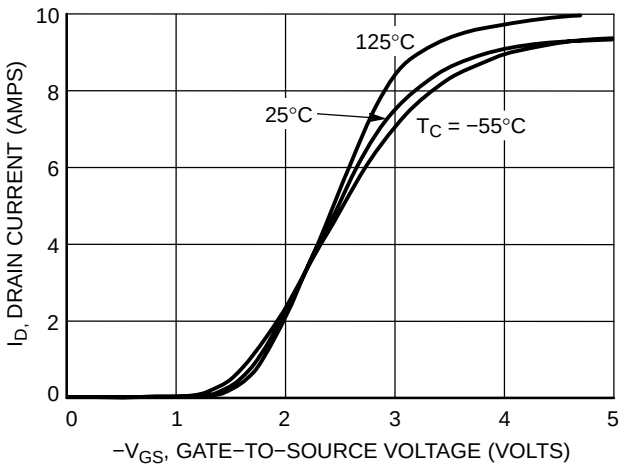


Figure 2. Transfer Characteristics

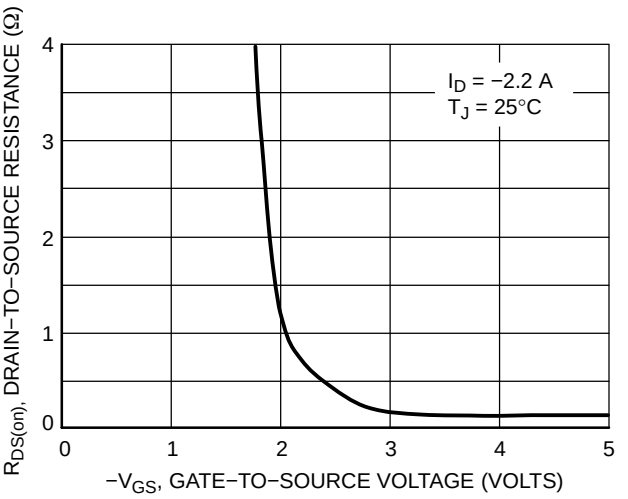


Figure 3. On−Resistance vs. Gate−to−Source Voltage

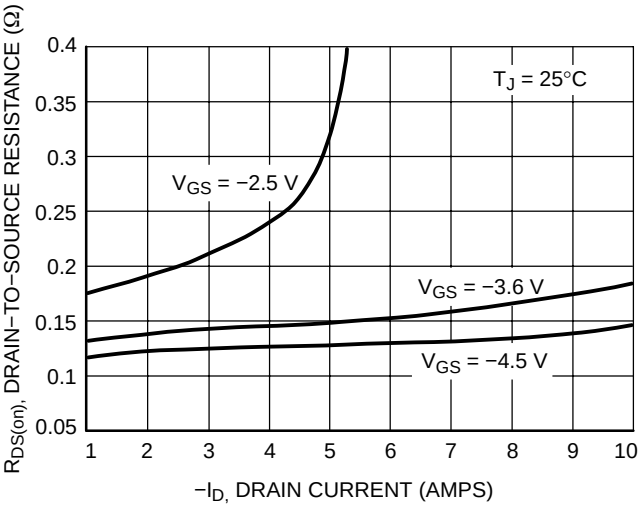


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

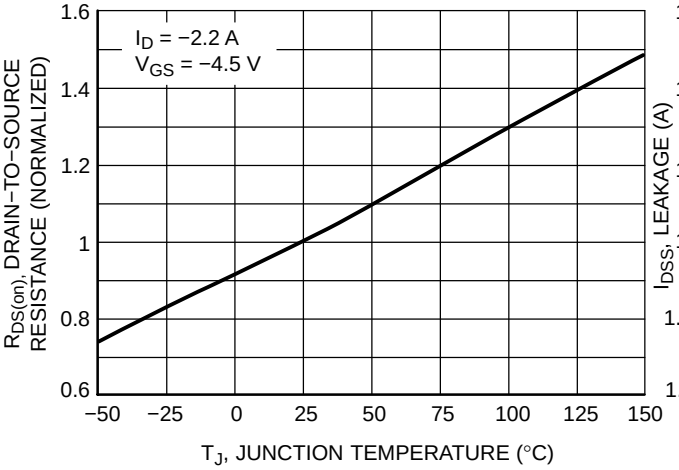


Figure 5. On−Resistance Variation with Temperature

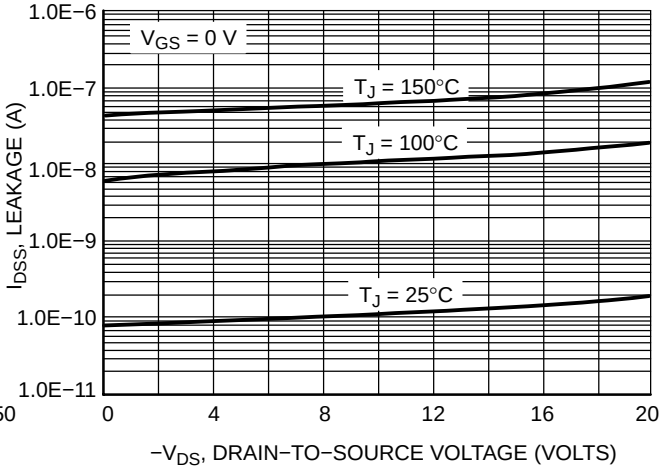


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

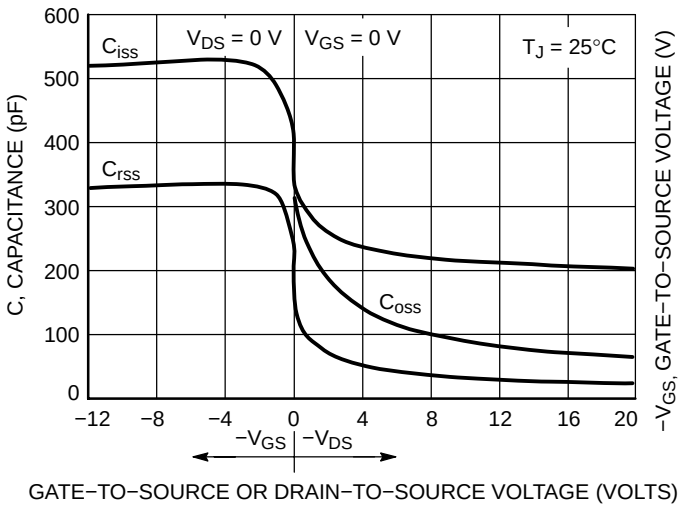


Figure 7. Capacitance Variation

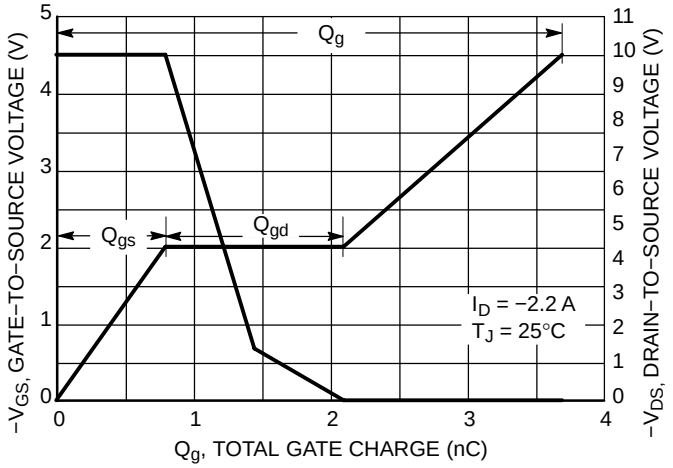


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

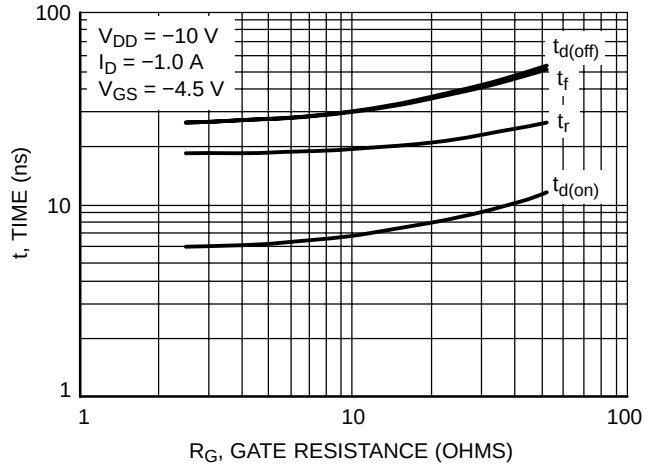


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

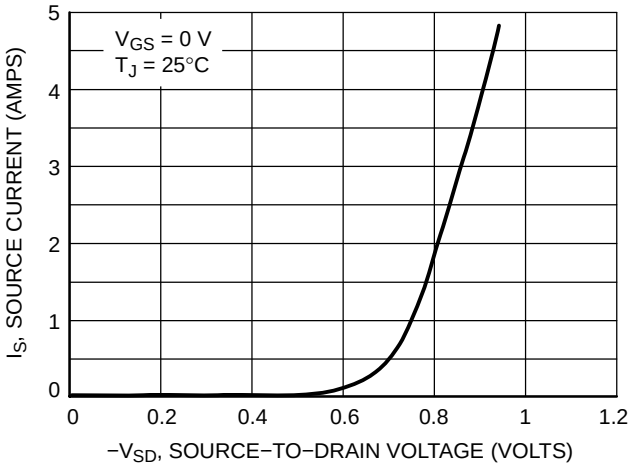


Figure 10. Diode Forward Voltage vs. Current

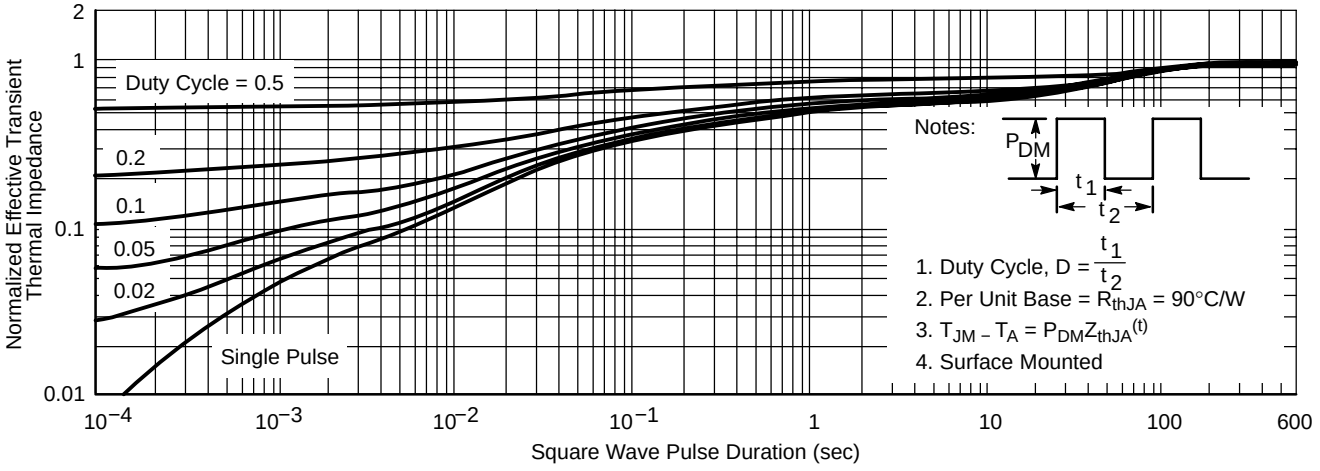


Figure 11. Normalized Thermal Transient Impedance, Junction−to−Ambient

SOLDERING FOOTPRINT*

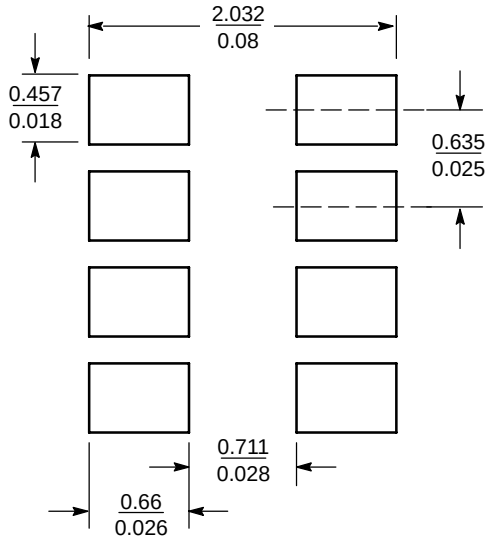


Figure 12. Basic

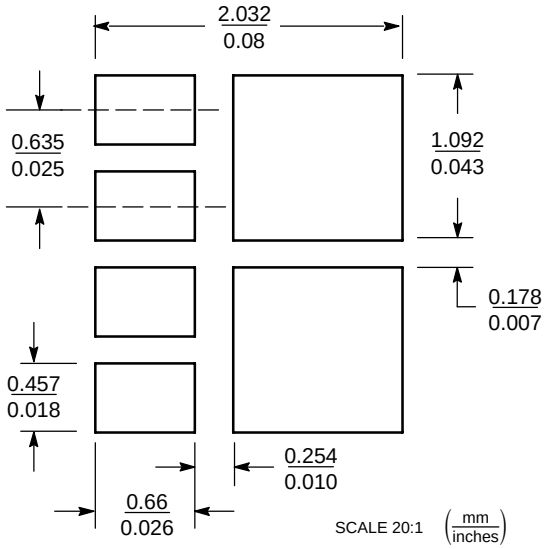


Figure 13. Style 2

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 12. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 13 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

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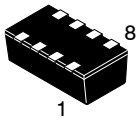
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

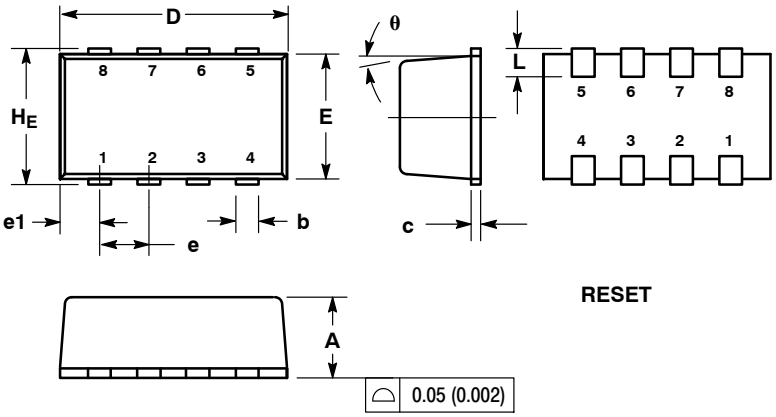
ON Semiconductor®

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

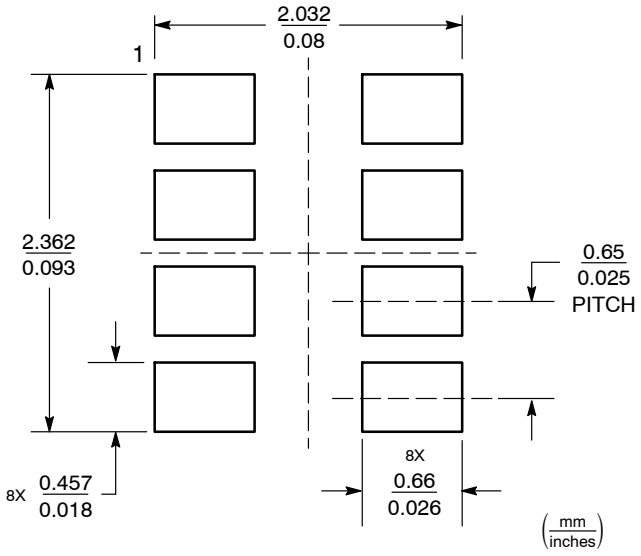
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

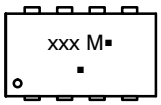
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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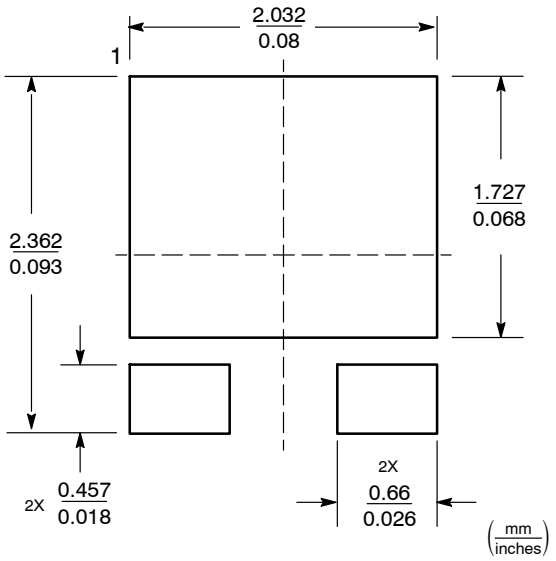
DESCRIPTION:	**ChipFET**	**PAGE 1 OF 2**

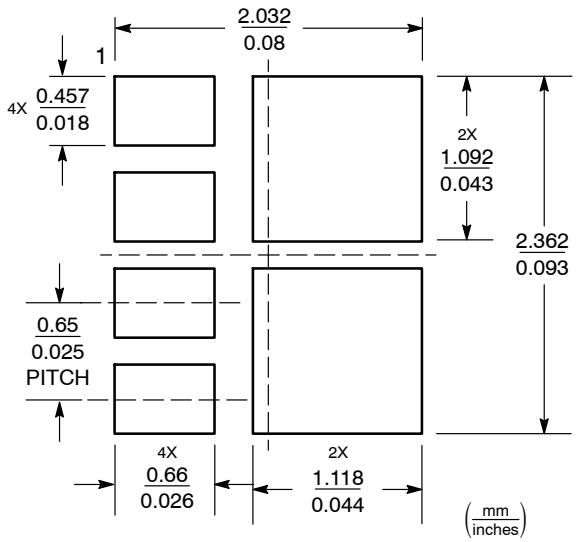
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

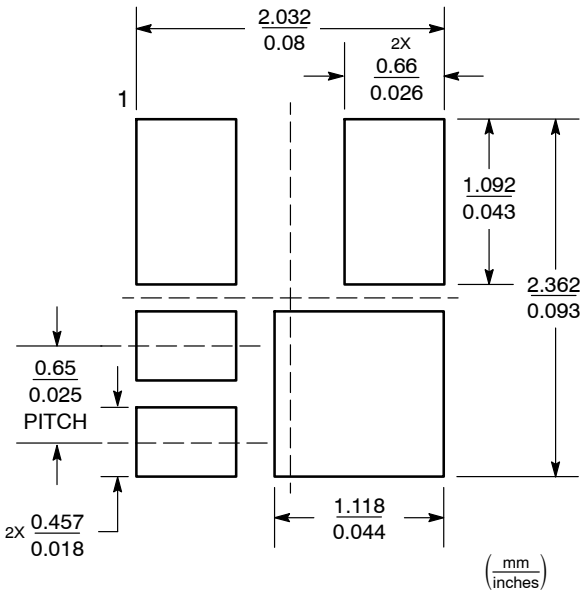
ADDITIONAL SOLDERING FOOTPRINTS*



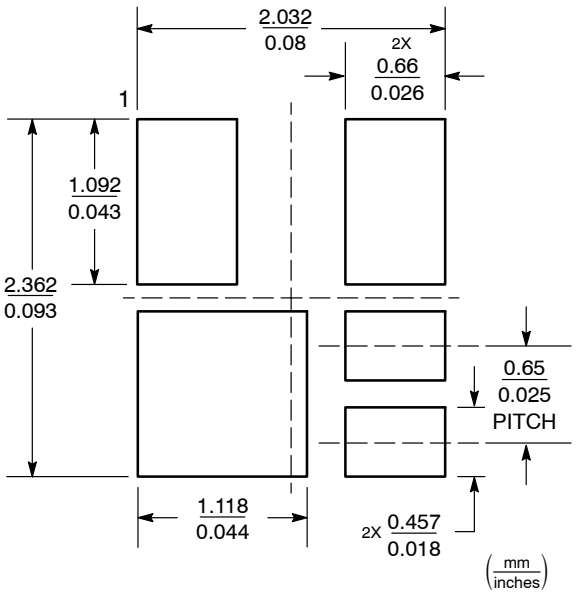
Styles 1 and 4



Style 2



Style 3



Style 5

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DESCRIPTION:	**ChipFET**	**PAGE 2 OF 2**

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