

# Enhancement Mode Gallium Nitride (GaN) HEMT

**40 V, 0.5 mΩ, 819 A, En-FCLGA 5.0x6.0**

## Preliminary Document NTLEF0D7N04GN1

### Features

- Low  $R_{DS(ON)}$  to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- $FOM-Q_G = 27 \text{ nC} \cdot \text{m}\Omega$
- Small Footprint for High Density PCB Design
- Pb-Free, Halide Free and RoHS Compliant

### Typical Applications

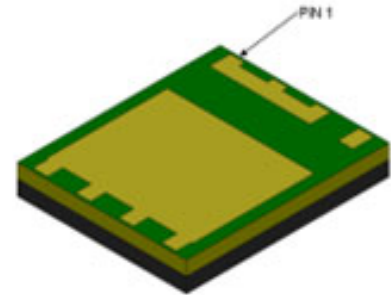
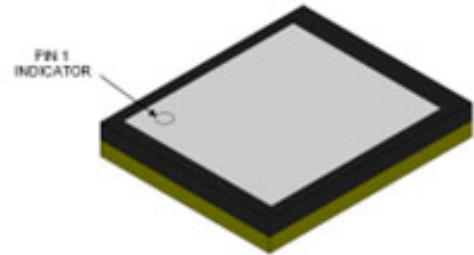
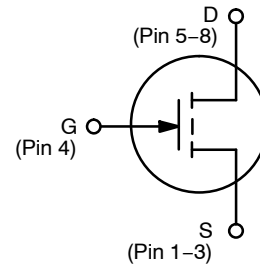
- High Density Power Modules
- High Frequency DC-DC Converters
- High Power Synchronous Rectifiers
- Motor Drivers

### MAXIMUM RATINGS ( $T_J = 25 \text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	40	V
Drain-to-Source Transient Voltage, $t_p < 100 \text{ } \mu\text{s}$	$V_{DS(TRAN)}$	TBD	V
Gate-to-Source Voltage	$V_{GS}$	-4 to 6	V
Gate-to-Source Transient Voltage, $t_p = 100 \text{ ns}$ , $f_p = 100 \text{ kHz}$ , open drain	$V_{GS(PULSE)}$	6.5 (TBD)	V
Continuous Drain Current, $T_{CASE} = 25 \text{ }^\circ\text{C}$ $T_{CASE} = 100 \text{ }^\circ\text{C}$	$I_{DS}$	819	A
		518	
Pulsed Drain Current, $t_p < 100 \text{ } \mu\text{s}$ , $T_J = 25 \text{ }^\circ\text{C}$ $T_J = 150 \text{ }^\circ\text{C}$	$I_{DS(PULSE)}$	1900	A
		1500	
Power Dissipation, $V_{GS} = 5 \text{ V}$ , $T_{CASE} = 25 \text{ }^\circ\text{C}$	$P_{TOT}$	962	W
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-40 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_{DS}$ MAX
40 V	0.5 mΩ	819 A



En-FCLGA 5.0 x 6.0 mm  
CASE TBD

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. onsemi may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Cases	$R_{\theta JC}$	0.1	$^{\circ}\text{C}/\text{W}$
Junction-to-Board	$R_{\theta JB}$	2.0	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	37	$^{\circ}\text{C}/\text{W}$
Maximum Soldering Temperature (MSL3)	$T_{SLD}$	260	$^{\circ}\text{C}$

1. Device on 1 in<sup>2</sup>, 2 oz copper pad on single layer FR-4 PCB

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	40			V
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$		6	200	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 125^{\circ}\text{C}$		200		
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 5\text{ V}, V_{DS} = 0\text{ V}$		0.5	200	$\mu\text{A}$
		$V_{GS} = 5\text{ V}, V_{DS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$		25		$\mu\text{A}$

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 5\text{ V}, I_{DS} = 8\text{ A}$		0.5	0.7	$\text{m}\Omega$
		$V_{GS} = 5\text{ V}, I_{DS} = 8\text{ A}, T_J = 125^{\circ}\text{C}$		TBD		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_{DS} = 38\text{ mA}, T_J = 25^{\circ}\text{C}$	0.9	1.2	2.1	V
		$V_{DS} = V_{GS}, I_{DS} = 38\text{ mA}, T_J = 125^{\circ}\text{C}$		TBD		

### DYNAMIC CHARACTERISTICS

Input Capacitance	$C_{ISS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		7715		$\text{pF}$		
Output Capacitance	$C_{OSS}$			2330				
Reverse Transfer Capacitance	$C_{RSS}$			110				
Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ V to } 20\text{ V}, V_{GS} = 0\text{ V}$		3300		$\text{pF}$		
Output Capacitance, Time Related	$C_{OSS(TR)}$			3925				
Output Charge	$Q_{OSS}$			78			$\text{nC}$	
Output Capacitance Stored Energy	$E_{OSS}$			0.66			$\mu\text{J}$	
Gate Resistance	$R_G$		$f = 5\text{ MHz}, \text{open drain}$		1.6			$\Omega$
Gate Charge	$Q_G$		$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}, V_{GS} = 0/5\text{ V}$		52			$\text{nC}$
Gate-to-Source Charge	$Q_{GS}$			14.2				
Gate-to-Drain Charge	$Q_{GD}$			5.6				
Gate Plateau Voltage	$V_{PLAT}$			1.8		V		

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{D(ON)}$	$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}, V_{GS} = 0/5\text{ V}, R_G = 2\ \Omega$		TBD		ns
Turn-Off Delay Time	$t_{D(OFF)}$			TBD		ns
Turn-On Rise Time	$t_R$			TBD		ns
Turn-Off Fall Time	$t_F$			TBD		ns

### REVERSE CONDUCTION CHARACTERISTICS

Source-to-Drain Reverse Voltage	$V_{SD}$	$V_{GS} = -3\text{ V}, I_{SD} = 50\text{ A}$		5.7		V
		$V_{GS} = 0\text{ V}, I_{SD} = 50\text{ A}$		1.9		
		$V_{GS} = 5\text{ V}, I_{SD} = 50\text{ A}$		0.025		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## GATE DRIVE GUIDELINES

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of

5 – 6 V is recommended, with optional negative gate bias for hard-switching applications to improve  $dv/dt$  immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

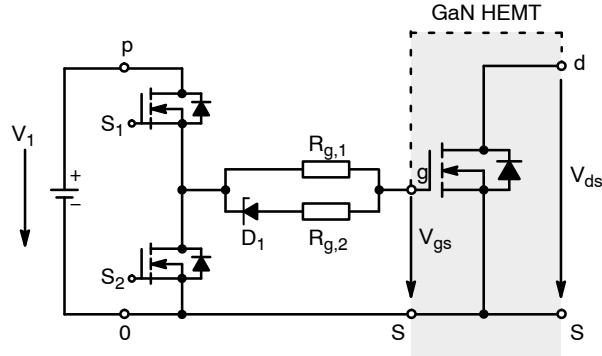


Figure 1. Schottky Gate Conventional Driver Schematic

## ORDERING INFORMATION

Device Order Number	Package Type	Shipping
ENGNTLEF0D7N04GN1TXG	En-FCLGA 5.0 x 6.0	TBD

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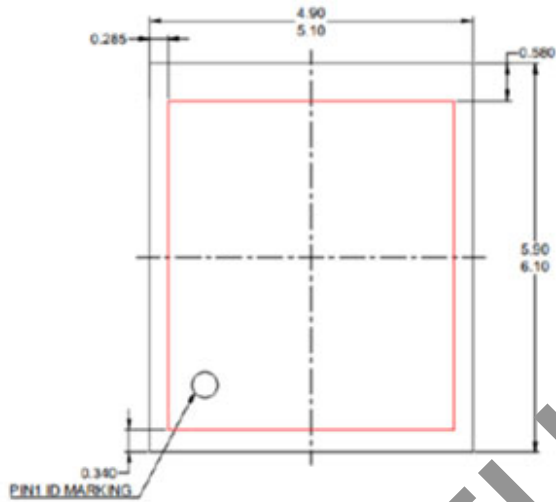
## REVISION HISTORY

Revision	Description of Changes	Date
P0	Initial Preliminary document release.	4/7/2026
P1	<ul style="list-style-type: none"><li>Electrical spec is updated and typical characteristics are added.</li></ul>	4/22/2026

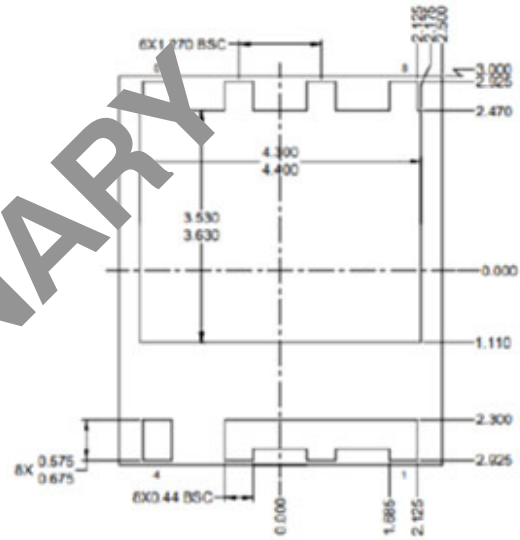
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## PACKAGE DIMENSIONS

En-FCLGA 5.0 x 6.0 mm  
CASE TBD  
ISSUE TBD



TOP VIEW



BOTTOM VIEW



SIDE VIEW

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) DRAWING IS NOT TO SCALE.

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