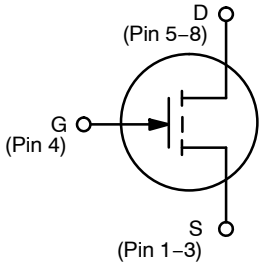
Enhancement Mode Gallium Nitride (GaN) HEMT

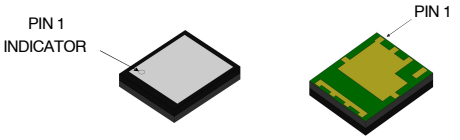
150 V, 1.6 mΩ, TBD A, PDSO-N8 5.0x6.0

Preliminary Document

NTLEF2D2N15GN1

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_{DS} MAX
150 V	1.6 mΩ	TBD A





PDSO-N8 5.00x6.00x0.87, 1.27P
CASE 144AC

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM-Q_G = 54.4 nC*mΩ
- Small Footprint for High Density PCB Design
- Pb-Free, Halide Free and RoHS Compliant

Typical Applications

- High Density Power Modules
- High Frequency DC-DC Converters
- High Power Synchronous Rectifiers
- Motor Drivers

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	150	V
Drain-to-Source Transient Voltage, t_P < 100 μs	$V_{DS(TRAN)}$	TBD	V
Gate-to-Source Voltage	V_{GS}	−4 to 6	V
Gate-to-Source Transient Voltage, t_P = 100 ns, f_P = 100 kHz, open drain	$V_{GS(PULSE)}$	6.5	V
Continuous Drain Current, T_{CASE} = 25 °C T_{CASE} = 100 °C	I_{DS}	 TBD TBD	A
Pulsed Drain Current, t_P < 100 μs, T_J = 25 °C T_J = 150 °C	$I_{DS(PULSE)}$	 840 640	A
Power Dissipation, V_{GS} = 5 V, T_{CASE} = 25 °C	P_{TOT}	TBD	W
Operating Junction Temperature	T_J	−55 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

© Semiconductor Components Industries, LLC, 2026

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Cases	$R_{\theta JC}$	TBD	°C/W
Junction-to-Board	$R_{\theta JB}$	TBD	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	TBD	°C/W
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	°C

1. Device on 1 in^2, 2 oz copper pad on single layer FR-4 PCB.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	150			V
Drain-to-Source Leakage Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 150 V		4	TBD	μA
		V_{GS} = 0 V, V_{DS} = 150 V, T_J = 125 °C		60		
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6 V, V_{DS} = 0 V		2	TBD	μA
		V_{GS} = 6 V, V_{DS} = 0 V, T_J = 125 °C		40		μA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 5 V, I_{DS} = 50 A		1.6	2.2	mΩ
		V_{GS} = 5 V, I_{DS} = 50 A, T_J = 125 °C		TBD		
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_{DS} = 10 mA, T_J = 25 °C		1.1		V
		V_{DS} = V_{GS}, I_{DS} = 10 mA, T_J = 125 °C		TBD		
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz		4820		pF
Output Capacitance	C_{OSS}			1150		
Reverse Transfer Capacitance	C_{RSS}			19		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	V_{DS} = 0 V to 75 V, V_{GS} = 0 V		TBD		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			TBD		
Output Charge	Q_{OSS}			187		nC
Output Capacitance Stored Energy	E_{OSS}			TBD		μJ
Gate Resistance	R_G	f = 5 MHz		TBD		Ω
Gate Charge	Q_G	V_{DS} = 75 V, I_{DS} = 50 A, V_{GS} = 0/5 V		34		nC
Gate-to-Source Charge	Q_{GS}			10.8		
Gate-to-Drain Charge	Q_{GD}			4.7		
Gate Plateau Voltage	V_{PLAT}			TBD		V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DS} = 75 V, I_{DS} = 50 A, V_{GS} = 0/5 V, R_G = 4 Ω		TBD		ns
Turn-Off Delay Time	$t_{D(OFF)}$			TBD		ns
Turn-On Rise Time	t_R			TBD		ns
Turn-Off Fall Time	t_F			TBD		ns
REVERSE CONDUCTION CHARACTERISTICS						
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = −3 V, I_{SD} = 50 A		TBD		V
		V_{GS} = 0 V, I_{SD} = 50 A		TBD		
		V_{GS} = 5 V, I_{SD} = 50 A		TBD		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Share Feedback
Your Opinion Matters

GATE DRIVE GUIDELINES

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of **5 – 6 V** is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

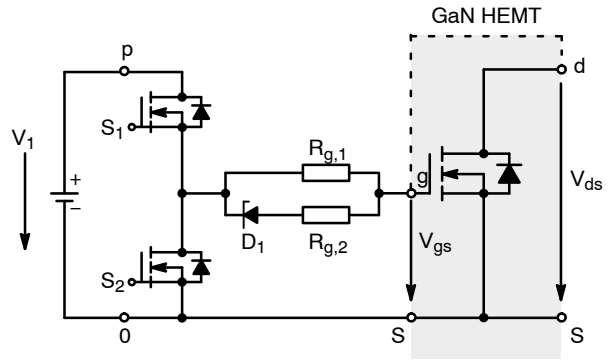


Figure 1. Schottky Gate Conventional Driver Schematic

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
ENGNTLEF2D2N15GN1TXG	PDSO-N8 5.00x6.00x0.87, 1.27P	2500 / Tape & Reel

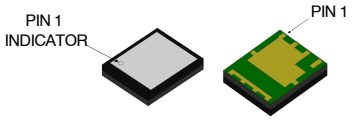
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Share Feedback
Your Opinion Matters

REVISION HISTORY

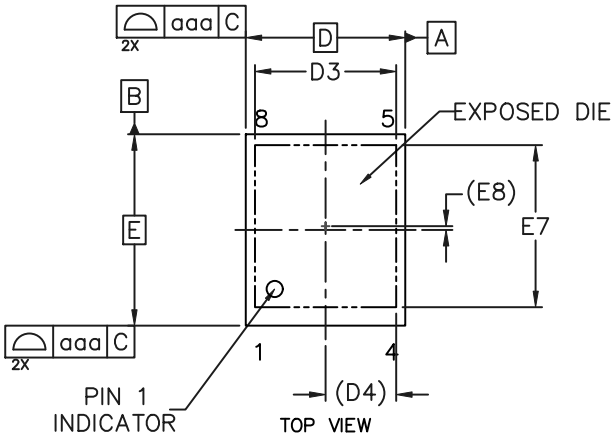
Revision	Description of Changes	Date
P0	Initial Preliminary document release.	4/3/2026
P1	Update – Package and Shipping information, Marking Diagram.	7/8/2026

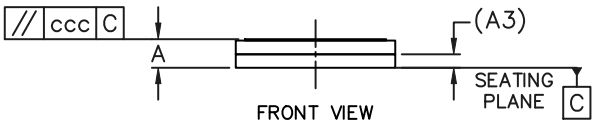
Share Feedback
Your Opinion Matters

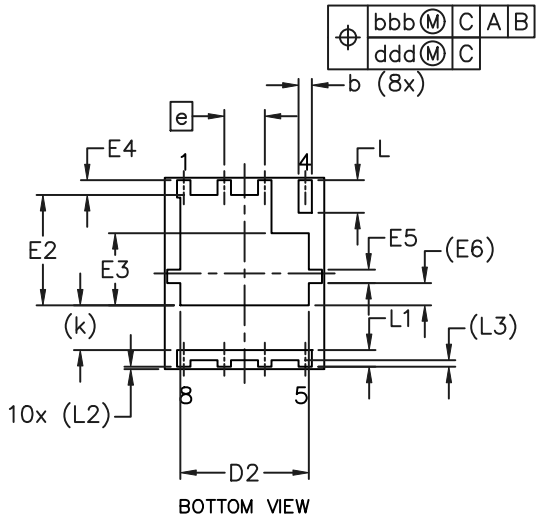


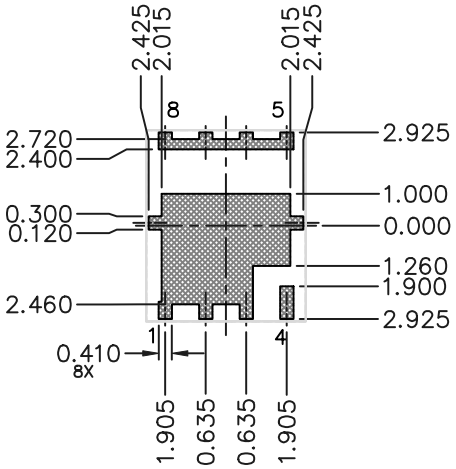
PDSO-N8 5.00x6.00x0.87, 1.27P
CASE 144AC
ISSUE O

DATE 19 MAR 2026









LAND PATTERN
RECOMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.77	0.87	0.97
A3		0.425 REF	
b	0.37	0.42	0.47
D		5.00 BSC	
D2	3.93	4.03	4.13
D3	3.60	–	4.40
D4		2.19 REF	
e		1.27 BSC	
E		6.00 BSC	
E2	3.36	3.46	3.56
E3	2.16	2.26	2.36
E4	0.415	0.465	0.515
E5	0.37	0.42	0.47
E6		0.70 REF	
E7	4.60	–	5.50
E8		0.12 REF	
k		1.40 REF	
L	0.925	1.025	1.125
L1	0.425	0.525	0.625
L2		0.075 REF	
L3		0.205 REF	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON74816H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**PDSO-N8 5.00x6.00x0.87, 1.27P**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales