

MOSFET - Power, Dual, N-Channel, Power Clip, POWER TRENCH[®], Asymmetric 25 V

NTMFD1D1N02X

Features

- Small Footprint (5x6mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These are Pb-free, Halogen Free / BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- System Voltage Rails

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | | | Symbol | Q1 | Q2 | Unit |
|---|---|--------------------------|----------------------|--------------|--------------|------------------|
| Drain-to-Source Voltage | | | V_{DSS} | 25 | 25 | V |
| Gate-to-Source Voltage | | | V_{GS} | +16V -12V | +16V -12V | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D | 75 | 178 | A |
| | | $T_C = 85^\circ\text{C}$ | | 54 | 128 | |
| Power Dissipation $R_{\theta JC}$ (Note 3) | | $T_C = 25^\circ\text{C}$ | P_D | 27 | 44 | W |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D | 20 | 40 | A |
| | | $T_A = 85^\circ\text{C}$ | | 15 | 29 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | | $T_A = 25^\circ\text{C}$ | P_D | 2.1 | 2.3 | W |
| Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D | 14 | 27 | A |
| | | $T_A = 85^\circ\text{C}$ | | 10 | 20 | |
| Power Dissipation $R_{\theta JA}$ (Notes 2, 3) | | $T_A = 25^\circ\text{C}$ | P_D | 0.96 | 1.0 | W |
| Pulsed Drain Current | $T_C = 25^\circ\text{C}$, $t_p = 100 \mu\text{s}$ | I_{DM} | | 331 | 625 | A |
| Single Pulse Drain-to-Source Avalanche Energy Q1: $I_L = 5.6 A_{pk}$, $L = 3 \text{ mH}$ (Note 4) Q2: $I_L = 13.6 A_{pk}$, $L = 3 \text{ mH}$ (Note 4) | | | E_{AS} | 47 | 277 | mJ |
| Operating Junction and Storage Temperature Range | | | T_J , T_{stg} | -55 to 150 | | $^\circ\text{C}$ |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s) | | | T_L | 260 | | $^\circ\text{C}$ |

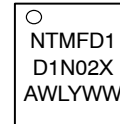
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

| FET | $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | I_D MAX |
|-----|---------------|-------------------------|-----------|
| Q1 | 25 V | 3.0 m Ω @ 10 V | 75 A |
| | | 3.75 m Ω @ 4.5 V | |
| Q2 | 25 V | 0.87 m Ω @ 10 V | 178 A |
| | | 1.1 m Ω @ 4.5 V | |



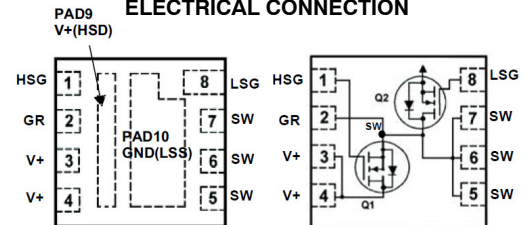
PQFN8
POWER CLIP
CASE 483AR

MARKING DIAGRAM



NTMFD1D1N02X = Specific Device Code
A = Assembly Site
WL = Wafer Lot Number
Y = Year of Production
WW = Work Week Number

ELECTRICAL CONNECTION



ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|-----------------|-----------------------|
| NTMFD1D1N02X | PQFN8 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFD1D1N02X

Table 1. THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Q1 Max | Q2 Max | Units |
|--|-----------------|--------|--------|-------|
| Junction-to-Case – Steady State (Note 1, 3) | $R_{\theta JC}$ | 4.6 | 2.8 | °C/W |
| Junction-to-Ambient – Steady State (Note 1, 3) | $R_{\theta JA}$ | 60 | 55 | |
| Junction-to-Ambient – Steady State (Note 2, 3) | $R_{\theta JA}$ | 130 | 120 | |

- Surface-mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.
- Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
- Q1 100% UIS tested at L = 0.1 mH, $I_{AS} = 17.4$ A.
Q2 100% UIS tested at L = 0.1 mH, $I_{AS} = 42.5$ A.

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Test Condition | FET | Min | Typ | Max | Unit | | |
|---|---------------------|---|---------------------------|---------------------------|-----|-----------|-------|---------------|---------------|
| OFF CHARACTERISTICS | | | | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | Q1 | 25 | | | V | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | Q2 | 25 | | | V | | |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS} / T_J$ | $I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$ | Q1 | | 15 | | mV/°C | | |
| | | $I_D = 250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$ | Q2 | | 16 | | | | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ | $T_J = 25^\circ\text{C}$ | | | | 10 | μA | |
| | | | $T_J = 125^\circ\text{C}$ | | | | 100 | | |
| | | | | $T_J = 25^\circ\text{C}$ | | | | 100 | μA |
| | | | | $T_J = 125^\circ\text{C}$ | | | | 100 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$ | Q1 | | | ± 100 | nA | | |
| | | $V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$ | Q2 | | | ± 100 | | | |

ON CHARACTERISTICS (Note 5)

| | | | | | | | |
|-----------------------------------|--------------------|---|----|------|------|------|------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 240\ \mu\text{A}$ | Q1 | 1.2 | 1.6 | 2.1 | V |
| | | $V_{GS} = V_{DS}, I_D = 850\ \mu\text{A}$ | Q2 | 1.2 | 1.6 | 2.1 | |
| Threshold Temperature Coefficient | $V_{GS(TH)} / T_J$ | $I_D = 240\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$ | Q1 | | -4.0 | | mV/°C |
| | | $I_D = 850\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$ | Q2 | | -4.3 | | |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ | Q1 | | 2.4 | 3.0 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$ | | | 3.1 | 3.75 | |
| | | $V_{GS} = 10\text{ V}, I_D = 37\text{ A}$ | Q2 | | 0.66 | 0.87 | |
| | | $V_{GS} = 4.5\text{ V}, I_D = 33\text{ A}$ | | 0.68 | 0.84 | 1.1 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 5\text{ V}, I_D = 20\text{ A}$ | Q1 | | 123 | | S |
| | | $V_{DS} = 5\text{ V}, I_D = 37\text{ A}$ | Q2 | | 322 | | |
| Gate Resistance | R_G | $T_A = 25^\circ\text{C}$ | Q1 | | 0.8 | | Ω |
| | | | Q2 | | 0.9 | | |

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
- Switching characteristics are independent of operating junction temperatures

NTMFD1D1N02X

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Test Condition | FET | Min | Typ | Max | Unit | | |
|-----------------------------------|--------------|--|--|--|------|-----|------|----|----|
| CHARGES & CAPACITANCES | | | | | | | | | |
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, V_{DS} = 12\text{ V}, f = 1\text{ MHz}$ | Q1 | | 1080 | | pF | | |
| | | | Q2 | | 4265 | | | | |
| Output Capacitance | C_{OSS} | | Q1 | | 322 | | pF | | |
| | | | Q2 | | 1020 | | | | |
| Reverse Capacitance | C_{RSS} | | Q1 | | 47 | | pF | | |
| | | | Q2 | | 118 | | | | |
| Total Gate Charge | $Q_{G(TOT)}$ | Q1: $V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 20\text{ A}$ Q2: $V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 37\text{ A}$ | Q1 | | 6.8 | | nC | | |
| | | | Q2 | | 27 | | | | |
| Gate-to-Drain Charge | Q_{GD} | | Q1 | | 1.4 | | nC | | |
| | | | Q2 | | 5.2 | | | | |
| Gate-to-Source Charge | Q_{GS} | | Q1 | | 3.0 | | nC | | |
| | | | Q2 | | 11 | | | | |
| Total Gate Charge | $Q_{G(TOT)}$ | | Q1: $V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 20\text{ A}$ Q2: $V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 37\text{ A}$ | Q1 | | 15 | | nC | |
| | | | | Q2 | | 59 | | | |
| Output Charge | Q_{OSS} | | | $V_{GS} = 0\text{ V}, V_{DS} = 12\text{ V}$ | Q1 | | 6.2 | | nC |
| | | | | | Q2 | | 22 | | |
| Plateau Voltage | V_{GP} | | | Q1: $V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 20\text{ A}$ Q2: $V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 37\text{ A}$ | Q1 | | 2.8 | | V |
| | | | | | Q2 | | 2.8 | | |

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 6)

| | | | | | | | |
|---------------------|--------------|---|----|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}$ Q1: $I_D = 20\text{ A}, V_{DD} = 12\text{ V}, R_G = 2\Omega$ Q2: $I_D = 37\text{ A}, V_{DD} = 12\text{ V}, R_G = 2\Omega$ | Q1 | | 10 | | ns |
| | | | Q2 | | 21 | | |
| Rise Time | $t_r(ON)$ | | Q1 | | 2.5 | | ns |
| | | | Q2 | | 6.6 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | Q1 | | 12 | | ns |
| | | | Q2 | | 26 | | |
| Fall Time | t_f | | Q1 | | 2.5 | | ns |
| | | | Q2 | | 6.0 | | |

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 6)

| | | | | | | | |
|---------------------|--------------|--|----|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}$ Q1: $I_D = 20\text{ A}, V_{DD} = 12\text{ V}, R_G = 2\Omega$ Q2: $I_D = 37\text{ A}, V_{DD} = 12\text{ V}, R_G = 2\Omega$ | Q1 | | 7.4 | | ns |
| | | | Q2 | | 11 | | |
| Rise Time | $t_r(ON)$ | | Q1 | | 1.1 | | ns |
| | | | Q2 | | 2.9 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | Q1 | | 17 | | ns |
| | | | Q2 | | 36 | | |
| Fall Time | t_f | | Q1 | | 1.4 | | ns |
| | | | Q2 | | 3.5 | | |

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

NTMFD1D1N02X

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Test Condition | FET | Min | Typ | Max | Unit | |
|--|----------|--|---------------------------|-----|-----|------|------|--|
| SOURCE-TO-DRAIN DIODE CHARACTERISTICS | | | | | | | | |
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ | $T_J = 25^\circ\text{C}$ | Q1 | | 0.81 | V | |
| | | | $T_J = 125^\circ\text{C}$ | | | 0.68 | | |
| | | $V_{GS} = 0\text{ V}, I_S = 37\text{ A}$ | $T_J = 25^\circ\text{C}$ | Q2 | | 0.8 | | |
| | | | $T_J = 125^\circ\text{C}$ | | | 0.65 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V},$ Q1: $I_S = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ Q2: $I_S = 37\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$ | Q1 | | 18 | | ns | |
| | Q2 | | | 35 | | | | |
| Reverse Recovery Charge | Q_{RR} | | Q1 | | 6.6 | | nC | |
| | | | Q2 | | 44 | | | |

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q1

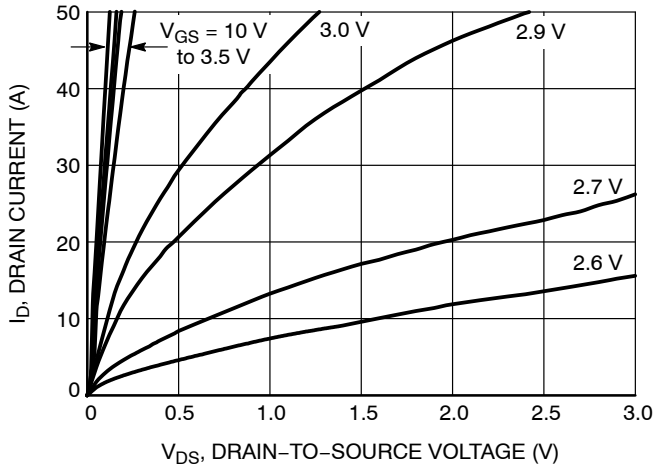


Figure 1. On-Region Characteristics

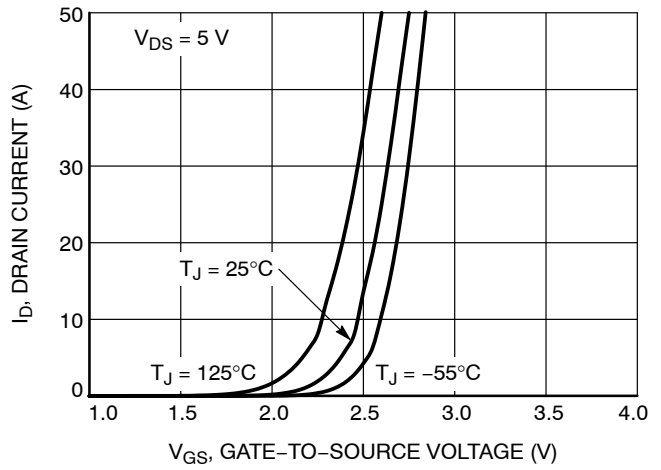


Figure 2. Transfer Characteristics

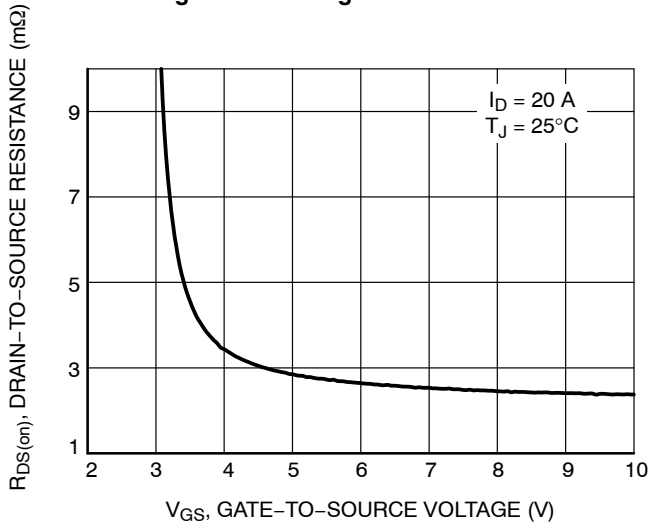


Figure 3. On-Resistance vs. Gate-to-Source Voltage

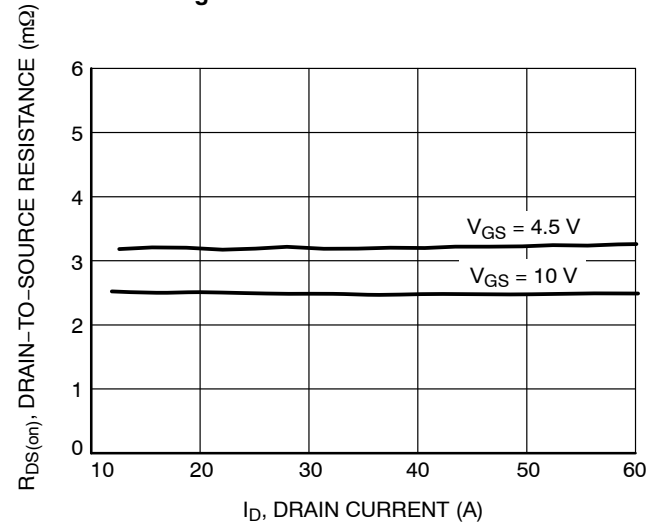


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

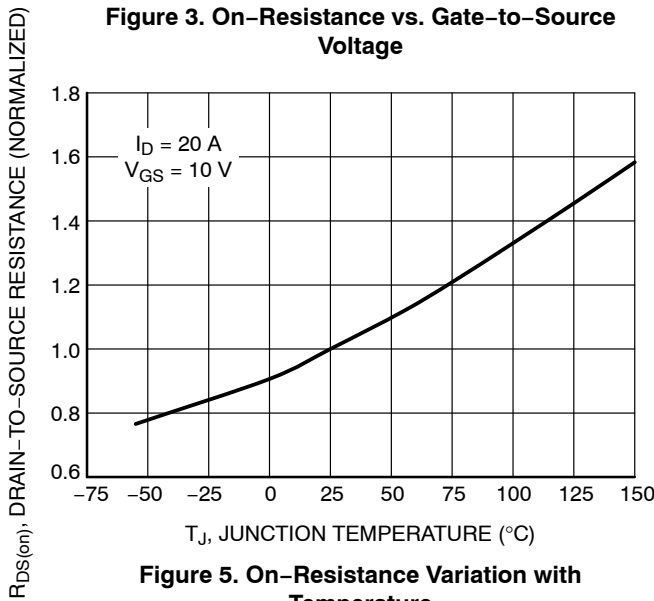


Figure 5. On-Resistance Variation with Temperature

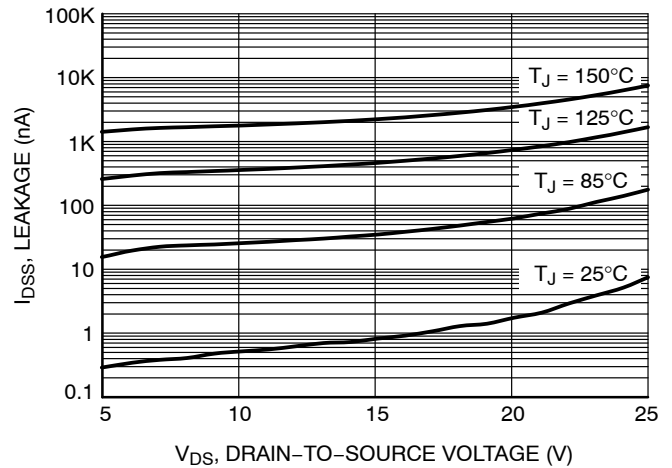


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q1

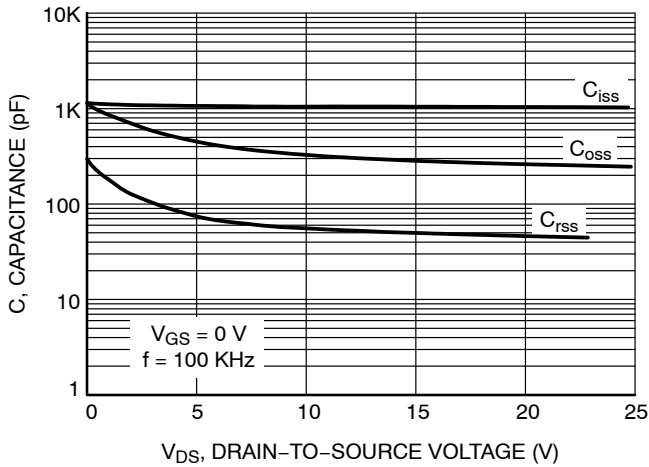


Figure 7. Capacitance Variation

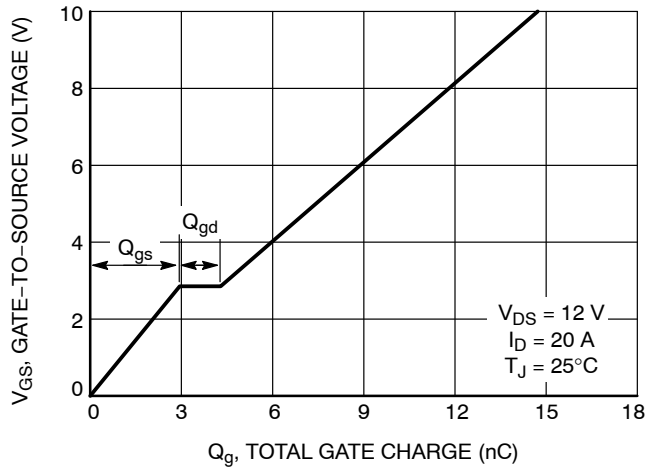


Figure 8. Gate-to-Source vs. Total Charge

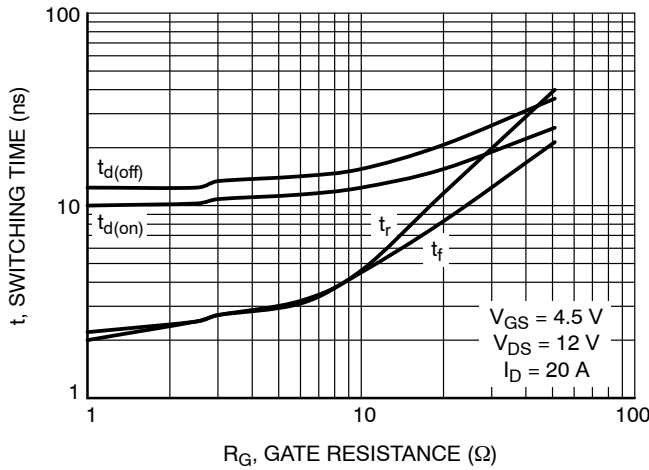


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

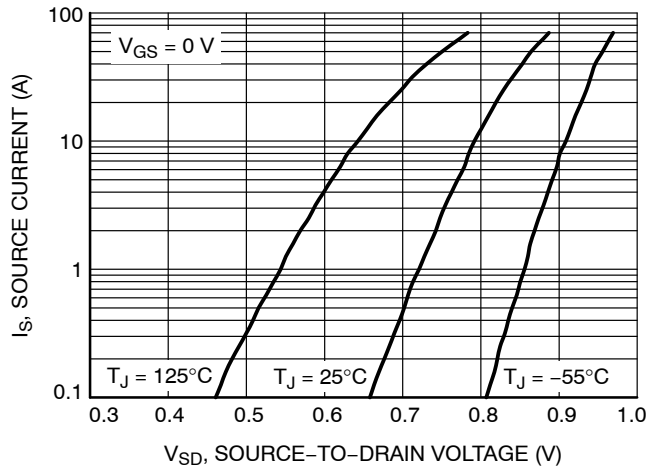


Figure 10. Diode Forward Voltage vs. Current

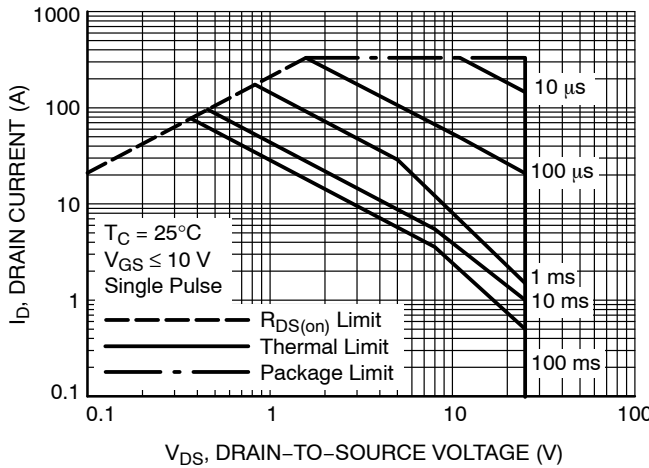


Figure 11. Maximum Rated Forward Biased Safe Operating Area

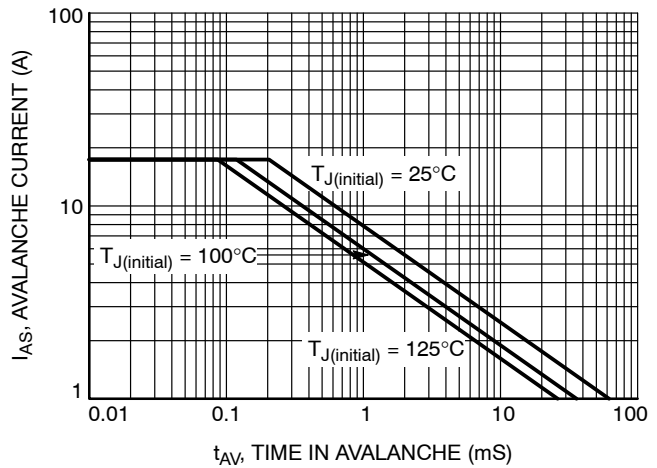


Figure 12. Avalanche Current vs. Time in Avalanche

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q1

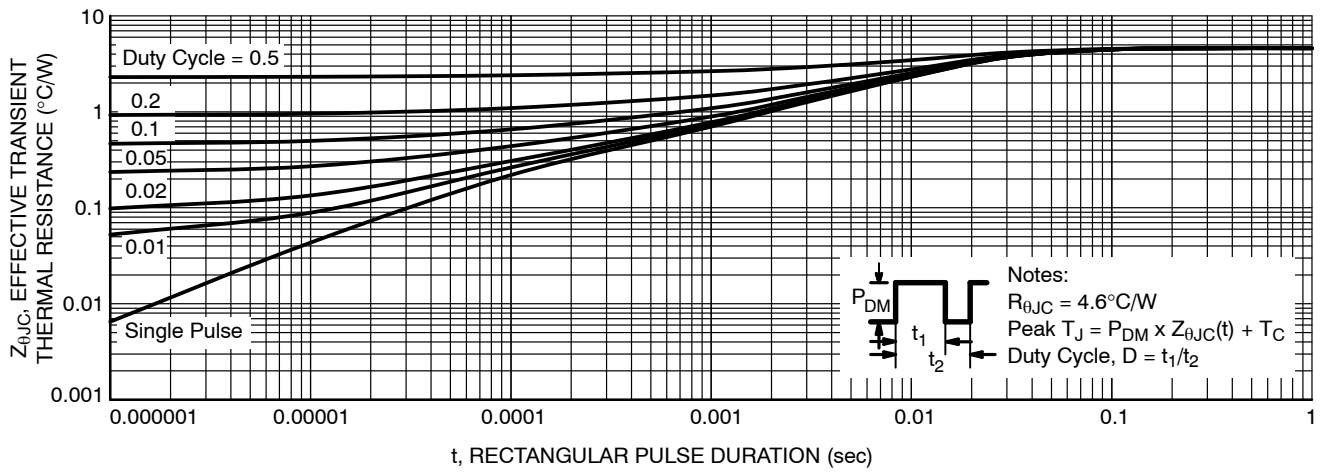


Figure 13. Transient Thermal Impedance

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q2

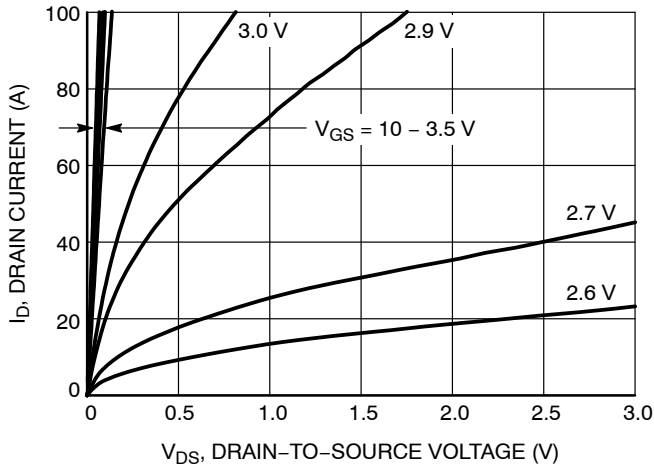


Figure 14. On-Region Characteristics

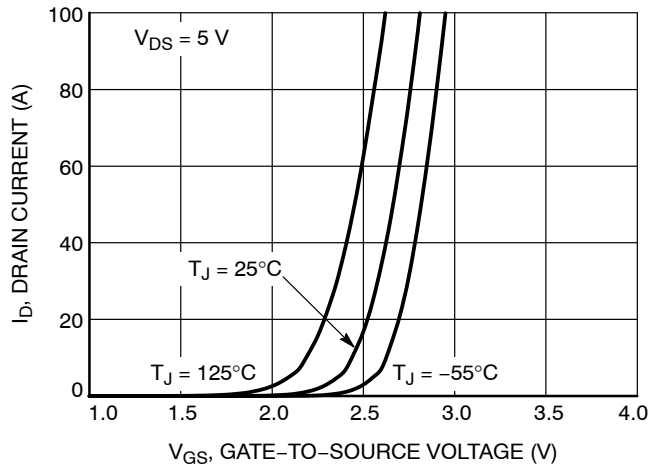


Figure 15. Transfer Characteristics

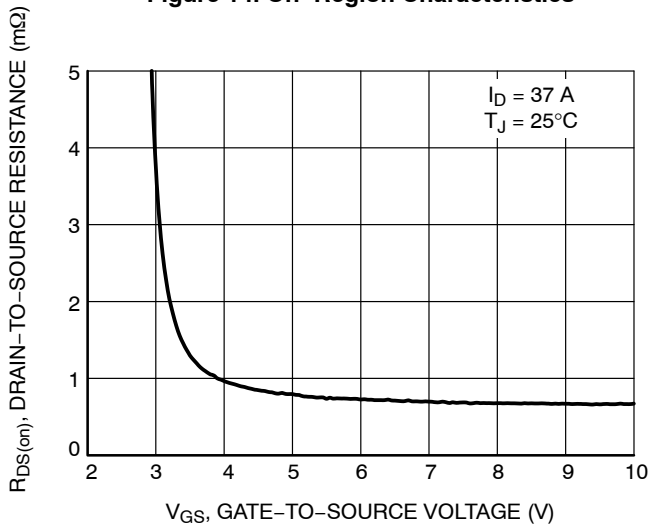


Figure 16. On-Resistance vs. Gate-to-Source Voltage

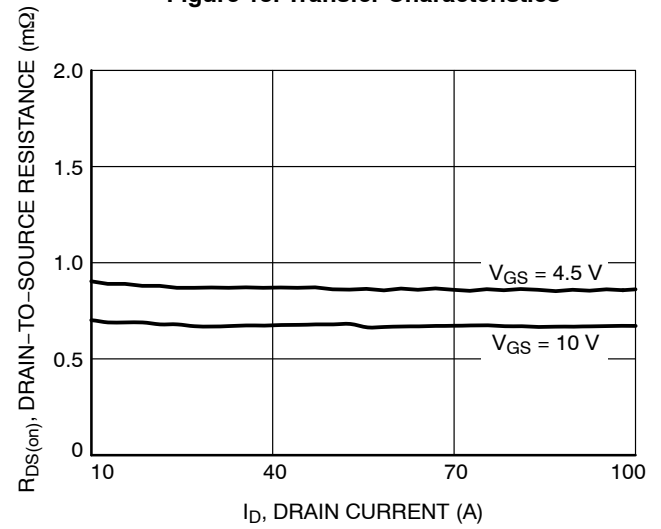


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

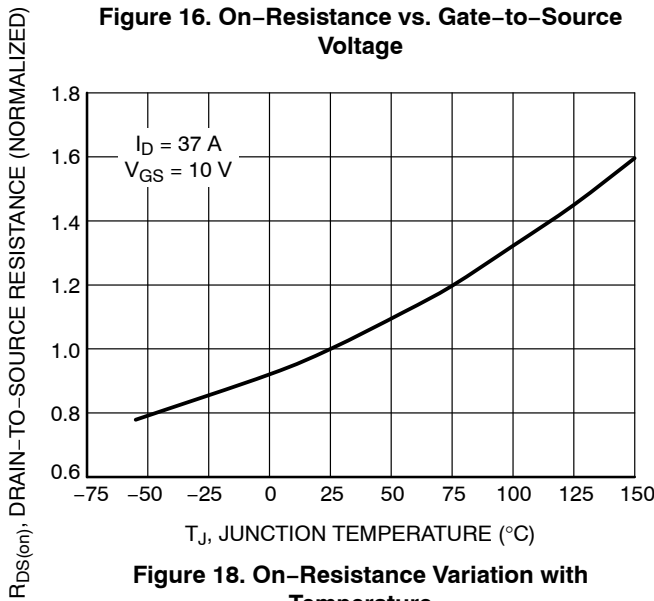


Figure 18. On-Resistance Variation with Temperature

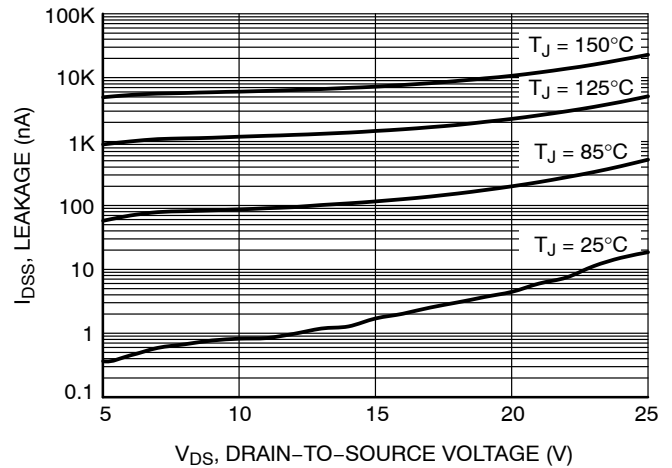


Figure 19. Drain-to-Source Leakage Current vs. Voltage

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q2

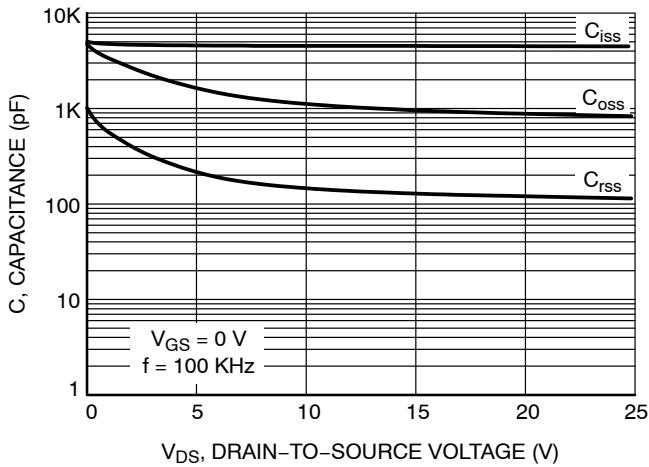


Figure 20. Capacitance Variation

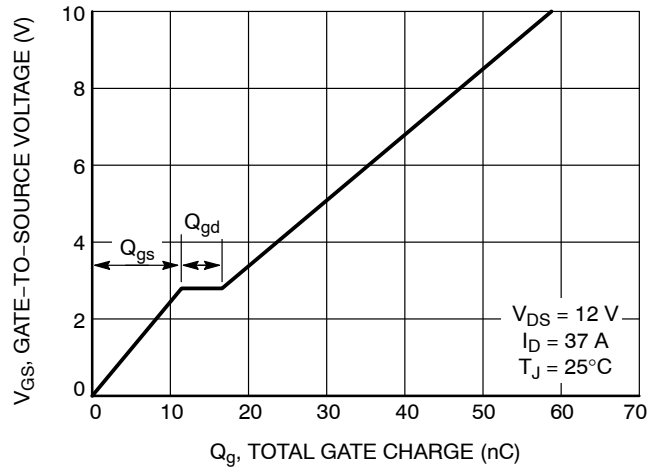


Figure 21. Gate-to-Source vs. Total Charge

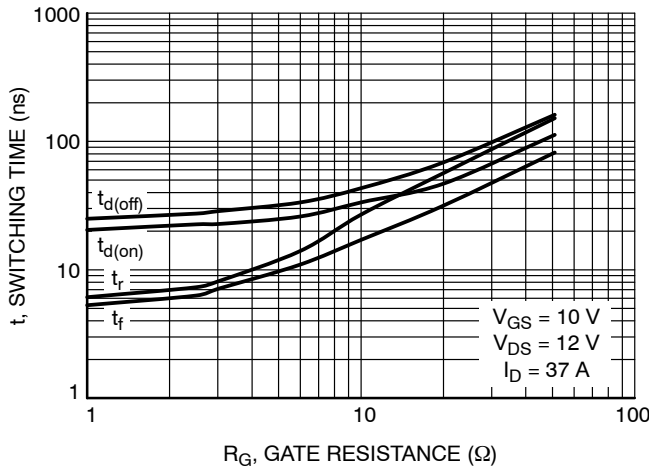


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

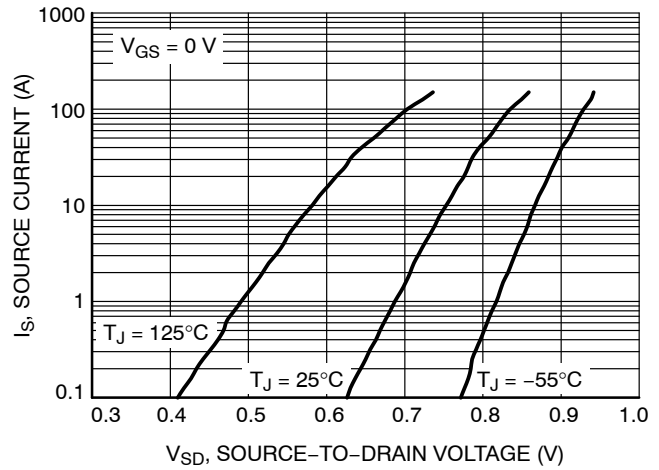


Figure 23. Diode Forward Voltage vs. Current

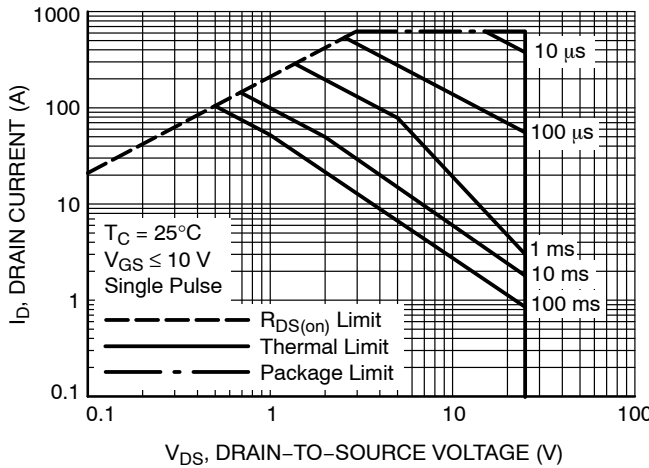


Figure 24. Maximum Rated Forward Biased Safe Operating Area

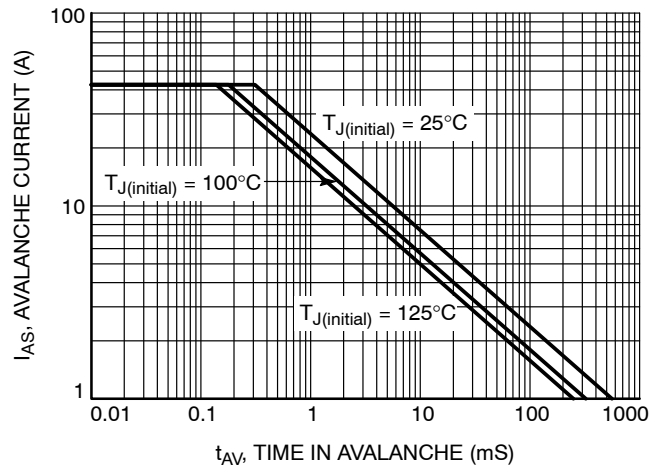


Figure 25. Avalanche Current vs. Time in Avalanche

NTMFD1D1N02X

TYPICAL CHARACTERISTICS – Q2

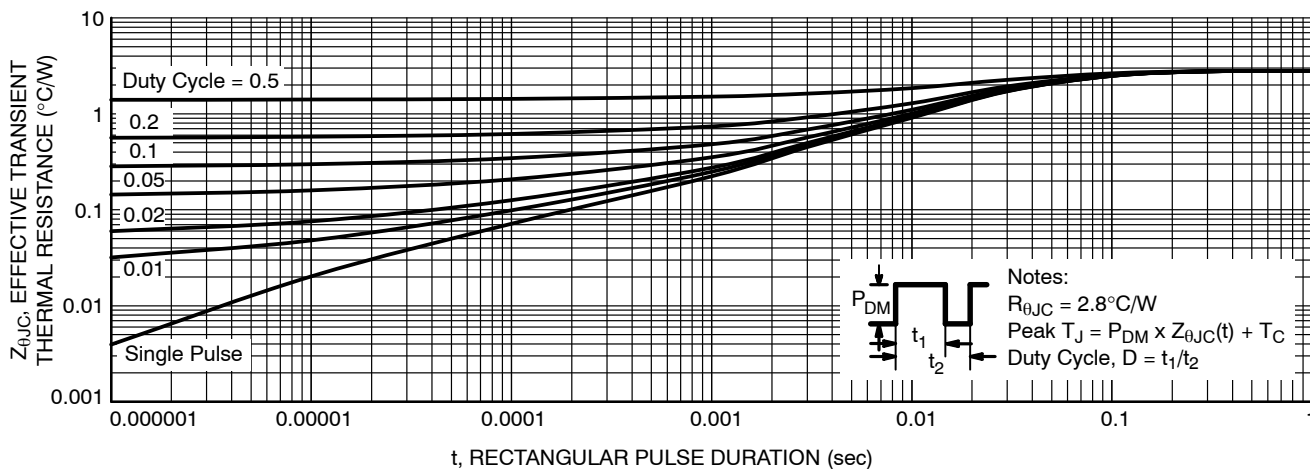
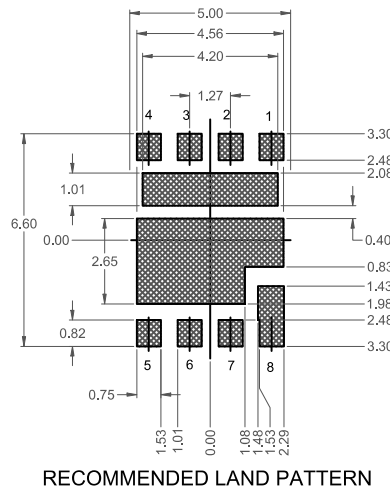
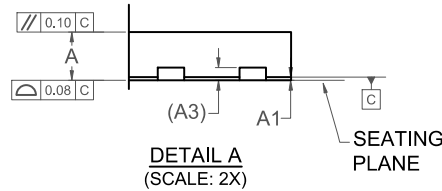
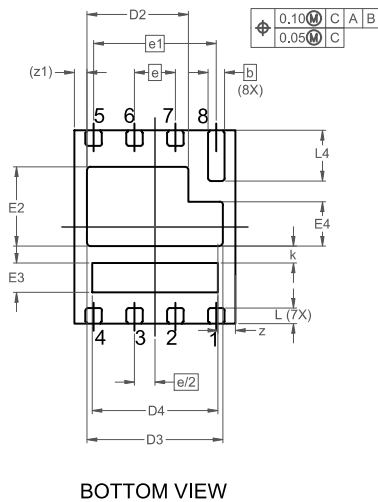
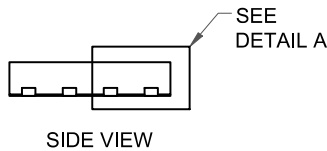
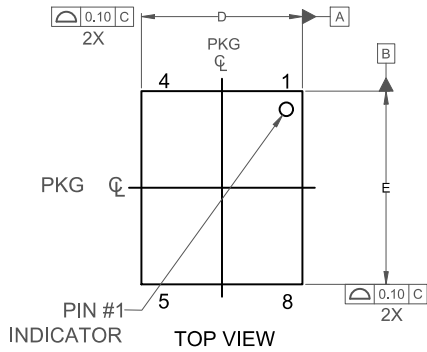


Figure 26. Transient Thermal Impedance

NTMFD1D1N02X

PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483AR
ISSUE A



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.51 BSC | | |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.05 | 3.15 | 3.25 |
| D3 | 4.12 | 4.22 | 4.32 |
| D4 | 3.80 | 3.90 | 4.00 |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 2.36 | 2.46 | 2.56 |
| E3 | 0.81 | 0.91 | 1.01 |
| E4 | 1.27 | 1.37 | 1.47 |
| e | 1.27 BSC | | |
| e/2 | 0.635 BSC | | |
| e1 | 3.81 BSC | | |
| k | 0.42 | 0.52 | 0.62 |
| L | 0.38 | 0.48 | 0.58 |
| L4 | 1.47 | 1.57 | 1.67 |
| z | 0.55 REF | | |
| z1 | 0.39 REF | | |

onsemi, Onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
 Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
 North American Technical Support:
 Voice Mail: 1 800-282-9855 Toll Free USA/Canada
 Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
 Phone: 00421 33 790 2910
 For additional information, please contact your local Sales Representative