

MOSFET - Power, Single N-Channel, STD Gate, DUAL COOL[®], DFN8 5x6

80 V, 2.6 mΩ, 154 A

NTMFSCHT2D6N08X

Features

- Advanced Dual-Side Cool Package with Enhanced Heat-Dissipation Molding Compound
- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_g to Minimize Gate Driving Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- DC/DC Intermediated Bus Converter
- Control FET in High Switching Frequency Application
- Synchronous Rectifier
- ORing FET

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

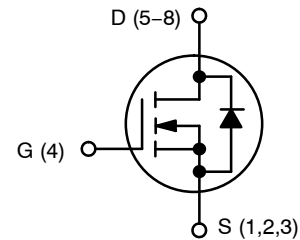
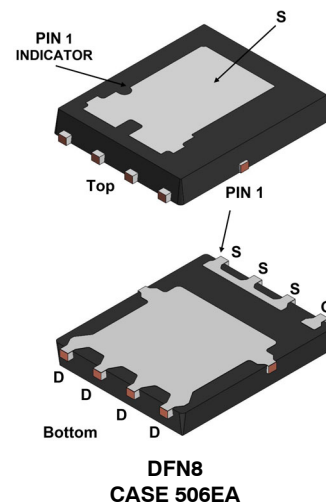
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	154	A
	$T_C = 100\text{ }^{\circ}\text{C}$		109	
Power Dissipation (Notes 1, 2)	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	133	W
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	634	A
Pulsed Source Current (Body Diode)		I_{SM}		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source-Drain Current (Body Diode)	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	133	A
Single Pulse Avalanche Energy ($I_{pk} = 53\text{ A}$) (Note 3)		E_{AS}	140	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

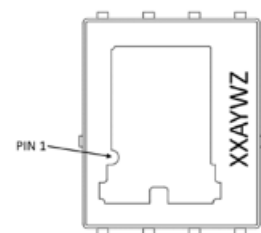
- The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
- Actual continuous current will be limited by thermal & electromechanical application board design.
- E_{AS} of 140 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 53 \text{ A}$, $V_{DD} = 64 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	2.6 mΩ @ $V_{GS} = 10 \text{ V}$	154 A

N-CHANNEL MOSFET



MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NTMFSCHT2D6N08X

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	1.1	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	1.13	
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	39	

4. Actual continuous current will be limited by thermal & electromechanical application board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 80\text{ V}, T_J = 125^\circ\text{C}$			250 (Note 5)	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 37\text{ A}, T_J = 25^\circ\text{C}$		2.2	2.6	m Ω
		$V_{GS} = 6\text{ V}, I_D = 18\text{ A}, T_J = 25^\circ\text{C}$		3.3	5.2	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 184\text{ }\mu\text{A}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 184\text{ }\mu\text{A}$		-7		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 37\text{ A}$		115		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance (Note 5)	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	1600	3200	4800	pF
Output Capacitance (Note 5)	C_{OSS}			930	1395	
Reverse Transfer Capacitance (Note 5)	C_{RSS}			14	28	
Output Charge	Q_{OSS}			66		nC
Total Gate Charge (Note 5)	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		28	42	
		$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		45	67	
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 40\text{ V}, I_D = 37\text{ A}$		10		
Gate-to-Source Charge	Q_{GS}			15		
Gate-to-Drain Charge	Q_{GD}			7	14	
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance (Note 5)	R_G	$f = 1\text{ MHz}$	0.4	0.9	1.2	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 37\text{ A}, R_G = 2.5\text{ }\Omega$		24		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(OFF)}$			35		
Fall Time	t_f			6		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 25^\circ\text{C}$		0.8	1.0	V
		$V_{GS} = 0\text{ V}, I_S = 37\text{ A}, T_J = 125^\circ\text{C}$		0.6		



NTMFSCHT2D6N08X

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI/dt = 1000\text{ A}/\mu\text{s}$, $I_S = 37\text{ A}$, $V_{DD} = 40\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$		24		ns
Charge Time	t_a			13		
Discharge Time	t_b			11		
Reverse Recovery Charge	Q_{RR}			163		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Defined by design, not subject to production test.



NTMF5CHT2D6N08X

TYPICAL CHARACTERISTICS

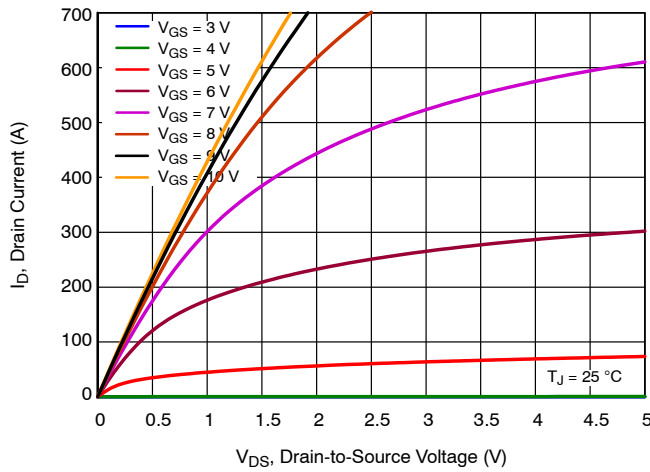


Figure 1. On-Region Characteristics

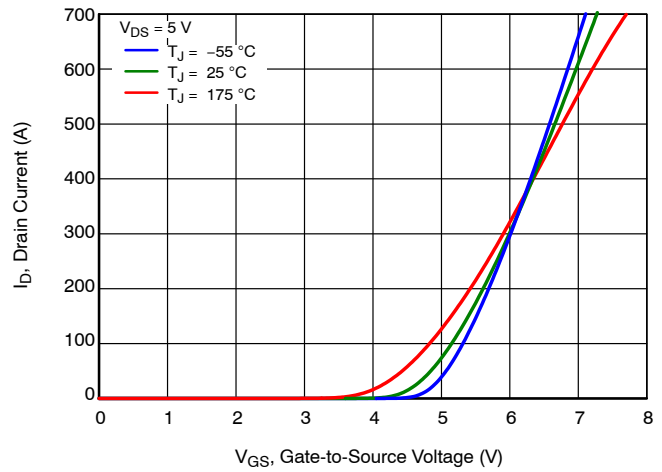


Figure 2. Transfer Characteristics

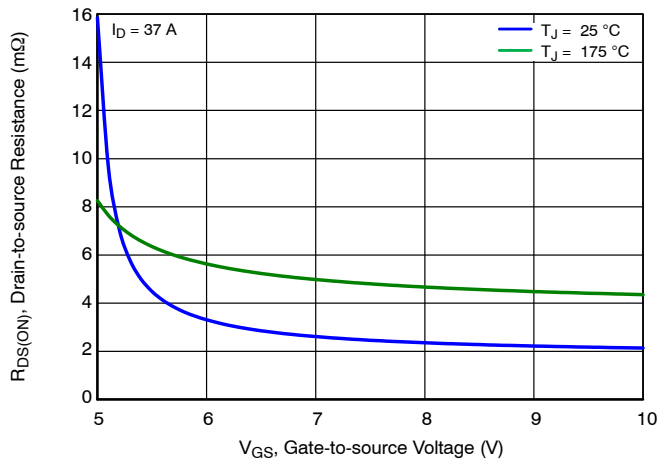


Figure 3. On-Resistance vs. Gate Voltage

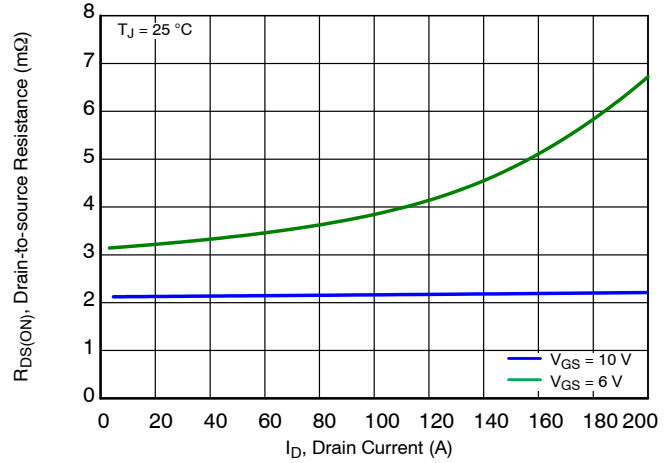


Figure 4. On-Resistance vs. Drain Current

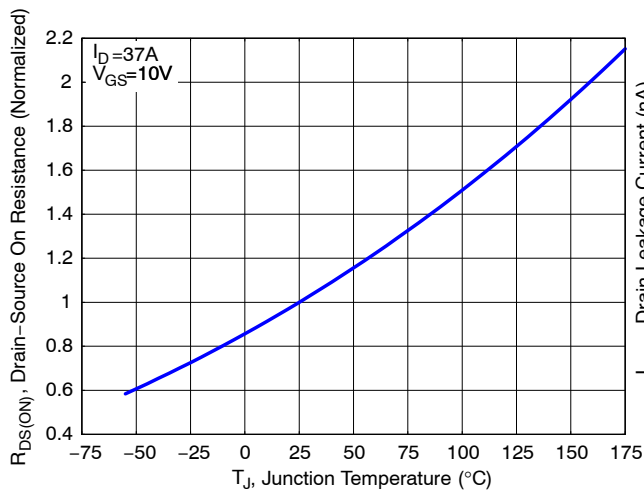


Figure 5. Normalized ON Resistance vs. Junction Temperature

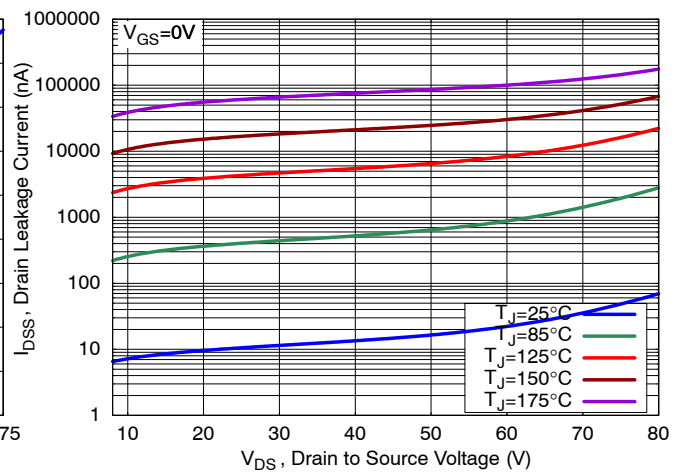


Figure 6. Drain Leakage Current vs. Drain Voltage

NTMFSCHT2D6N08X

TYPICAL CHARACTERISTICS (continued)

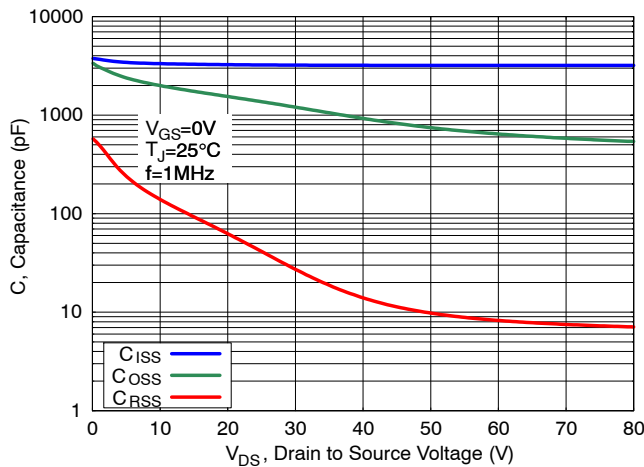


Figure 7. Capacitance Characteristics

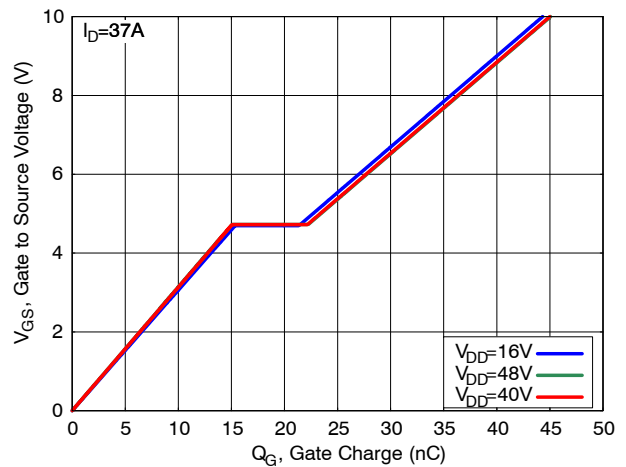


Figure 8. Gate Charge Characteristics

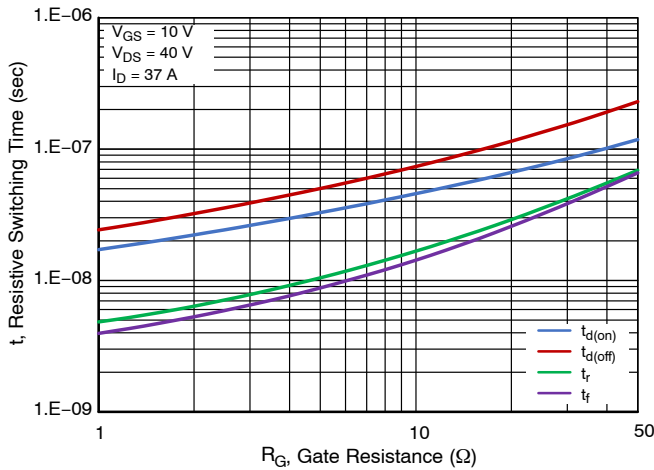


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

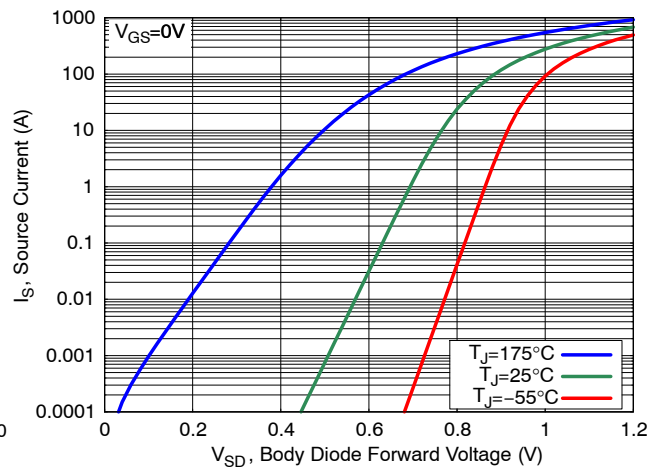


Figure 10. Diode Forward Characteristics

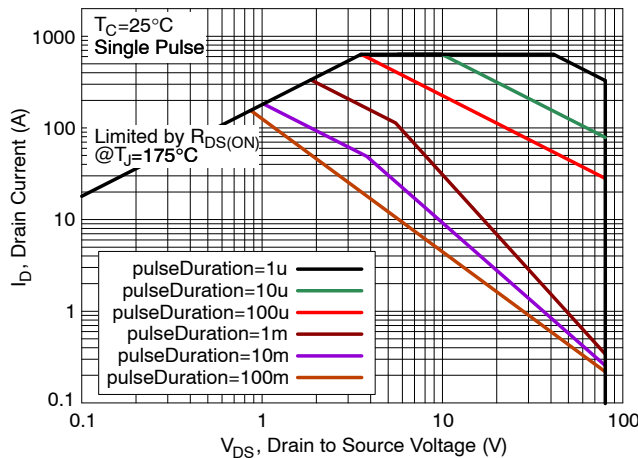


Figure 11. Safe Operating Area (SOA)

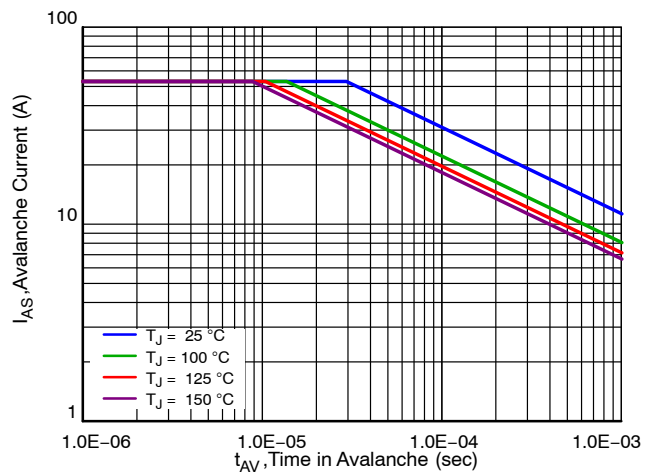


Figure 12. Avalanche Current vs. Pulse Time (UIS)

NTMFSCHT2D6N08X

TYPICAL CHARACTERISTICS (continued)

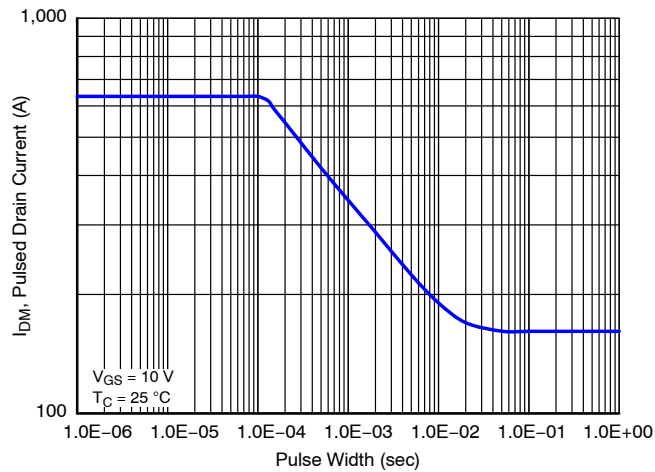


Figure 13. I_{DM} vs Pulse Width

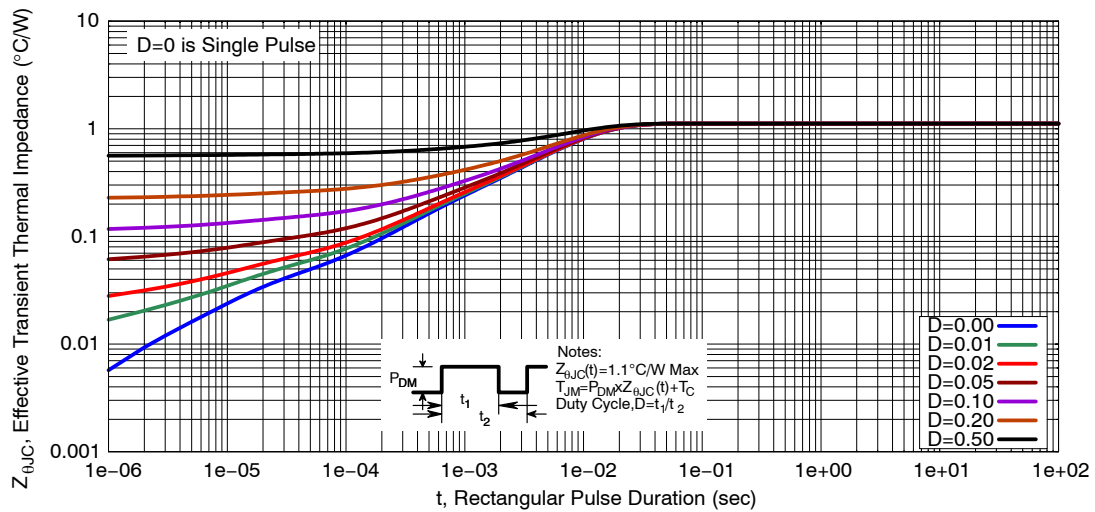


Figure 14. Transient Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSCHT2D6N08XTWG	7X	DFN8 4.9x5.8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

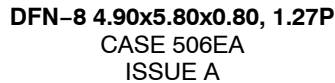
DUAL COOL is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

NTMFSCHT2D6N08X

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	10/2/2026

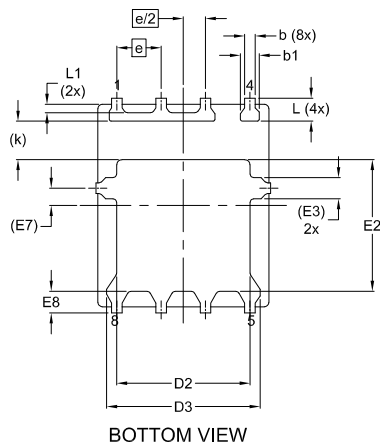




TOP VIEW

TOP VIEW

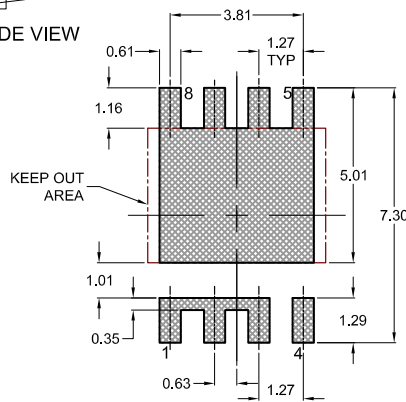
FRONT VIEW



BOTTOM VIEW

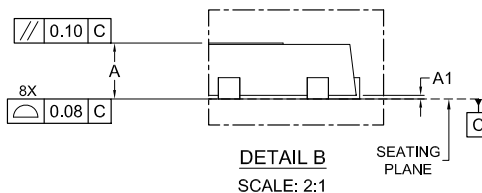
SEE DETAIL A

SIDE VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ONSEMI SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERM/D.



DETAIL B
SCALE: 2:1

SEATING

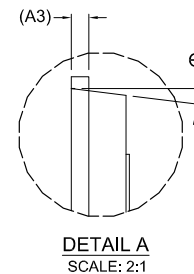
A diagram of a 16-pin connector. The connector is rectangular with a central rectangular cutout. On the right side, the text 'XXAYWZ' is printed vertically. On the left side, an arrow points to the first pin, which is labeled 'PIN 1'.

XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.80	0.85
A1	-	-	0.05
A3	0.25 REF		
b	0.21	0.31	0.41
b1	0.44	0.54	0.64
D	4.90	5.00	5.10
D1	4.90 BSC		
D2	3.72	3.82	3.92
D3	4.30	4.40	4.50
D4	2.75 REF		
D5	0.79 REF		
E	6.05	6.15	6.25
E1	5.80 BSC		
E2	3.67	3.77	3.87
E3	0.60 REF		
E4	3.85 REF		
E5	0.54 REF		
E6	0.60 REF		
E7	0.50 REF		
E8	0.52	0.62	0.72
e	1.27 BSC		
e/2	0.635BSC		
k	1.10 REF		
L	0.56	0.66	0.76
L1	0.15	0.25	0.35
Θ	0°	---	7°



DETAIL A
SCALE: 2:1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales