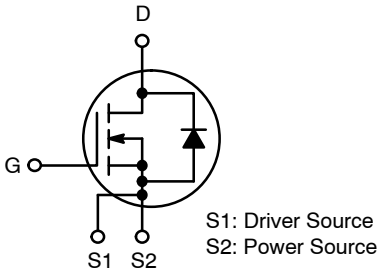
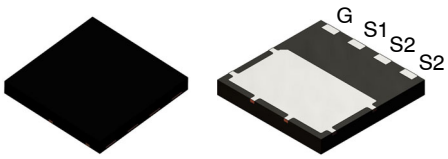
MOSFET - Power, Single, N-Channel, SUPERFET®, FAST, PQFN4
600 V, 100 mΩ, 27 A

NTMT100N60S5H

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	100 mΩ @ 10 V	27 A



N−Channel MOSFET



Power88
PQFN4 8x8, 2P
CASE 520AB

Description

The SUPERFET V MOSFET FAST series helps maximize system efficiency by the extremely low switching losses in hard switching application. The Power88 package which is an ultraslim SMD package offers excellent switching performance by providing kelvin source configuration and lower parasitic source inductance.

Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 80 mΩ
- 100% Avalanche Tested
- Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	600	V
Gate−to−Source Voltage	DC	V_{GS}	±30	V
	AC (f > 1 Hz)		±30	
Continuous Drain Current	T_C = 25°C	I_D	27	A
	T_C = 100°C		17	
Power Dissipation	T_C = 25°C	P_D	179	W
Pulsed Drain Current (Note 1)	T_C = 25°C	I_{DM}	95	A
Pulsed Source Current (Body Diode) (Note 1)		I_{SM}	95	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)		I_S	27	A
Single Pulse Avalanche Energy	I_L = 5.1 A, R_G = 25 Ω	E_{AS}	230	mJ
Avalanche Current		I_{AS}	5.1	A
Repetitive Avalanche Energy (Note 1)		E_{AR}	1.79	mJ
MOSFET dv/dt		dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)			20	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{SD} ≤ 13.5 A, di/dt ≤ 200 A/s, V_{DD} ≤ 400 V, starting T_J = 25°C.

MARKING DIAGRAM

NTMT100N60S5H = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTMT100N60S5H	PQFN4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case, Max.	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction−to−Ambient, Max.	$R_{\theta JA}$	45	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	600	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 10 mA, Referenced to 25°C	–	630	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 600 V, T_J = 25°C	–	–	1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 13.5 A, T_J = 25°C	–	80	100	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2.7 mA, T_J = 25°C	2.7	–	4.3	V
Forward Trans−conductance	g_{FS}	V_{DS} = 20 V, I_D = 13.5 A	–	26.8	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz	–	2616	–	pF
Output Capacitance	C_{OSS}		–	39.8	–	
Time Related Output Capacitance	$C_{OSS(tr)}$	I_D = Constant, V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	610	–	
Energy Related Output Capacitance	$C_{OSS(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	66.2	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 400 V, I_D = 13.5 A, V_{GS} = 10 V	–	46.6	–	nC
Gate−to−Source Charge	Q_{GS}		–	12.7	–	
Gate−to−Drain Charge	Q_{GD}		–	12.1	–	
Gate Resistance	R_G	f = 1 MHz	–	1.16	–	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 0/10 V, V_{DD} = 400 V, I_D = 13.5 A, R_G = 4.7 Ω	–	21.6	–	ns
Rise Time	t_r		–	5.81	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	61.1	–	
Fall Time	t_f		–	2.64	–	
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 13.5 A, T_J = 25°C	–	–	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_{SD} = 13.5 A, dI/dt = 100 A/μs, V_{DD} = 400 V	–	362	–	ns
Reverse Recovery Charge	Q_{RR}		–	5331	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

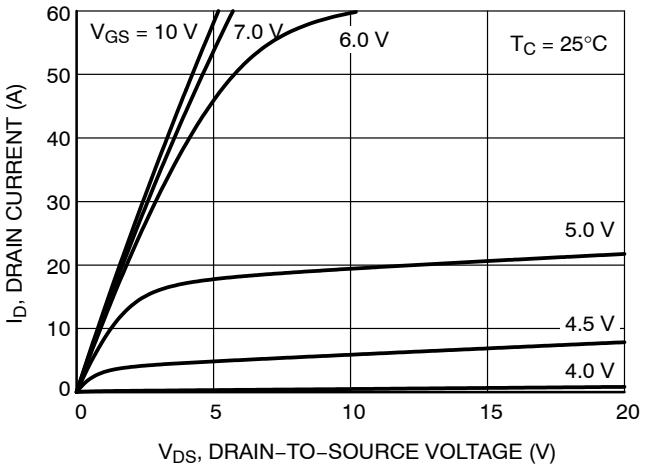


Figure 1. On−Region Characteristics

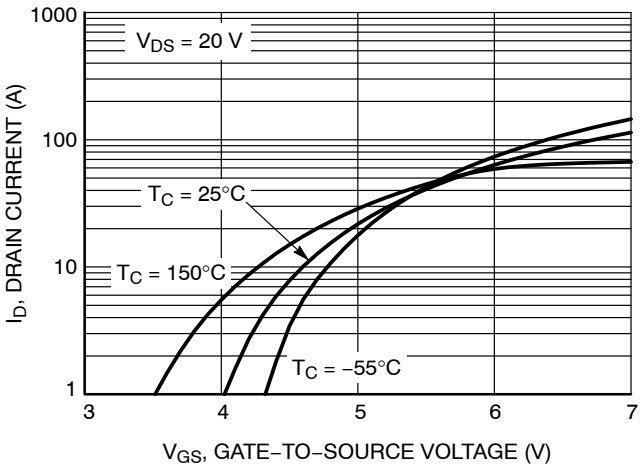


Figure 2. Transfer Characteristics

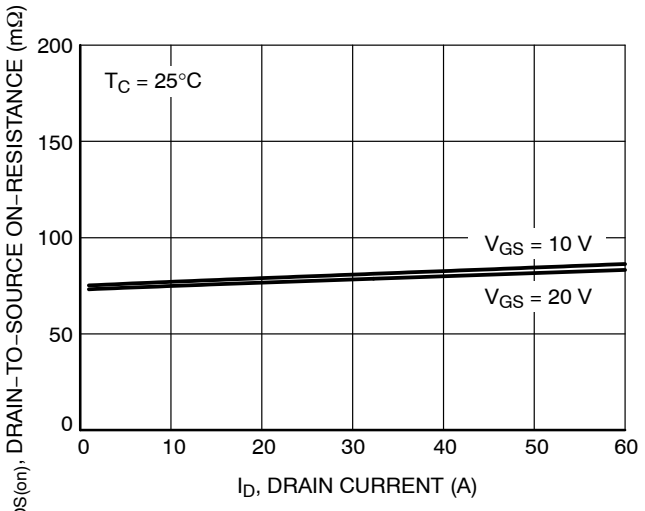


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

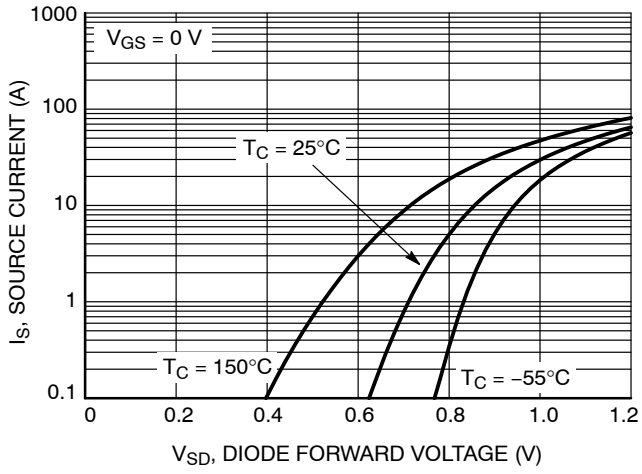


Figure 4. Diode Forward Voltage vs. Source Current

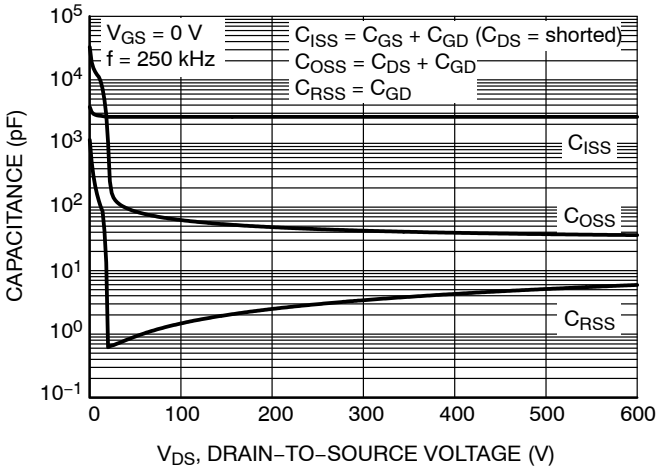


Figure 5. Capacitance Characteristics

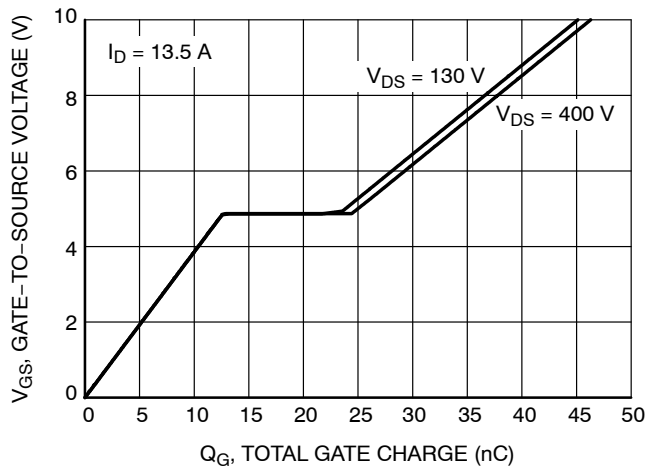


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

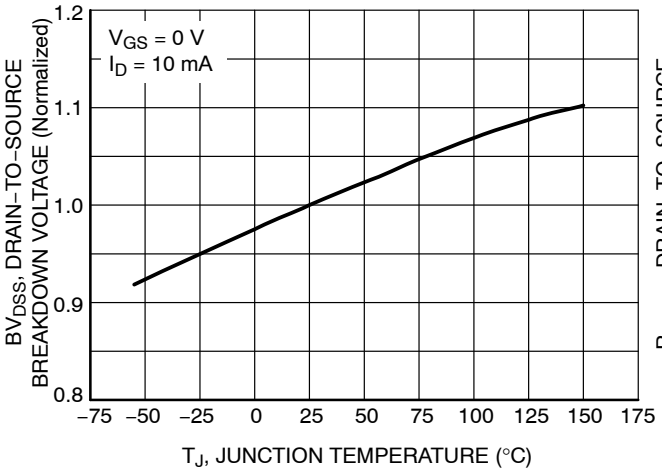


Figure 7. Breakdown Voltage Variation vs. Temperature

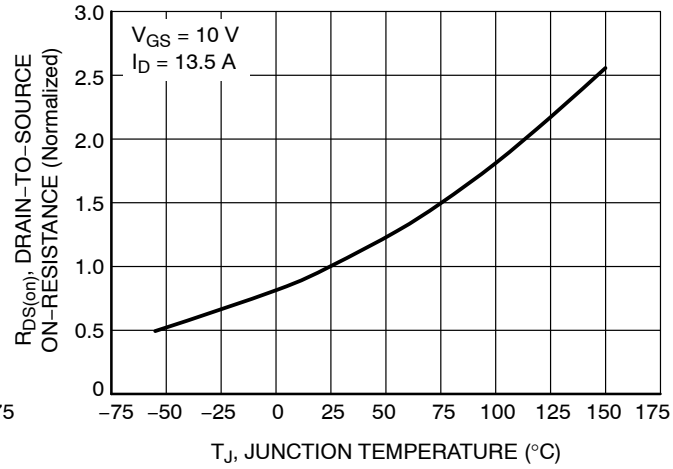


Figure 8. On−Resistance Variation vs. Temperature

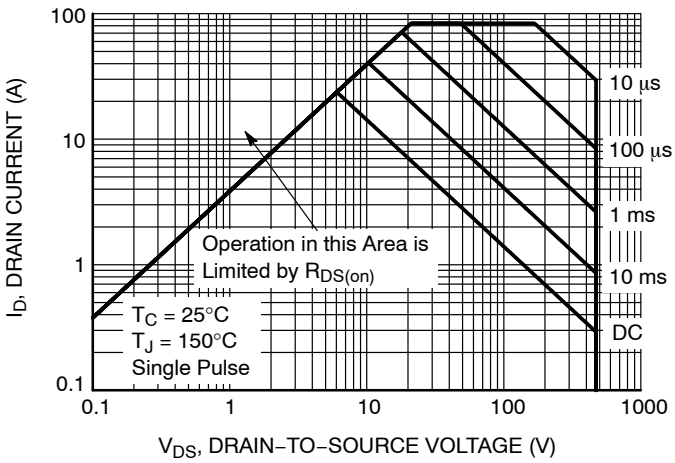


Figure 9. Maximum Safe Operating Area

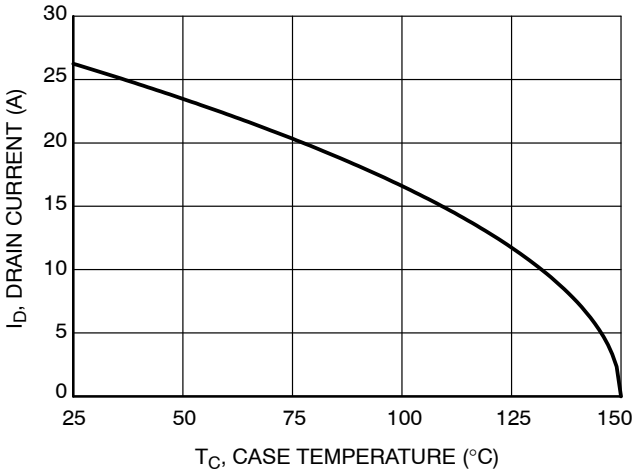


Figure 10. Maximum Drain Current vs. Case Temperature

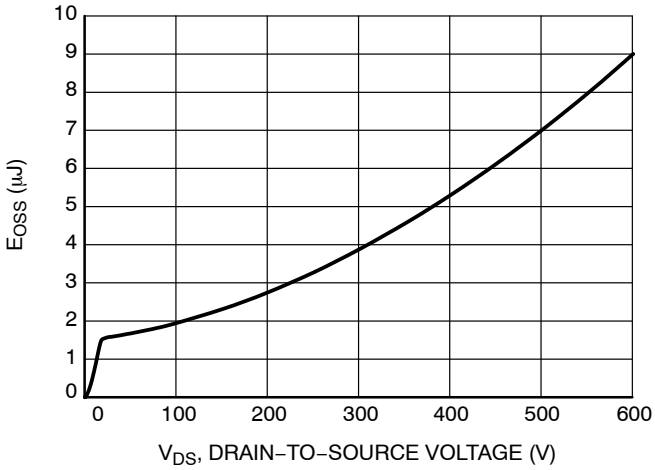


Figure 11. E_{OSS} vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

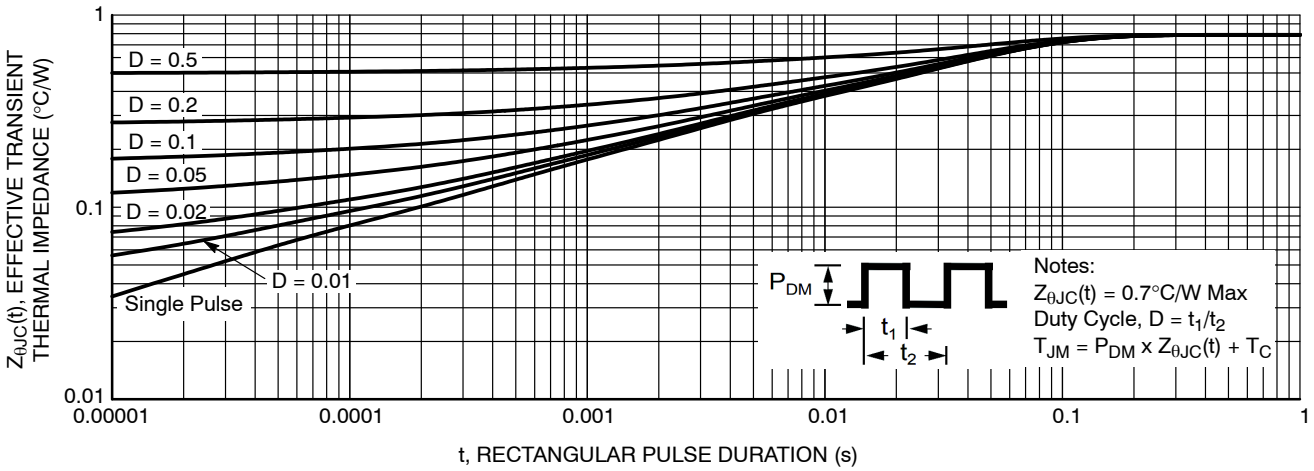


Figure 12. Transient Thermal Impedance

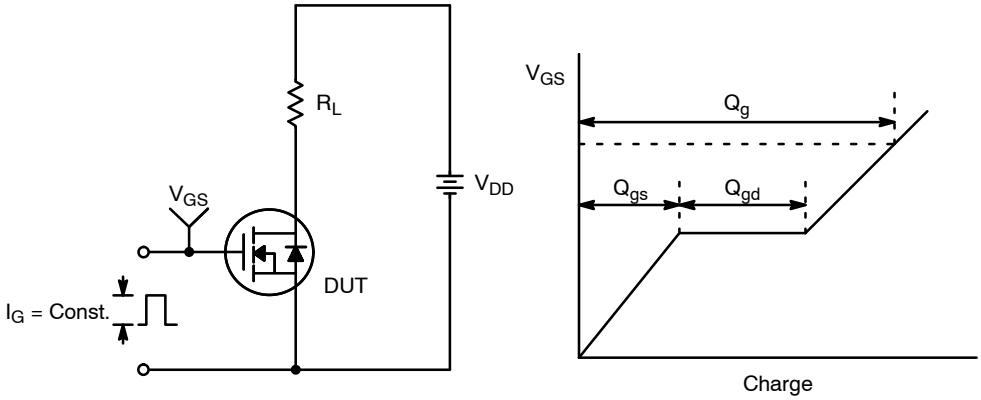


Figure 13. Gate Charge Test Circuit & Waveform

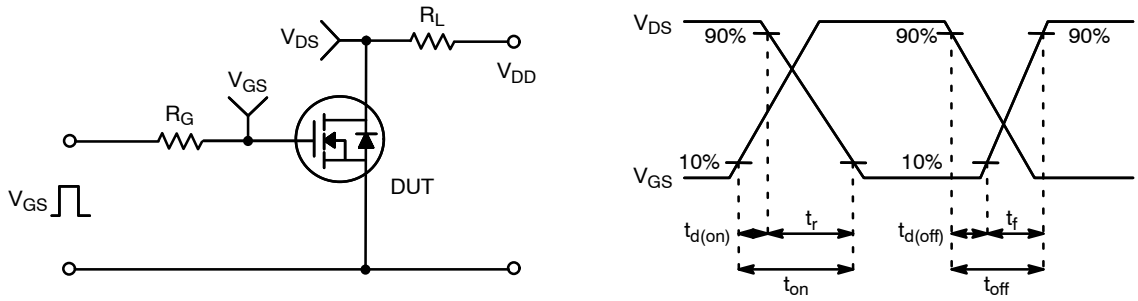


Figure 14. Resistive Switching Test Circuit & Waveforms

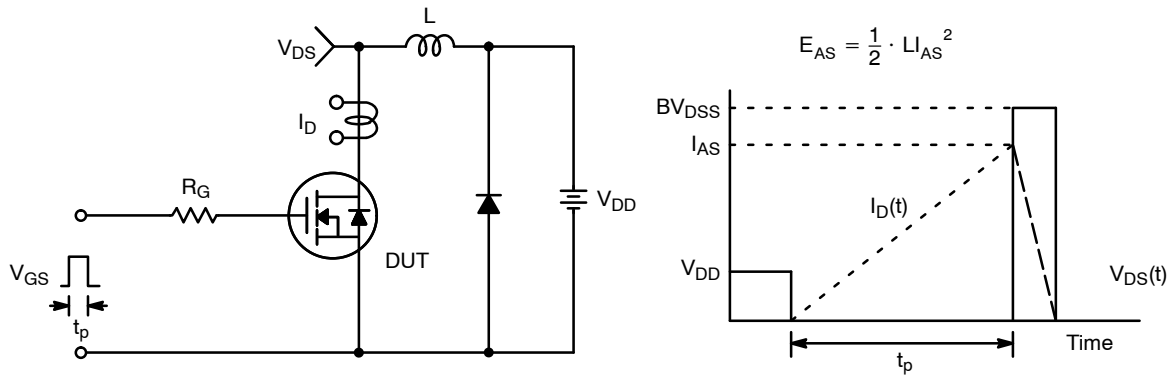


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

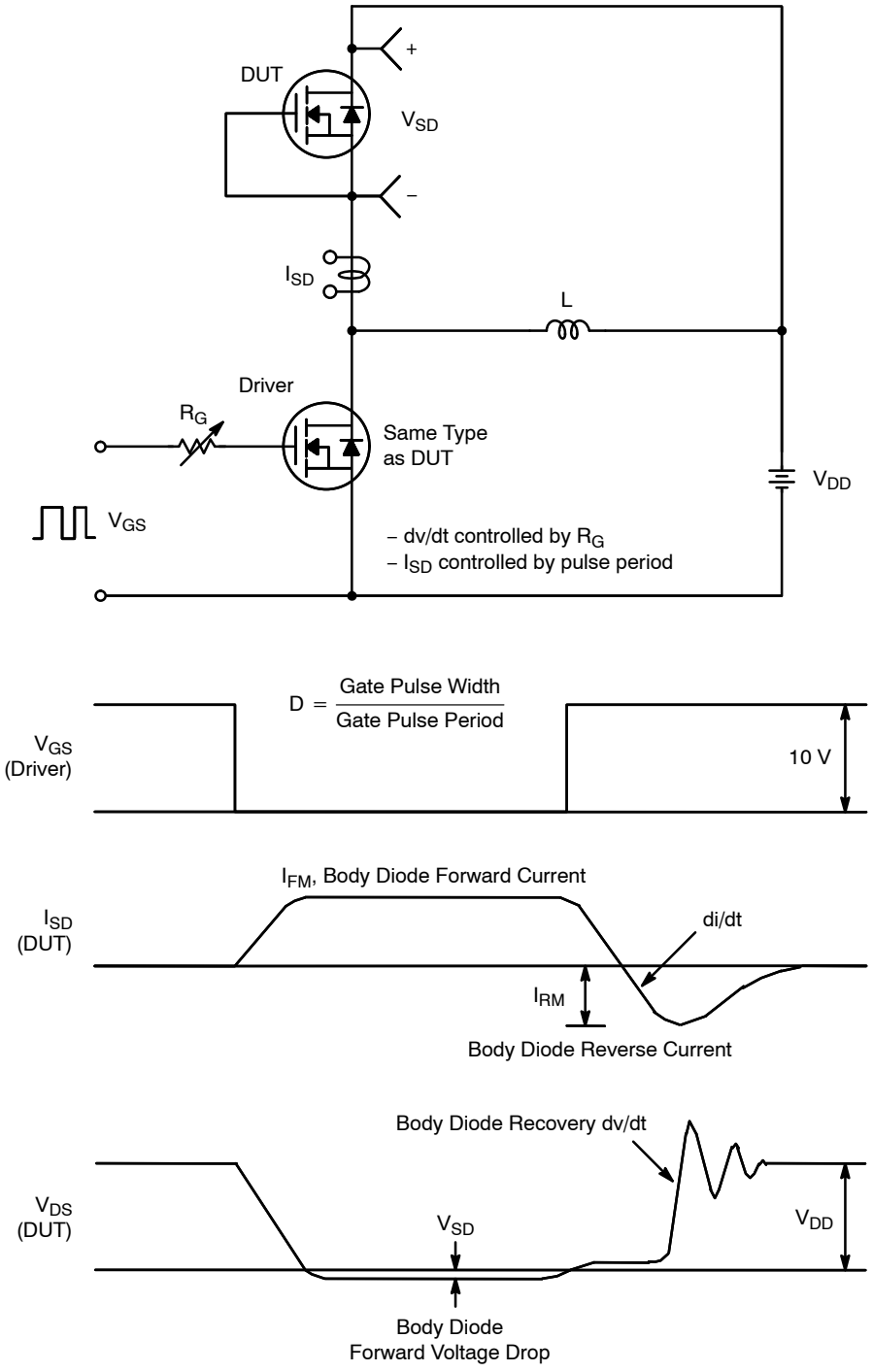
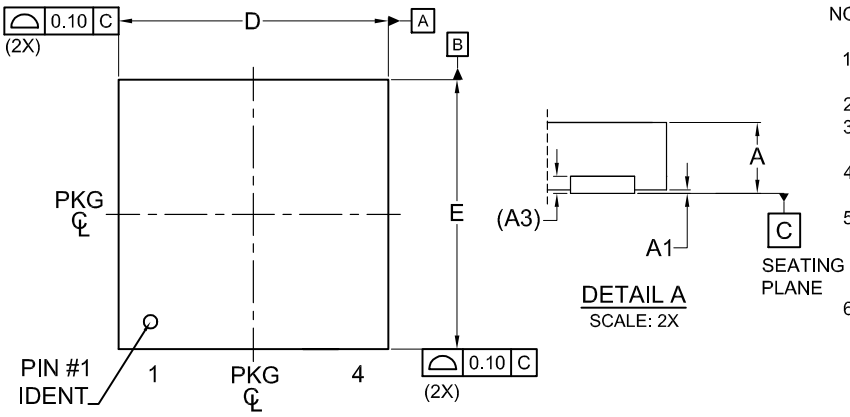


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

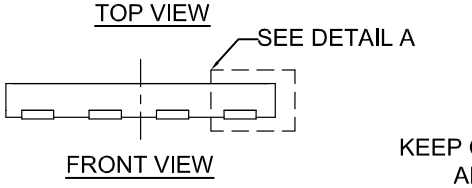
PACKAGE DIMENSIONS

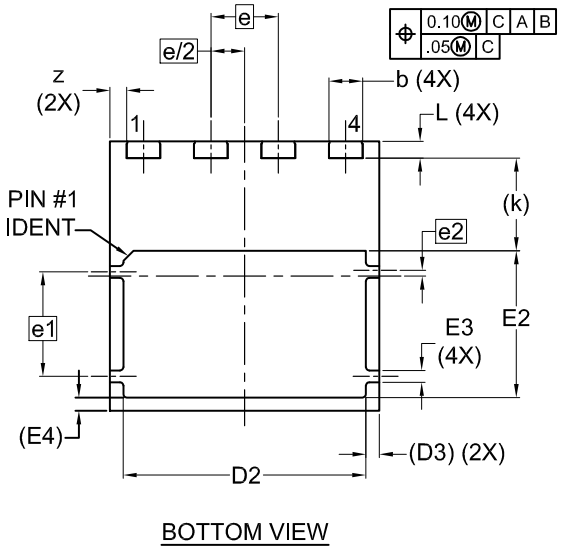
PQFN4 8X8, 2P
CASE 483AP
ISSUE A

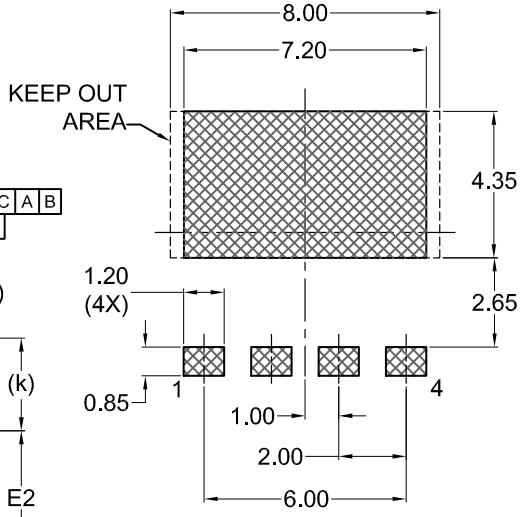


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.







*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	7.10	7.20	7.30
D3	0.40 REF		
E	7.90	8.00	8.10
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4	0.40 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	3.10 BSC		
e2	0.17 BSC		
k	2.75 REF		
L	0.40	0.50	0.60

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