MOSFET - Power, Single N-Channel, STD Gate, TCPAK1012

80 V, 0.79 mΩ, 643 A

NVBYST0D8N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	0.79 mΩ @ V_{GS} = 10 V	643 A

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
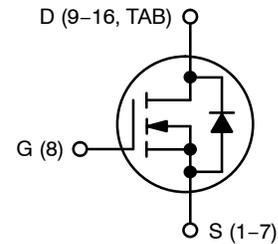- Motor Drives
- Automotive 48V System

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

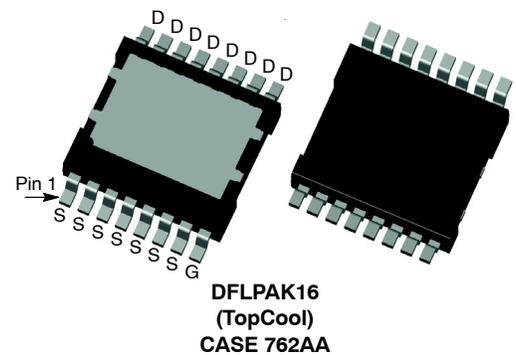| Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	643	A
	T_C = 100 °C		455	
Power Dissipation	T_C = 25 °C	P_D	652	W
Pulsed Drain Current	T_C = 25 °C t_p = 100 μs	I_{DM}	1976	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to +175	°C
Continuous Source-Drain Current (Body Diode)		I_S	1097	A
Single Pulse Avalanche Energy (I_{PK} = 132 A)		E_{AS}	871	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Surface-mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. EAS is based on started T_J = 25 °C, rated IAS, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

D (9–16, TAB)

G (8)

S (1–7)

N-CHANNEL MOSFET

D D D D D D D

Pin 1

S S S S S S S G

DFLPAK16 (TopCool) CASE 762AA

MARKING DIAGRAM

0D8N08X AYWZZ

0D8N08X = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVBYST0D8N08X	TCPAK1012	1500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JC}$	0.23	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	38	
Thermal Characterization Parameter, Junction-to-Source Lead (Pin 1–7)*	Ψ_{JL}	3.9	
Thermal Characterization Parameter, Junction-to-Drain Lead (Pin 9–16)*	Ψ_{JL}	3.3	

* Low thermal conductivity test boards compliant with JEDEC Standard 51-3 for leaded surface-mount packages. 1s0p PCB board with a 1 in^2 copper plane, tested under natural convection conditions.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C	–	37	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C	–	–	2	μA
		V_{DS} = 80 V, T_J = 125 °C	–	–	250	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 80 A, T_J = 25 °C	–	0.67	0.79	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 703 μA, T_J = 25 °C	2.4	–	3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 703 μA	–	–7.5	–	mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 80 A	–	324	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	13097	–	pF
Output Capacitance	C_{OSS}		–	3744	–	
Reverse Transfer Capacitance	C_{RSS}		–	56	–	
Output Charge	Q_{OSS}		–	268	–	nC
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V	–	182	–	
Threshold Gate Charge	$Q_{G(TH)}$		–	40	–	
Gate-to-Source Charge	Q_{GS}		–	59	–	
Gate-to-Drain Charge	Q_{GD}		–	28	–	
Gate Plateau Voltage	V_{GP}		–	4.6	–	V
Gate Resistance	R_G	f = 1 MHz	–	0.26	–	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 80 A, R_G = 2.5 Ω	–	50	–	ns
Rise Time	t_r		–	16	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	86	–	
Fall Time	t_f		–	14	–	
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 80 A, V_{GS} = 0 V, T_J = 25 °C	–	0.79	1.2	V
		I_S = 80 A, V_{GS} = 0 V, T_J = 125 °C	–	0.63	–	

NVBYST0D8N08X

ELECTRICAL CHARACTERISTICS (T$_J$ = 25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t$_{RR}$	V$_{GS}$ = 0 V, I$_S$ = 80 A, dI/dt = 1000 A/μs, V$_{DD}$ = 64 V	–	55	–	ns
Charge Time	t$_a$		–	28	–	
Discharge Time	t$_b$		–	27	–	
Reverse Recovery Charge	Q$_{RR}$		–	609	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS
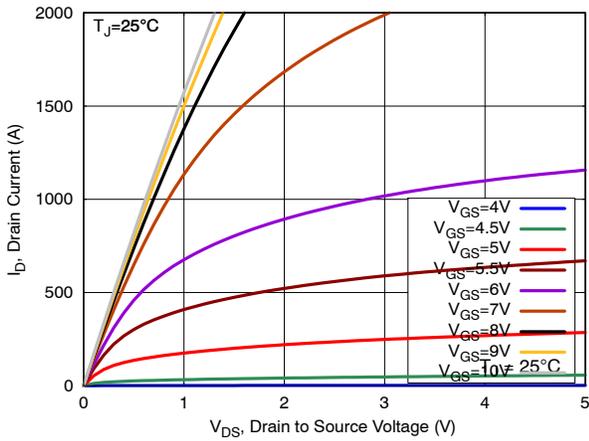
Figure 1. On-Region Characteristics
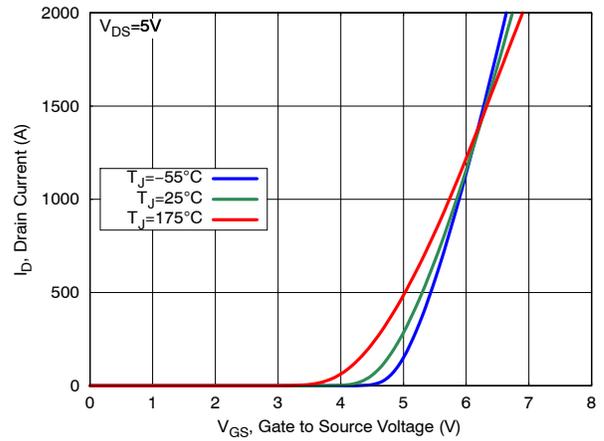
Figure 2. Transfer Characteristics
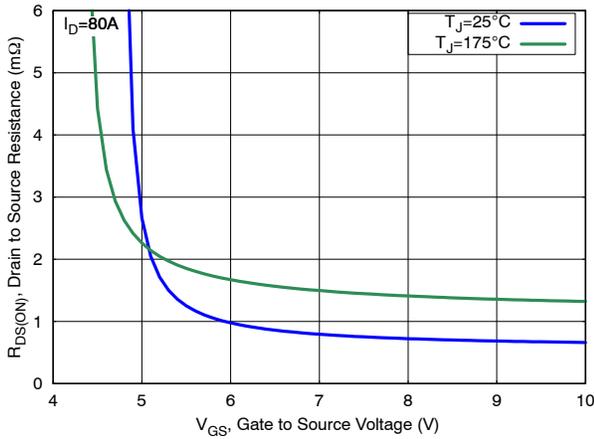
Figure 3. On-Resistance vs. Gate Voltage
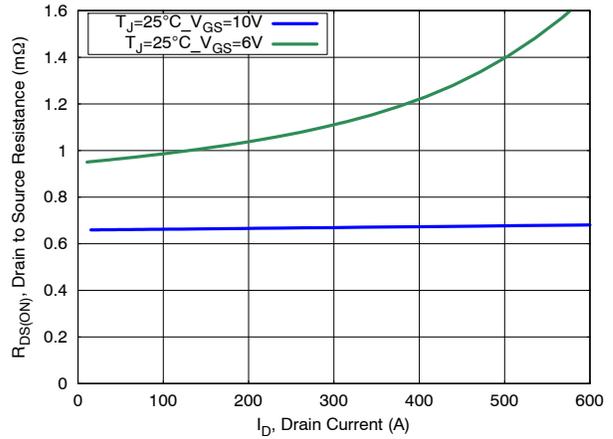
Figure 4. On-Resistance vs. Drain Current
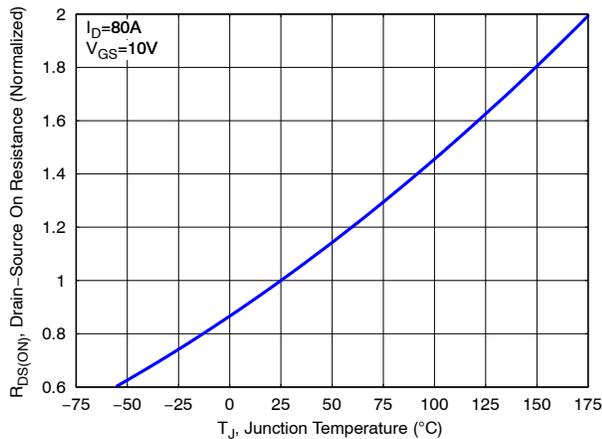
Figure 5. Normalized ON Resistance vs. Junction Temperature
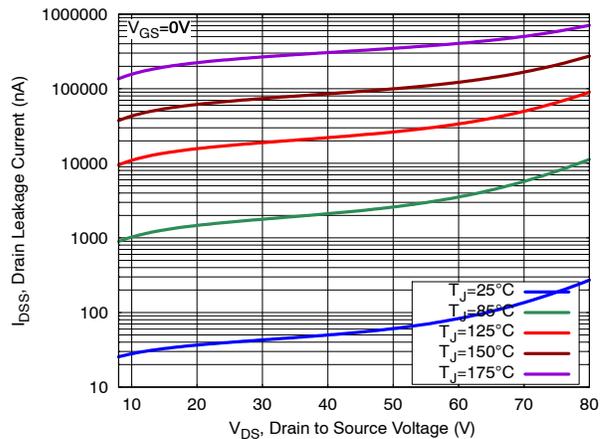
Figure 6. Drain Leakage Current vs Drain Voltage

TYPICAL CHARACTERISTICS
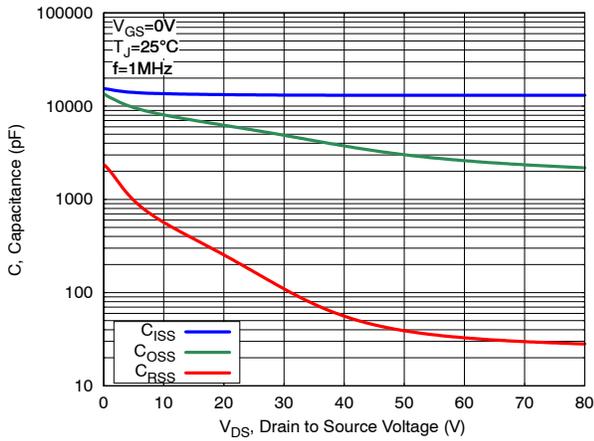
Figure 7. Capacitance Characteristics
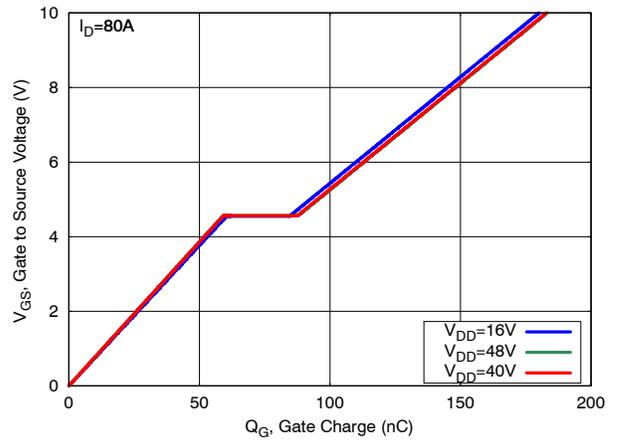
Figure 8. Gate Charge Characteristics
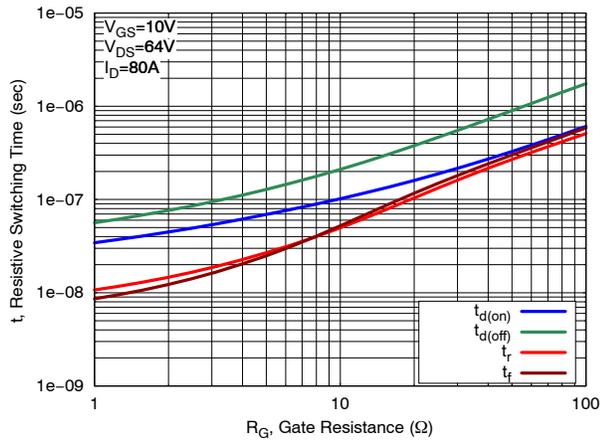
Figure 9. Resistive Switching Time Variation vs. Gate Resistance
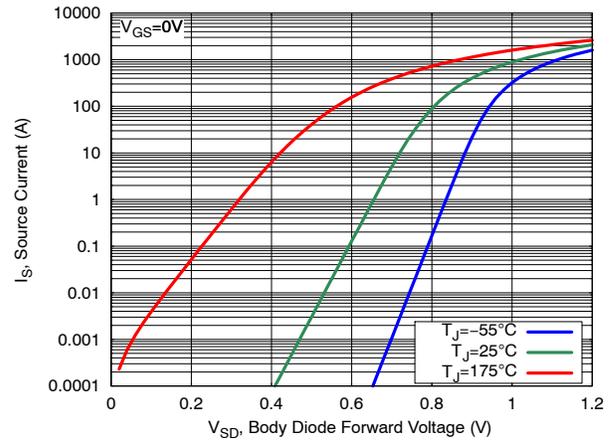
Figure 10. Diode Forward Characteristics
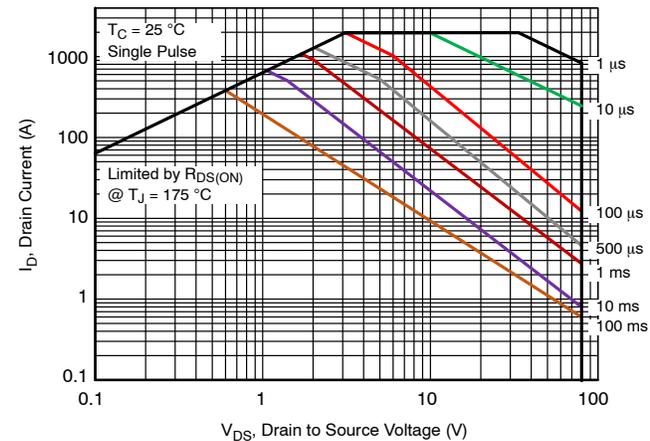
Figure 11. Safe Operating Area (SOA)
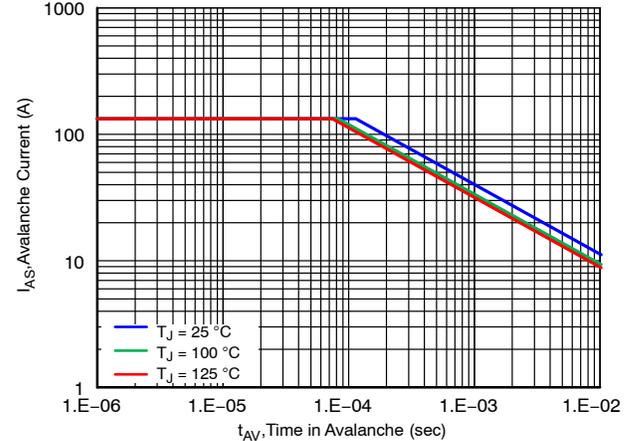
Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS
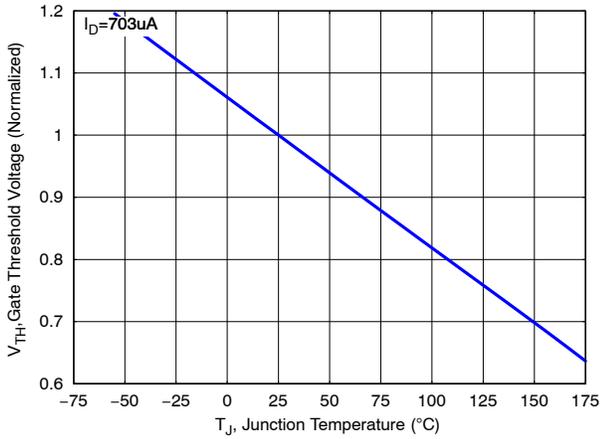
Figure 13. Gate Threshold Voltage vs Junction Temperature
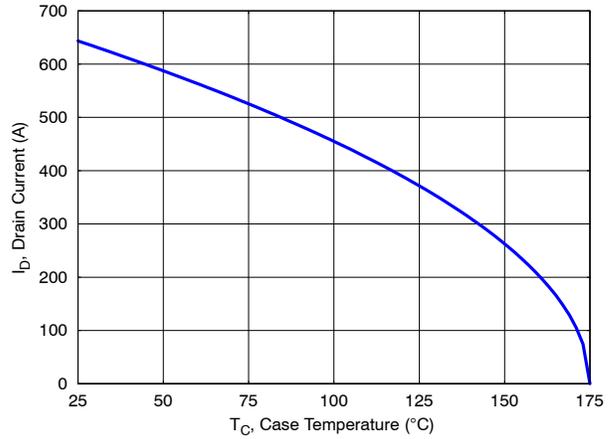
Figure 14. Maximum Current vs. Case Temperature
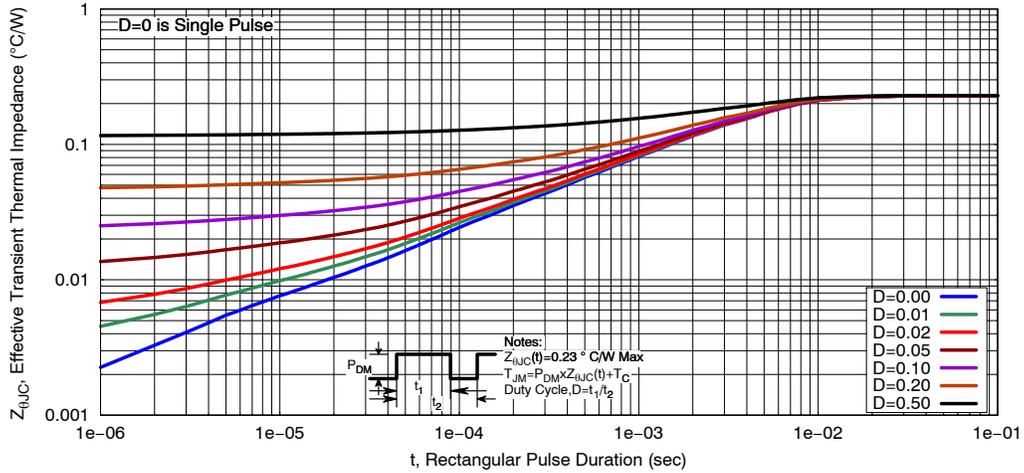
Figure 15. Transient Thermal Response

REVISION HISTORY

Revision	Description of Changes	Date
0	Thermal characteristics update. Maximum power & drain current update. Switching curve update. FBSOA & UIS update. BVDSS temp. coefficient update.	08/21/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

PACKAGE DIMENSIONS

TCPAK16 8.80x10.10, 1.20P (TCPAK1012)
CASE 762AA
ISSUE E

DATE 23 MAY 2025

TOP VIEW

SIDE VIEW

DETAIL 'A'
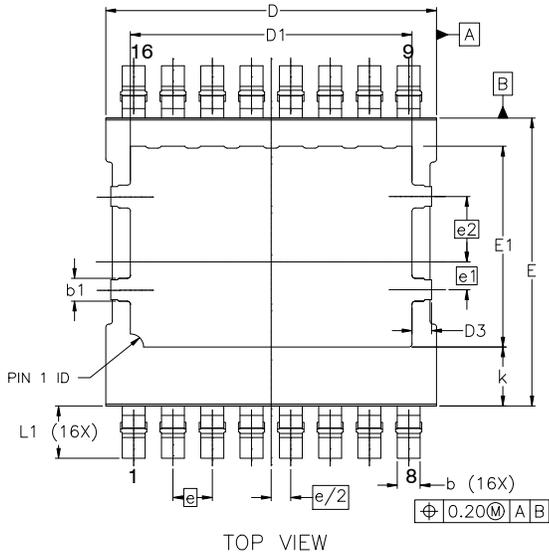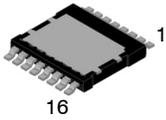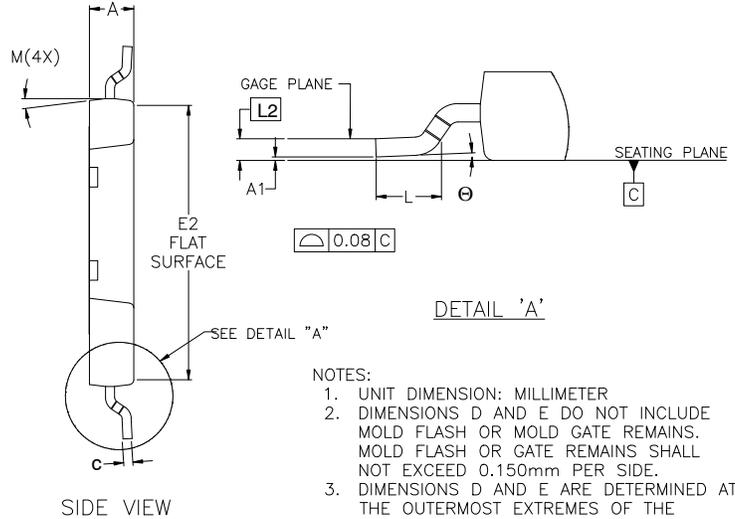
NOTES:
1. UNIT DIMENSION: MILLIMETER
2. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR MOLD GATE REMAINS. MOLD FLASH OR GATE REMAINS SHALL NOT EXCEED 0.150mm PER SIDE.
3. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4. CENTER PAD IS FOR PKG MECHANICAL SUPPORT ONLY. NO SOLDERING REQUIRED.
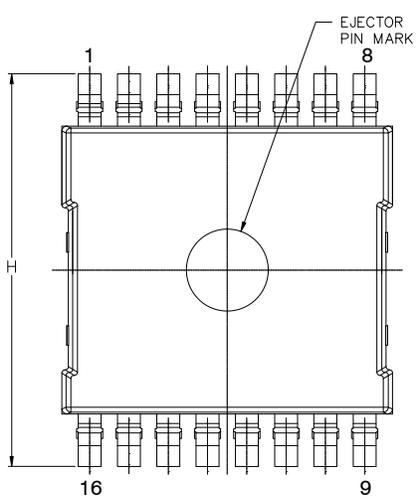
BOTTOM VIEW
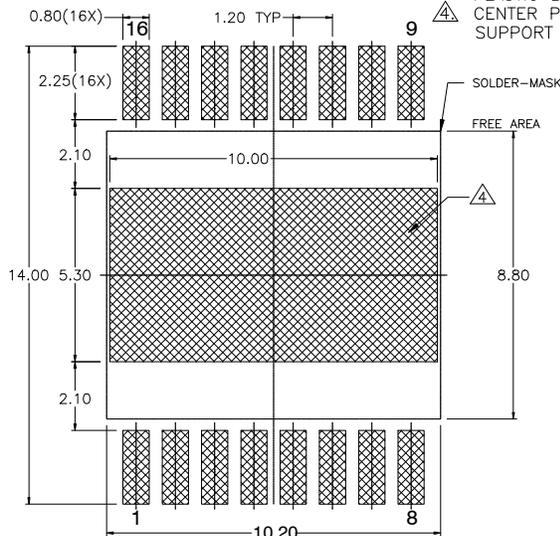
LAND PATTERN RECOMMENDATION

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.30	1.35	1.40
A1	0.00	0.05	0.10
b	0.67	0.72	0.77
b1	0.65	0.70	0.75
c	0.21	0.26	0.31
D	10.00	10.10	10.20
D1	8.50	8.60	8.70
D3	0.55	0.60	0.75
E	8.70	8.80	8.90
E1	6.04	6.14	6.24
E2	---	---	8.70
e	1.20 BSC		
e/2	0.60 BSC		
e1	0.85 BSC		
e2	2.00 BSC		
k	1.70	1.80	1.90
H	11.80	12.00	12.20
L	0.80	1.00	1.20
L1	1.40	1.60	1.80
L2	0.30 BSC		
Θ	−	2.5°	5°

GENERIC MARKING DIAGRAM*

XXXXXXXXXX AYWZZ
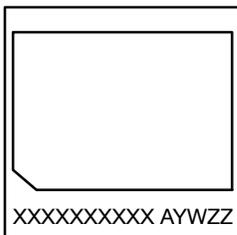
XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NVBYST0D8N08X

ADDITIONAL INFORMATION

◊