

# MOSFET – Power, N-Channel

80 V, 1.0 mΩ

## NVCW4LS001N08HA



### Features

- Typical  $R_{DS(on)}$  = 0.82 mΩ at  $V_{GS} = 10$  V
- Typical  $Q_{g(tot)}$  = 166 nC at  $V_{GS} = 10$  V
- AEC-Q101 Qualified
- RoHS Compliant

### DIMENSION (μm)

Die Size	6604 x 4445
Scribe Width	80
Source Attach Area	(6362 x 2059) x 2
Gate Attach Area	330 x 600
Die Thickness	101.6

Gate and Source : AlCu  
 Drain : Ti-Ni-Ag (back side of die)  
 Passivation : Polyimide  
 Wafer Diameter : 8 inch  
 Wafer Unsawn on UV Tape  
 Bad dice identified in Inking  
 Gross Die Count : 806

### ORDERING INFORMATION

Device	Package
NVCW4LS001N08HA	Unsawn Wafer on Ring Frame

### RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40% to 66%

### ELECTRICAL CHARACTERISTICS

The Chip is 100% Probed to Meet the Conditions and Limits Specified at  $T_J = 25^\circ\text{C}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$ V	80	–	–	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 80$ V, $V_{GS} = 0$ V	–	–	10	μA
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = 20$ V, $V_{DS} = 0$ V	–	–	100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 650 \mu\text{A}$	2.0	–	4.0	V
* $R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 50$ A, $V_{GS} = 10$ V	–	0.82	1.0	mΩ

\*Accurate  $R_{DS(on)}$  test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max  $R_{DS(on)}$  specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die  $R_{DS(on)}$  performance depends on the Source wire/ribbon bonding layout.

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## ABSOLUTE MAXIMUM RATINGS

in Reference to the NVBLS1D1N08H electrical data in TOLL (  $T_J = 25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DSS}$	Drain to Source Voltage	80	V	
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Note 1, 2)	$T_C = 25^{\circ}\text{C}$	351	A
		$T_C = 100^{\circ}\text{C}$	248	A
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^{\circ}\text{C}$	311	W
		$T_C = 100^{\circ}\text{C}$	156	W
$E_{AS}$	Single Pulse Avalanche Energy ( $I_{L(pk)} = 31.9\text{ A}$ )	1580	mJ	
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^{\circ}\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case Steady State	0.48	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Steady State (Note 3)	35.8	$^{\circ}\text{C}/\text{W}$

3. Surface-mounted on FR4 board using a  $650\text{ mm}^2$ , 2 oz. Cu pad.

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## ELECTRICAL CHARACTERISTICS

in Reference to the NVBLS1D1N08H electrical data in TOLL (  $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80	–	–	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$	–	–	100	nA

### ON CHARACTERISTICS (Note 4)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 650 \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Drain to Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	–	0.92	1.05	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 50 \text{ A}$	–	213	–	S

### CHARGES, CAPACITANCE

$C_{iss}$	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	–	11200	–	pF
$C_{oss}$	Output Capacitance		–	1600	–	pF
$C_{rss}$	Reverse Transfer Capacitance		–	49	–	pF
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 10 \text{ V}, V_{DS} = 64 \text{ V}, I_D = 50 \text{ A}$	–	166	–	nC
$Q_{g(th)}$	Threshold Gate Charge		–	29	–	nC
$Q_{gs}$	Gate to Source Gate Charge		–	44	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	35	–	nC

### SWITCHING CHARACTERISTICS (Note 5)

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 64 \text{ V}, I_D = 50 \text{ A}, V_{GS} = 10 \text{ V},$ $R_G = 6 \Omega$	–	45	–	ns
$t_r$	Rise Time		–	43	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	141	–	ns
$t_f$	Fall Time		–	43	–	ns

### DRAIN – SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Voltage	$I_S = 50 \text{ A}, V_{GS} = 0 \text{ V}$	–	–	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S = 50 \text{ A}, V_{GS} = 0 \text{ V}, dl_S/dt = 100 \text{ A}/\mu\text{s}$	–	92	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	234	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

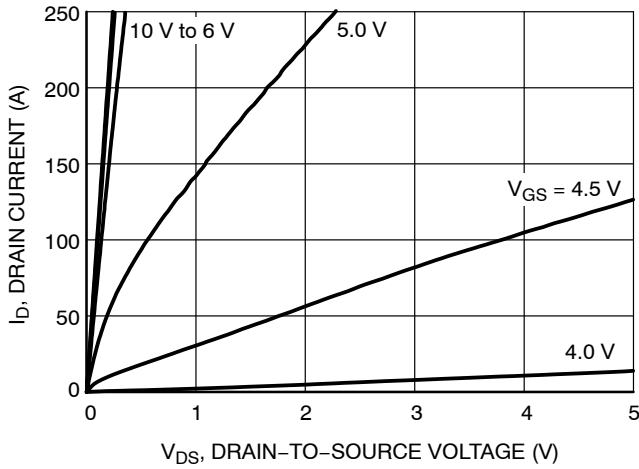


Figure 1. On-Region Characteristics

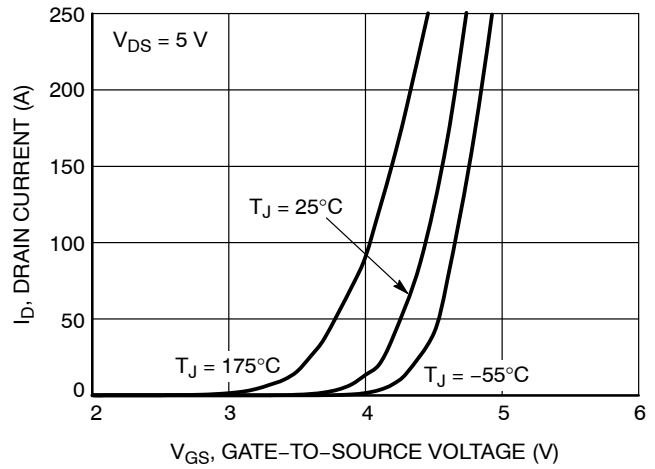


Figure 2. Transfer Characteristics

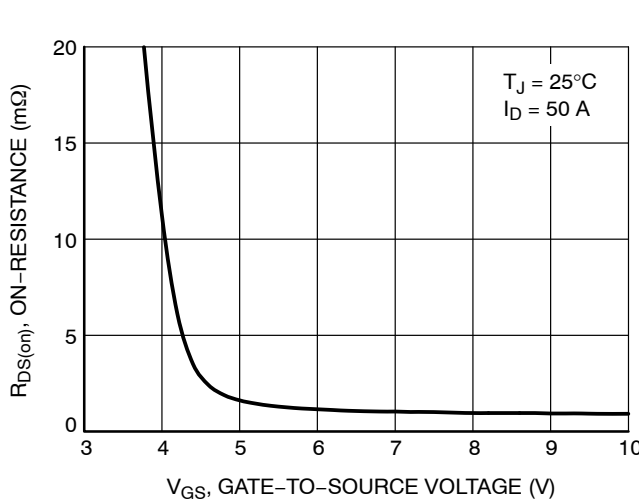


Figure 3. On-Resistance vs. Gate-to-Source Voltage

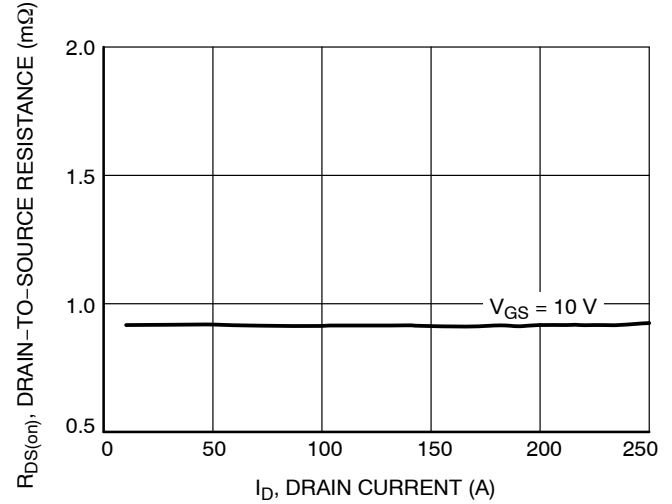


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

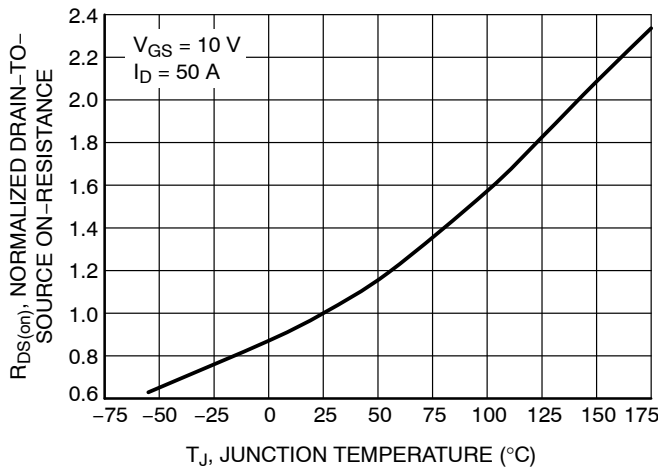


Figure 5. On-Resistance Variation with Temperature

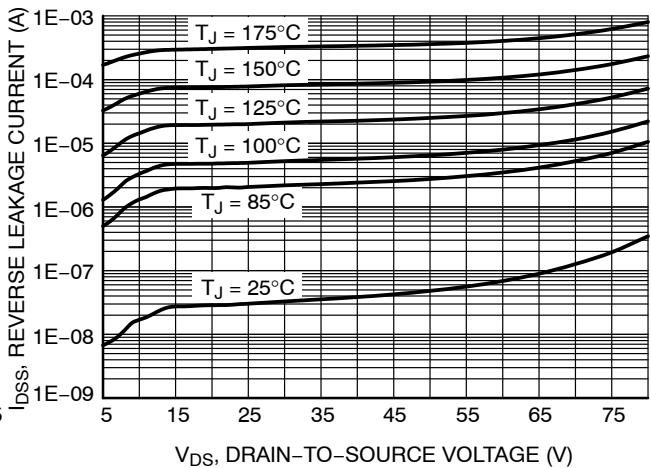
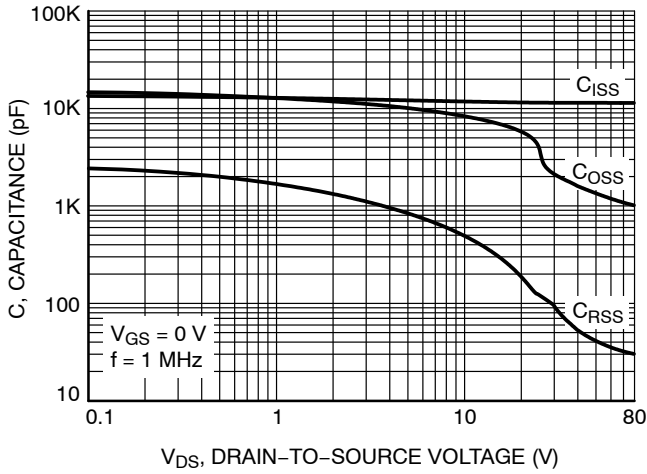


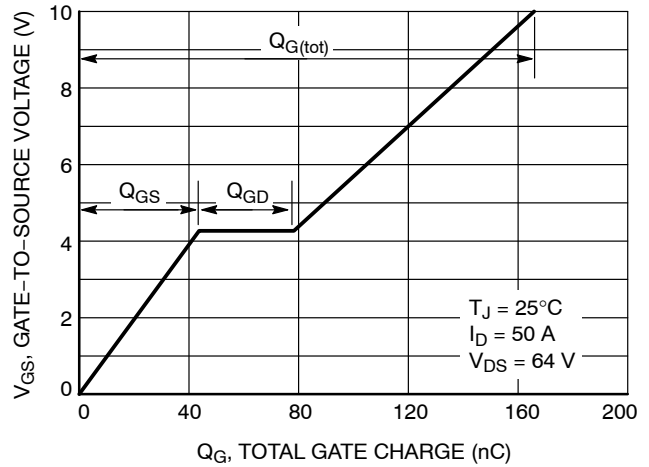
Figure 6. Drain-to-Source Leakage Current vs. Voltage

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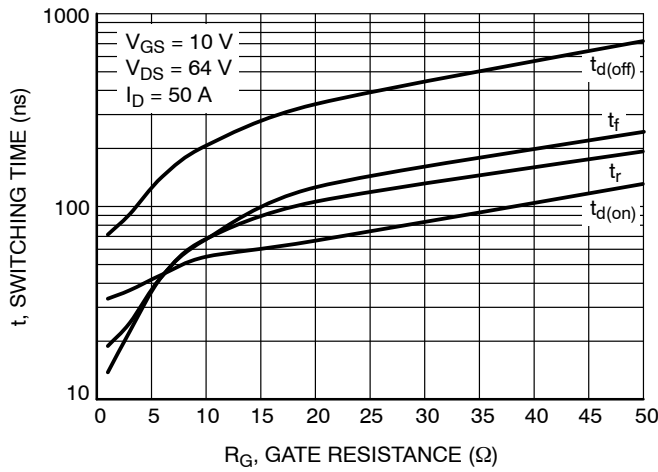
## TYPICAL CHARACTERISTICS



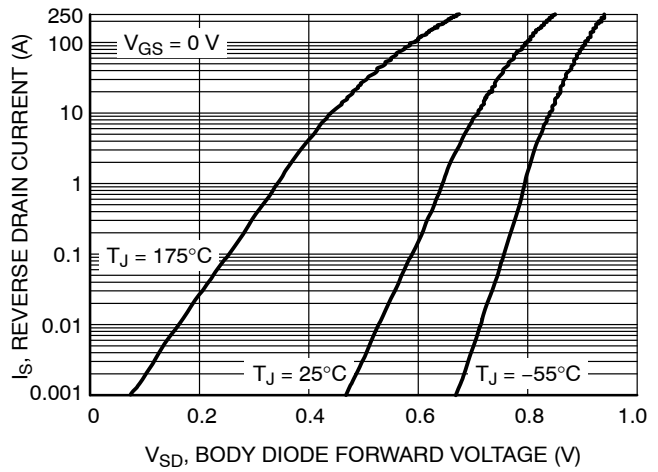
**Figure 7. Capacitance Variation**



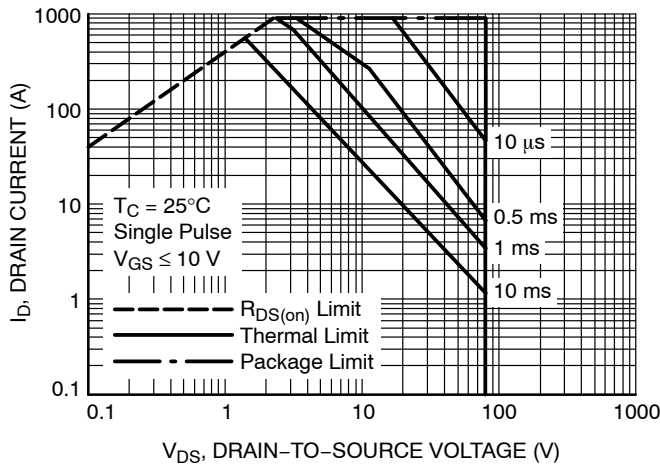
**Figure 8. Gate-to-Source Voltage vs. Total Charge**



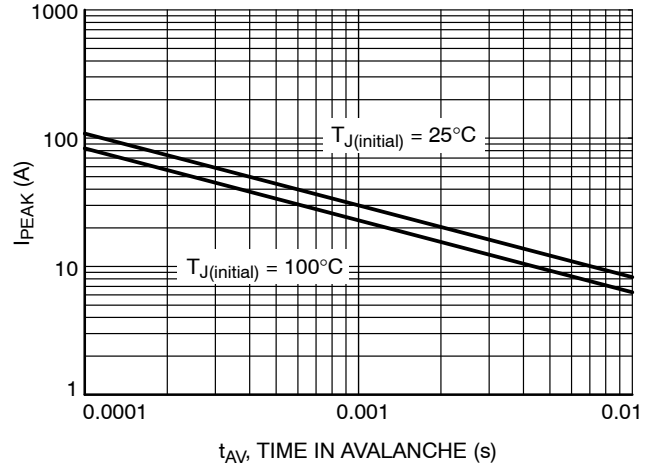
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Drain Current vs. Time in Avalanche**

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## TYPICAL CHARACTERISTICS

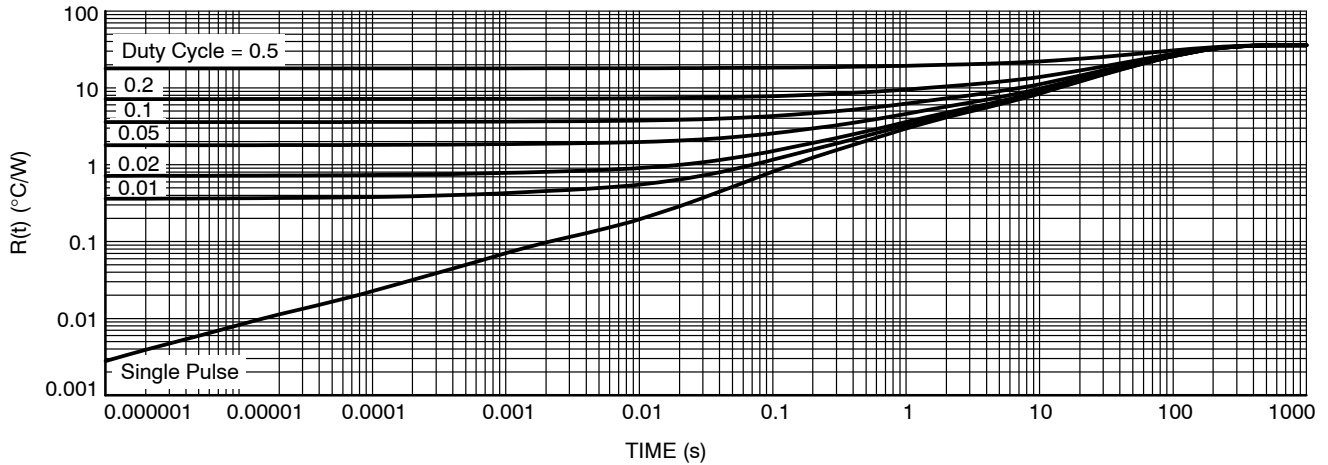


Figure 13. Transient Thermal Impedance

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