

MOSFET – Power, N-Channel, SUPERFET® III, Easy Drive

650 V, 360 mΩ, 10 A

NVD360N65S3

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on) max.} \times Q_g typ. \& R_{DS(on) max.} \times E_{OSS}$)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage – DC	V_{GSS}	± 30	V
Gate-to-Source Voltage – AC ($f > 1$ Hz)	V_{GSS}	± 30	V
Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	I_D	10	A
Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	I_D	6	A
Drain Current – Pulsed (Note 3)	I_{DM}	25	A
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	83	W
Power Dissipation – Derate Above 25°C	P_D	0.67	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	40	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	0.83	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	20	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	T_L	300	$^\circ\text{C}$

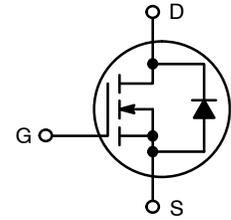
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	1.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2, 6)	$R_{\theta JA}$	52	$^\circ\text{C}/\text{W}$

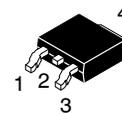
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse-width limited by maximum junction temperature.
4. $I_{AS} = 2.1$ A, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
5. $I_{SD} = 5$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq 400$ V, starting $T_J = 25^\circ\text{C}$.
6. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

V_{DSS}	$R_{DS(ON) MAX}$	$I_D MAX$
650 V	360 mΩ @ 10 V	10 A

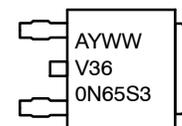


POWER MOSFET



DPAK
CASE 369C

MARKING DIAGRAM



- A = Assembly Location
Y = Year
WW = Work Week
V360N65S3 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVD360N65S3	DPAK3 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVD360N65S3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D = 1 mA, Referenced to 25°C		650		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{DS} = 520 V, T _C = 125°C		0.33		
Gate-to-Body Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 0.2 mA	2.5		4.5	V
Threshold Temperature Coefficient	ΔV _{GS(th)} /ΔT _J	V _{GS} = V _{DS} , I _D = 0.2 mA		-8.8		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		314	360	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 20 V, I _D = 5 A		6		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 400 V, f = 1 MHz		756		pF
Output Capacitance	C _{oss}			17.4		
Reverse Transfer Capacitance	C _{rss}			1.53		
Effective Output Capacitance	C _{oss(eff.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		179		pF
Energy Related Output Capacitance	C _{oss(er.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		29.3		pF
Total Gate Charge at 10 V	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 400 V, I _D = 5 A (Note 7)		16.8		nC
Threshold Gate Charge	Q _{G(TH)}			2.8		
Gate-to-Source Gate Charge	Q _{GS}			4.6		
Gate-to-Drain "Miller" Charge	Q _{GD}			7		
Equivalent Series Resistance	ESR	f = 1 MHz		1		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 400 V, I _D = 5 A, R _g = 4.7 Ω (Note 7)		13.6		ns
Turn-On Rise Time	t _r			9.44		ns
Turn-Off Delay Time	t _{d(off)}			33.9		ns
Turn-Off Fall Time	t _f			11.2		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

Maximum Continuous Source-to-Drain Diode Forward Current	I _S	V _{GS} = 0 V			10	A
Maximum Pulsed Source-to-Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			25	A
Source-to-Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 5 A			1.2	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μs, I _{SD} = 5 A		197		ns
Charge Time	t _a			18		
Discharge Time	t _b			10		
Reverse Recovery Charge	Q _{rr}			2089		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Essentially independent of operating temperature typical characteristics.

NVD360N65S3

TYPICAL CHARACTERISTICS

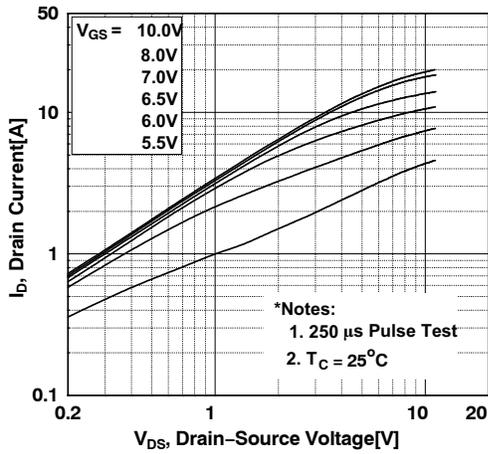


Figure 1. On-Region Characteristics 25°C

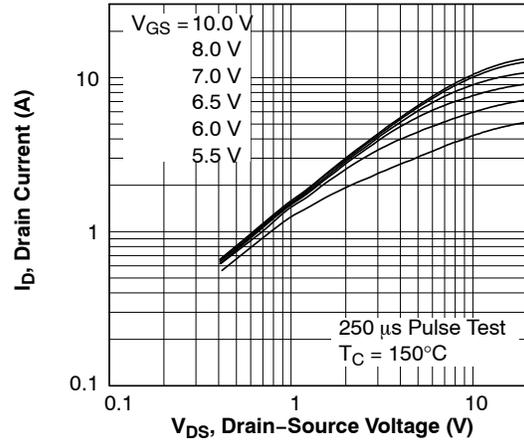


Figure 2. On-Region Characteristics 150°C

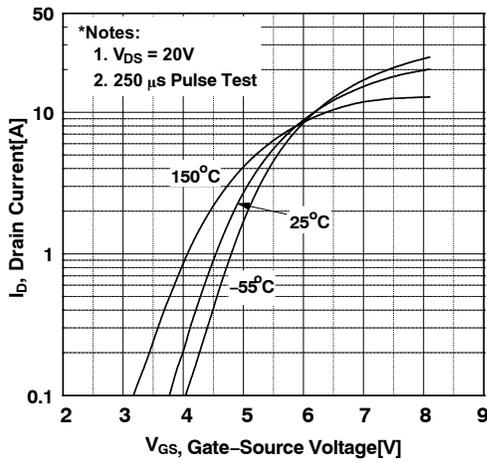


Figure 3. Transfer Characteristics

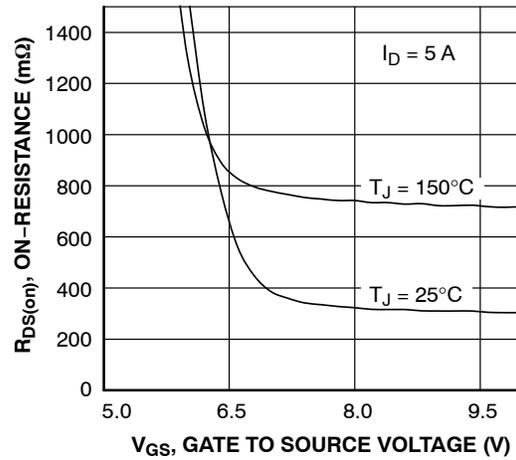


Figure 4. $R_{DS(on)}$ vs. Gate Voltage

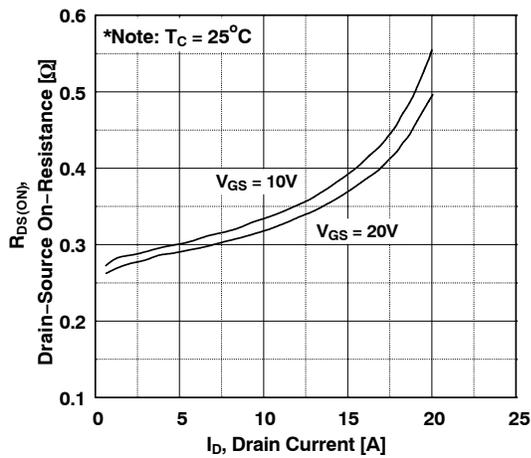


Figure 5. On-Resistance Variation vs. Drain Current and Gate Voltage

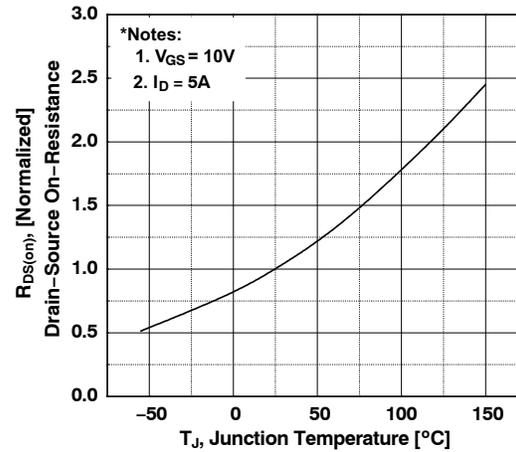


Figure 6. On-Resistance Variation vs. Temperature

TYPICAL CHARACTERISTICS

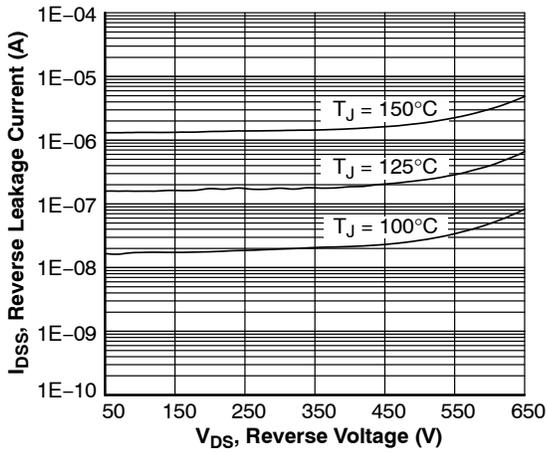


Figure 7. Drain-to-Source Leakage Current vs. Voltage

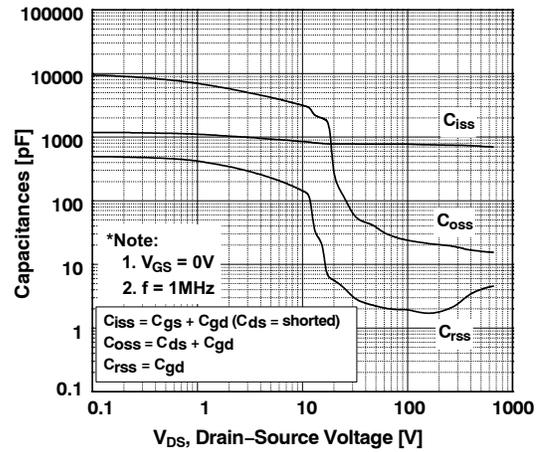


Figure 8. Capacitance Characteristics

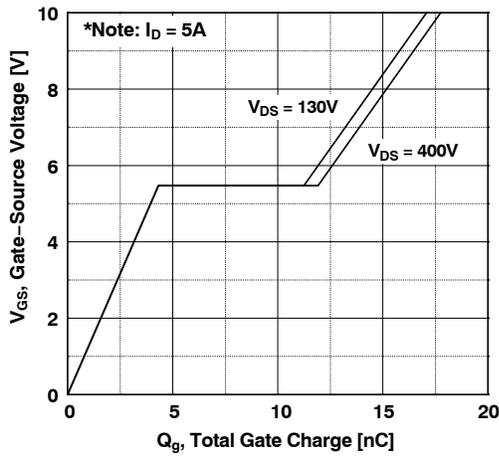


Figure 9. Gate Charge Characteristics

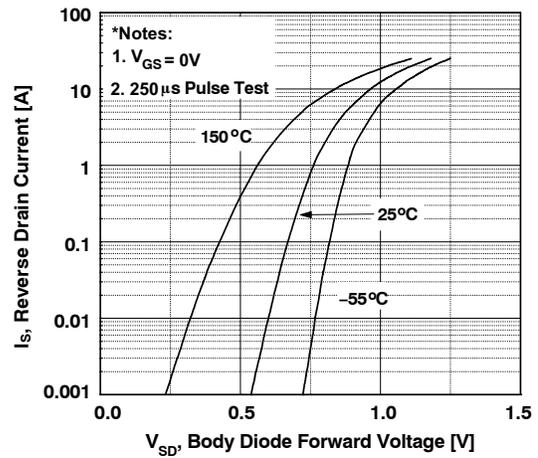


Figure 10. Body Diode Forward Voltage Variation vs. Source Current and Temperature

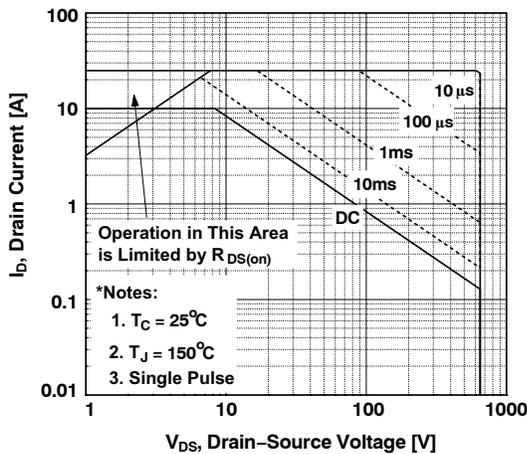


Figure 11. Maximum Safe Operating Area

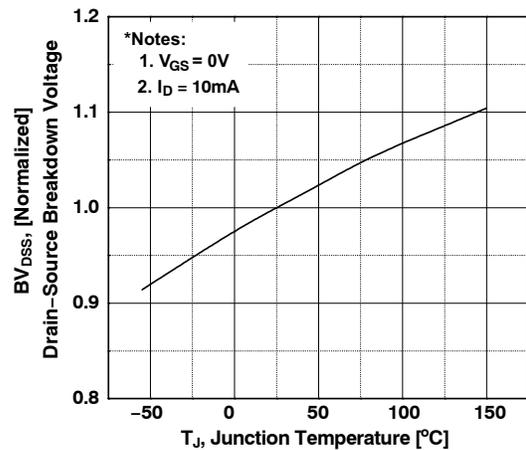


Figure 12. Breakdown Voltage Variation vs. Temperature

NVD360N65S3

TYPICAL CHARACTERISTICS

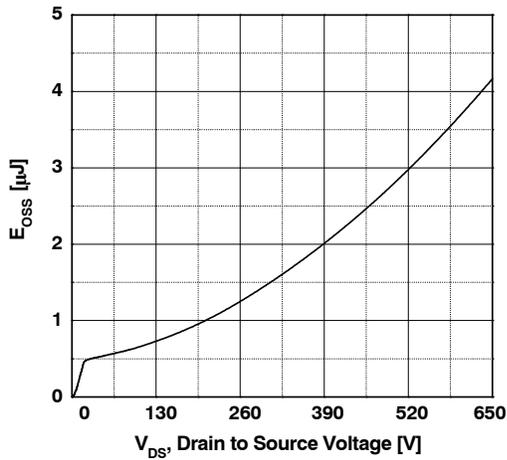


Figure 13. E_{OSS} vs. Drain to Source Voltage

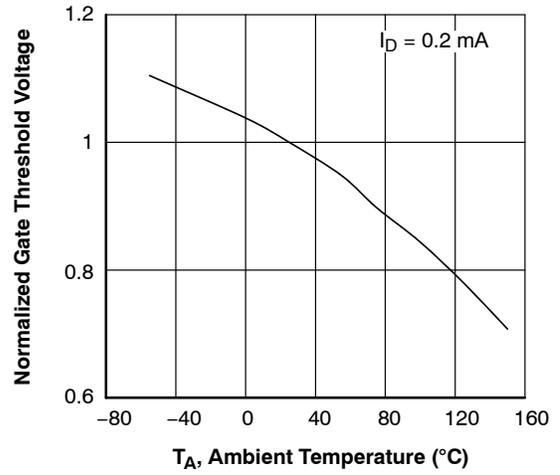


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

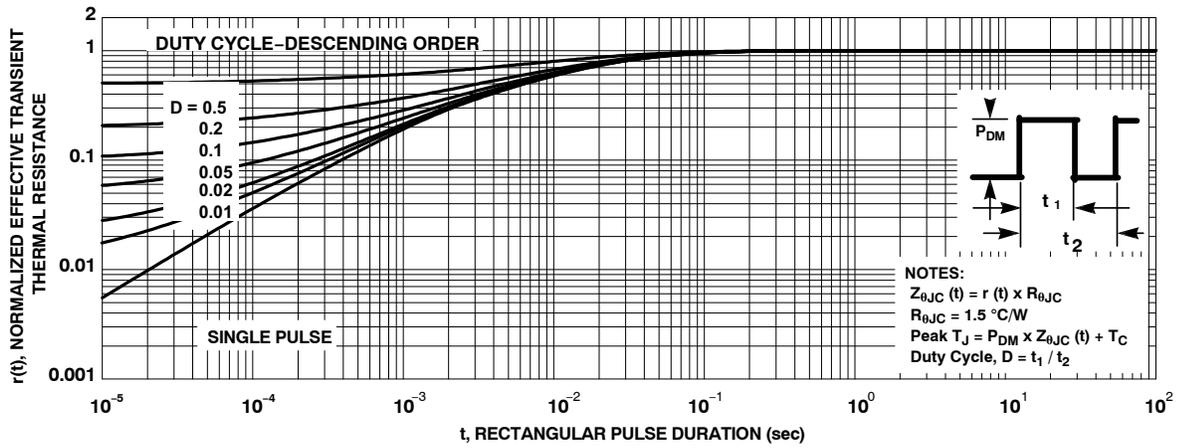


Figure 15. Transient Thermal Response Curve

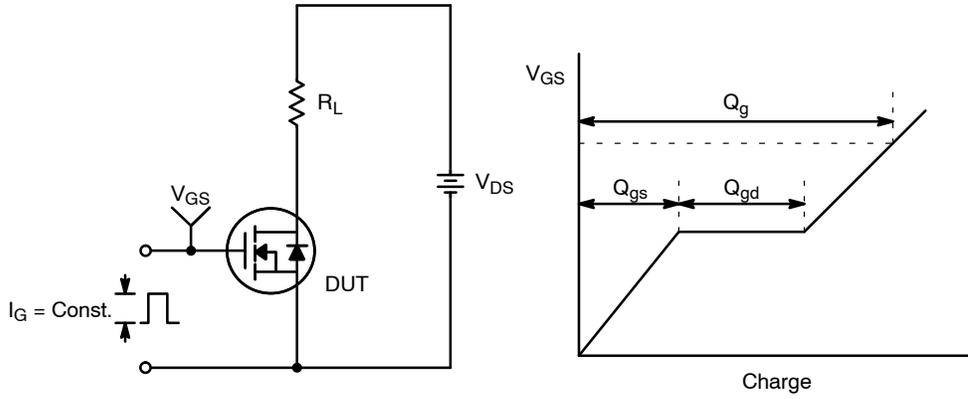


Figure 16. Gate Charge Test Circuit & Waveform

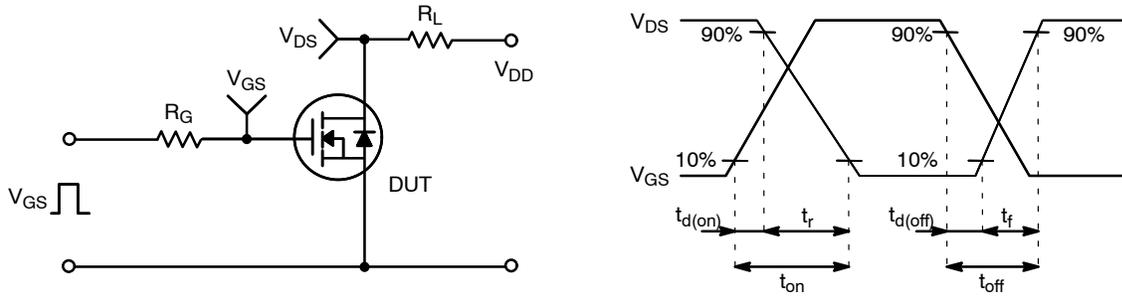


Figure 17. Resistive Switching Test Circuit & Waveforms

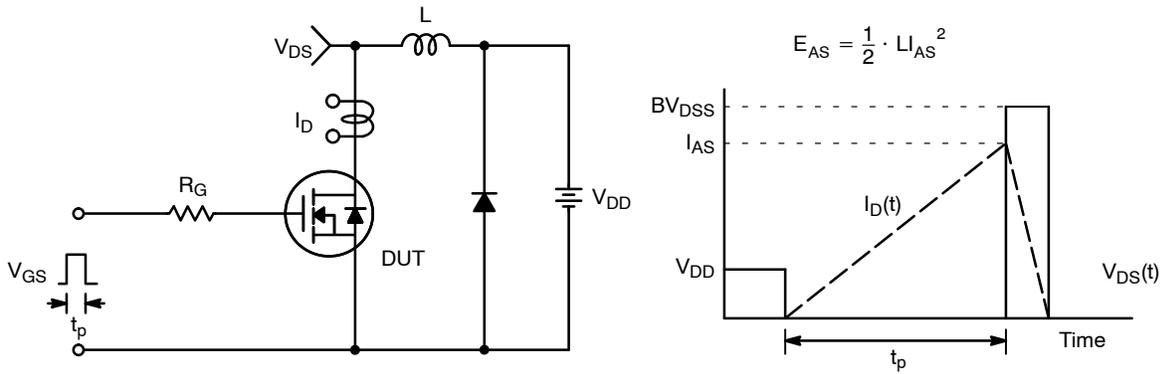


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

NVD360N65S3

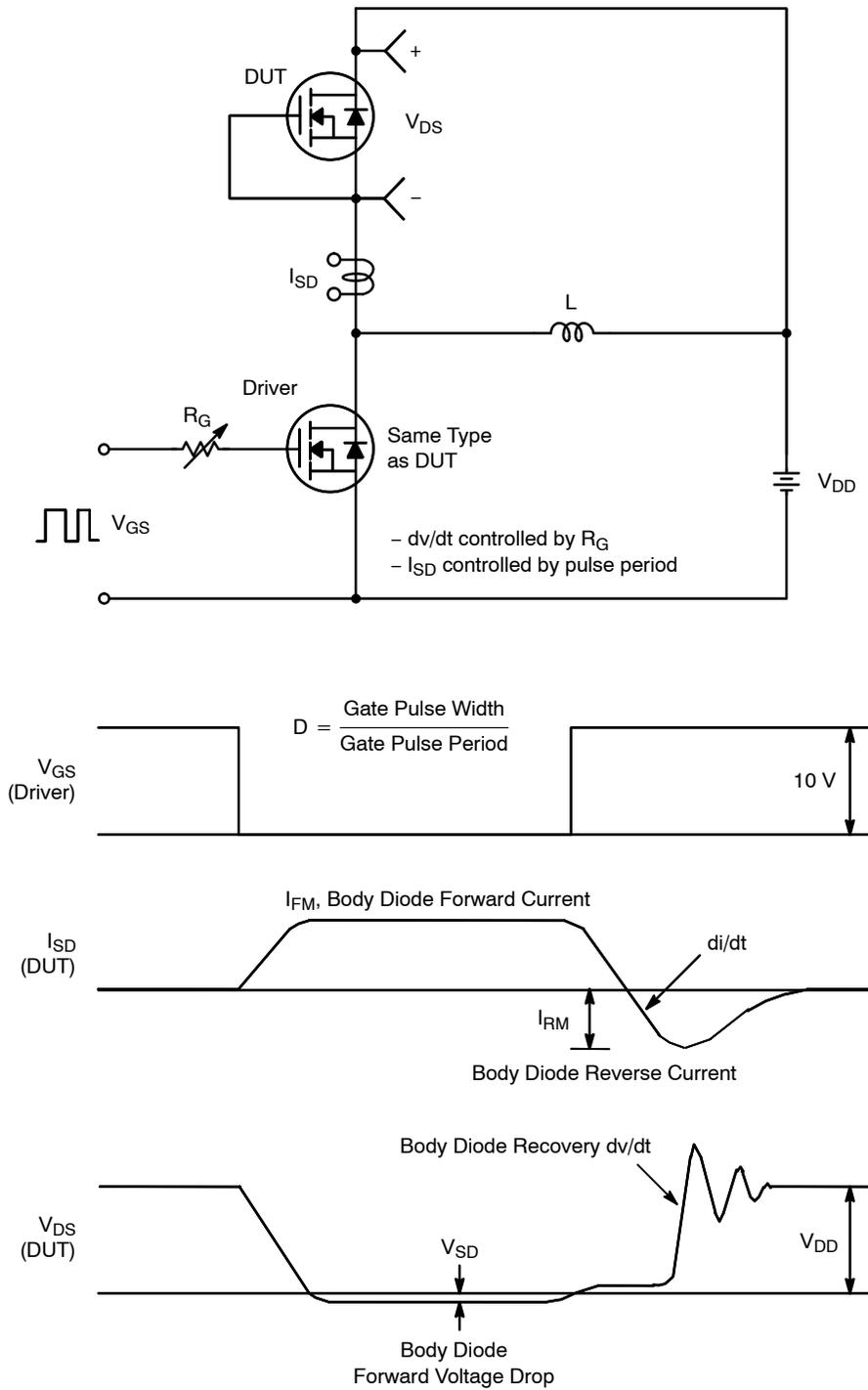
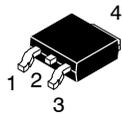


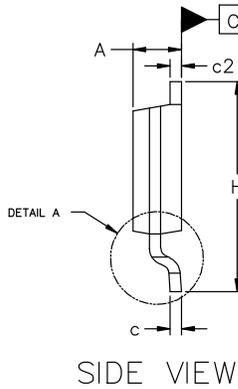
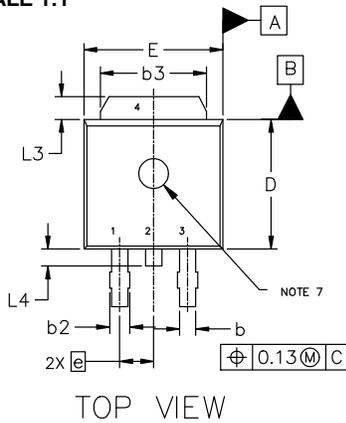
Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms



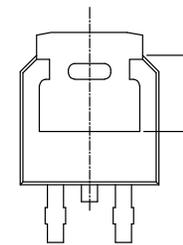
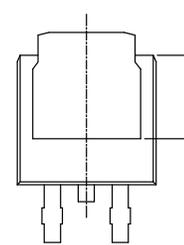
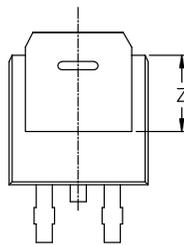
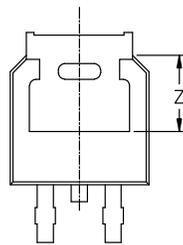
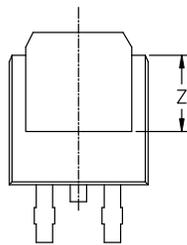
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



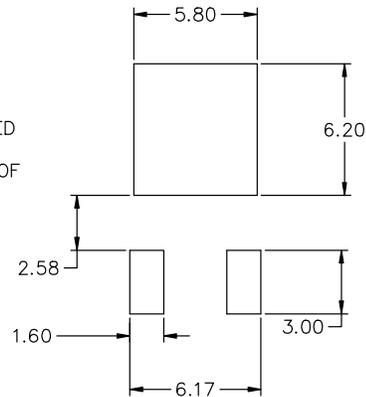
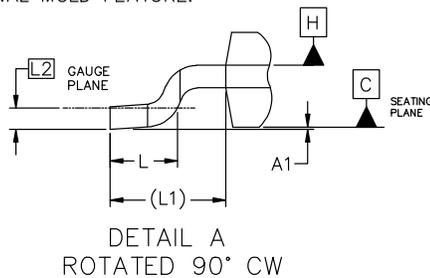
MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

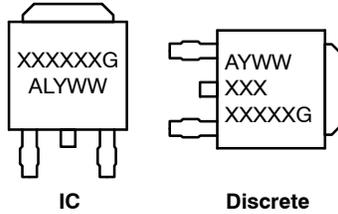
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DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN</p> | <p>STYLE 3:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 4:
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE</p> | <p>STYLE 5:
 PIN 1. GATE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |
| <p>STYLE 6:
 PIN 1. MT1
 2. MT2
 3. GATE
 4. MT2</p> | <p>STYLE 7:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 8:
 PIN 1. N/C
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. RESISTOR ADJUST
 4. CATHODE</p> | <p>STYLE 10:
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |

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