

MOSFET - Power, Single N-Channel, DFN5/DFNW5 30 V, 127 A NVMFS4C05N, **NVMFS4C305N**

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVMFS4C05NWF Wettable Flanks Option for Enhanced Optical
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS

MAXIMUM RATINGS (T_{.1} = 25 °C unless otherwise stated)

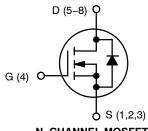
| Parameter | | | Symbol | Value | Unit |
|---|------------------------|---|--------------------------------------|----------------|------|
| Drain-to-Source Volta | .ge | | V_{DSS} | 30 | V |
| Gate-to-Source Voltage | je | | V_{GS} | ±20 | V |
| Continuous Drain Current R _{θJA} | T _A = 25 °C | | l _D | 27.2 | Α |
| (Notes 1, 2 and 4) | | T _A = 80 °C | טי | 21.6 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2 and 4) | Steady State | T _A = 25 °C | P _D | 3.61 | W |
| Continuous Drain Current R ₀ JC (Notes 1, 2, 3 and 4) | | T _C = 25 °C | | 127 | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3 and 4) | | T _C = 80 °C | l _D | 101 | А |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3 and 4) | | T _C = 25 °C | P _D | 79 | W |
| Pulsed Drain Current | $T_A = 25$ | $T_A = 25 {}^{\circ}C, t_p = 10 \mu s$ | | 174 | Α |
| Operating Junction and Storage Temperature | | | T _J , T _{STG} | -55 to +175 | °C |
| Source Current (Body | / Diode) | | I _S | 72 | Α |
| Single Pulse Drain-to- Energy (T _J = 25 °C, I _I | | | E _{AS} | 42 | mJ |
| Lead Temperature for (1/8" from case for 10 | | Purposes | TL | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

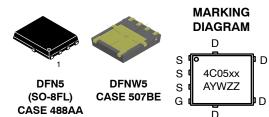
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.
- 3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
- 4. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.

1

| V _{(BR)DSS} | V _{(BR)DSS} R _{DS(ON)} MAX | |
|----------------------|--|-------|
| 30 V | 2.8 m Ω @ 10 V | 127 A |
| | 4.0 mΩ @ 4.5 V | 121 A |



N-CHANNEL MOSFET



= Specific Device Code for NVMFS4C05N

4C05WF= Specific Device Code of NVMFS4C05NWF

= Assembly Location = Year

W = Work Week 77 = Lot Traceabililty

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--|--------------------|-----------------------|
| NVMFS4C05NT1G, NVMFS4C305NT1G-YE, NVMFS4C305NET1G-YE, NVMFS4C305NET1G | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS4C05NT3G | DFN5 (Pb-Free) | 5000 / Tape & Reel |
| NVMFS4C05NWFT1G, NVMFS4C05NWFET1G | DFNW5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS4C05NWFT3G | DFNW5 (Pb-Free) | 5000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case (Drain) | $R_{	heta JC}$ | 1.9 | °C/W |
| Junction-to-Ambient – Steady State (Note 5) | $R_{\theta JA}$ | 41.6 | C/VV |

^{5.} Surface-mounted on FR4 board using 650 mm², 2 oz Cu pad.

ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Тур | Max | Unit |
|--|--|--|---|------|-------|-----------|----------|
| OFF CHARACTERISTICS | | | | | | | • |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | $V_{GS} = 0 \text{ V}, I_D = 0 \text{ V}$ | = 250 μΑ | 30 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} / T _J | | | | 12 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 24 V | $T_J = 25 ^{\circ}\text{C}$ $T_J = 125 ^{\circ}\text{C}$ | | | 1.0 10 | μΑ |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} | _S = ±20 V | | | ±100 | nA |
| ON CHARACTERISTICS (Note 6) | • | | | | • | • | • |
| Gate Threshold Voltage | V _{GS(TH)} | $V_{GS} = V_{DS}, I_{D}$ | = 250 μΑ | 1.3 | | 2.2 | V |
| Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | | -5.1 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 30 A | | 2.3 | 2.8 | mΩ |
| | | V _{GS} = 4.5 V | I _D = 30 A | | 3.3 | 4.0 | |
| Forward Transconductance | 9FS | V _{DS} = 1.5 V, I | _ | | 68 | | S |
| Gate Resistance | R_{G} | T _A = 25 | °C | 0.3 | 1.0 | 2.0 | Ω |
| CHARGES AND CAPACITANCES | | | | | | | |
| Input Capacitance | C _{ISS} | | | | 1972 | | |
| Output Capacitance | C _{OSS} | $V_{GS} = 0 \text{ V, f} = 1 \text{ MH}$ | łz, V _{DS} = 15 V | | 1215 | | pF |
| Reverse Transfer Capacitance | C _{RSS} | | | | 59 | | |
| Capacitance Ratio | C _{RSS} /C _{ISS} | $V_{GS} = 0 \text{ V}, V_{DS} = 1$ | 5 V, f = 1 MHz | | 0.030 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | | | | 14 | | |
| Threshold Gate Charge | Q _{G(TH)} | | | | 3.3 | | nC |
| Gate-to-Source Charge | Q_{GS} | V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A | | | 6.0 | | |
| Gate-to-Drain Charge | Q_{GD} | | | | 5.0 | | |
| Gate Plateau Voltage | V _{GP} | | | | 3.1 | | V |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 15 V; I _D = 30 A | | | 30 | | nC |
| SWITCHING CHARACTERISTICS (Note | 7) | | | | | | |
| Turn-On Delay Time | t _{d(ON)} | | | | 11 | | |
| Rise Time | t _r | $V_{GS} = 4.5 \text{ V}, V_{E}$ | os = 15 V, | | 32 | | ns |
| Turn-Off Delay Time | t _{d(OFF)} | $I_D = 15 \text{ A}, R_G = 3.0 \Omega$ | | | 21 | | 113 |
| Fall Time | t _f | | | | 7.0 | | 1 |
| Turn-On Delay Time | t _{d(ON)} | | | | 8.0 | | |
| Rise Time | t _r | $V_{GS} = 10 \text{ V}, V_{E}$ | | | 26 | | ns |
| Turn-Off Delay Time | t _{d(OFF)} | $I_D = 15 \text{ A}, R_G = 3.0 \Omega$ | | | 26 | | 113 |
| Fall Time | t _f | | | | 5.0 | | <u>l</u> |
| DRAIN-SOURCE DIODE CHARACTERIS | TICS | | | | - | - | |
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0 V$, | T _J = 25 °C | | 0.77 | 1.1 | V |
| | | $I_{S} = 10 \text{ A}$ | T _J = 125 °C | | 0.62 | | 1 ° |
| Reverse Recovery Time | t _{RR} | $V_{GS} = 0 \text{ V, } dl_{S}/dt = 100 \text{ A/}\mu\text{s,}$ | | 40.2 | | | |
| Charge Time | t _a | | | | 20.3 | | ns |
| Discharge Time | t _b | | | | 19.9 | | 1 |
| Reverse Recovery Charge | Q_{RR} | | | | 30.2 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

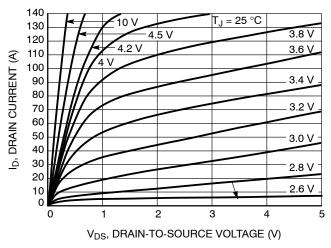


Figure 1. On-Region Characteristics

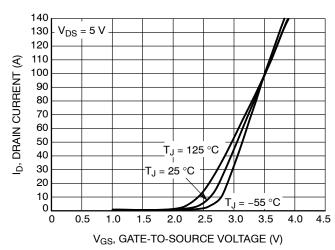


Figure 2. Transfer Characteristics

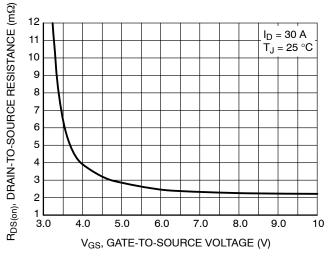


Figure 3. On-Resistance vs. V_{GS}

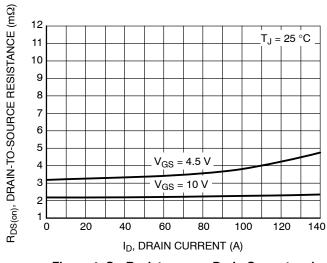


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

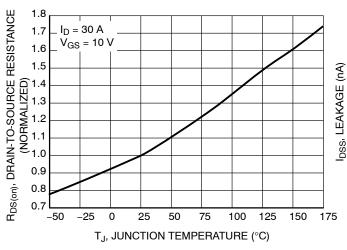


Figure 5. On-Resistance Variation with Temperature

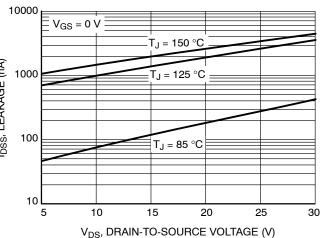


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

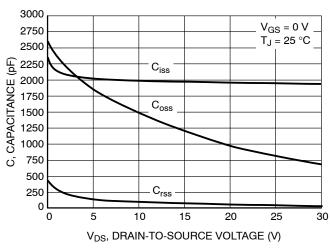


Figure 7. Capacitance Variation

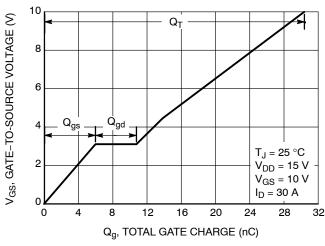


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

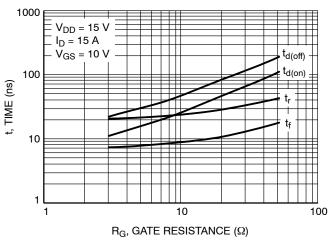


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

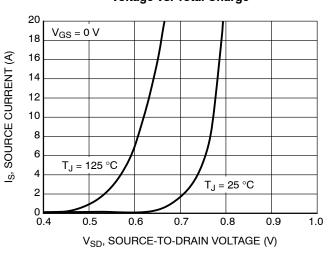


Figure 10. Diode Forward Voltage vs. Current

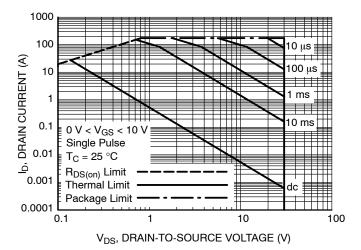


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

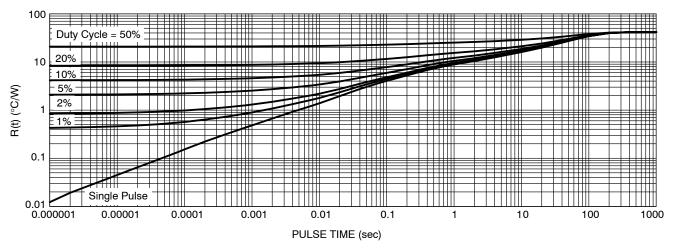


Figure 12. Thermal Response

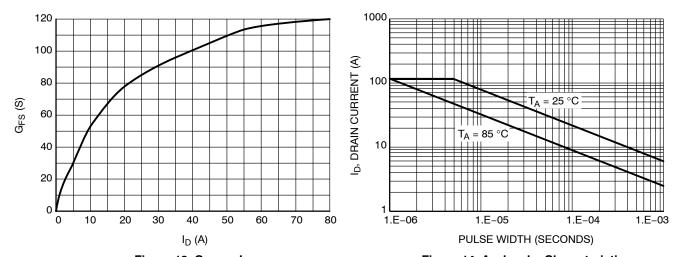


Figure 13. G_{FS} vs. I_D

Figure 14. Avalanche Characteristics

REVISION HISTORY

| Revision | Description of Changes | Date | |
|----------|--|-----------|--|
| 7 | Added a new OPN - NVMFS4C305NET1G. Updated the main title - added DFNW5. | 8/27/2025 | |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.





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SIDE VIEW

DFN5 5x6, 1.27P (SO-8FL) CASE 488AA **ISSUE N**

DATE 25 JUN 2018

NOTES:

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE
- MOLD FLASH PROTRUSIONS OR GATE BURRS

| | MILLIMETERS | | | |
|-----|----------------|----------|------|--|
| DIM | MIN | NOM | MAX | |
| Α | 0.90 | 1.00 | 1.10 | |
| A1 | 0.00 | | 0.05 | |
| b | 0.33 | 0.41 | 0.51 | |
| С | 0.23 | 0.28 | 0.33 | |
| D | 5.00 | 5.15 | 5.30 | |
| D1 | 4.70 | 4.90 | 5.10 | |
| D2 | 3.80 | 4.00 | 4.20 | |
| E | 6.00 | 6.15 | 6.30 | |
| E1 | 5.70 | 5.90 | 6.10 | |
| E2 | 3.45 | 3.65 | 3.85 | |
| е | | 1.27 BSC | ; | |
| G | 0.51 | 0.575 | 0.71 | |
| K | 1.20 | 1.35 | 1.50 | |
| L | 0.51 | 0.575 | 0.71 | |
| L1 | 0.125 REF | | | |
| М | 3.00 3.40 3.80 | | 3.80 | |
| θ | 0 ° | | 12 ° | |

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

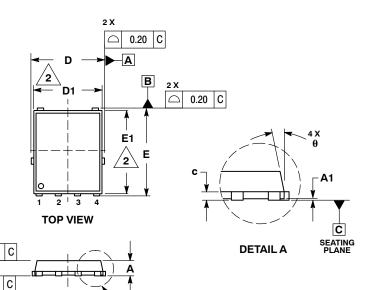
= Assembly Location Α

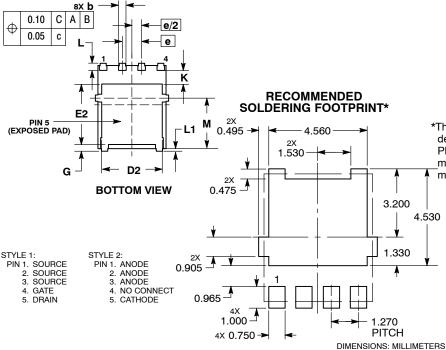
= Lot Traceability

Υ = Year W = Work Week

ZZ

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.





DETAIL A

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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|------------------|--------------------------|--|-------------|--|
| DESCRIPTION: | DFN5 5x6, 1.27P (SO-8FL) | | PAGE 1 OF 1 | |

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PIN 1

IDENTIFIER

DFNW5 4.90x5.90x1.00, 1.27P

CASE 507BE **ISSUE B**

A

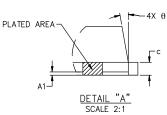
DATE 19 SEP 2024

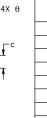
12°

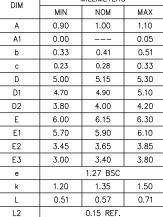
6

NOTES:

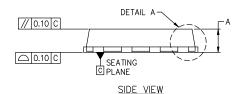
- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018. 1.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.







MILLIMETERS



TOP VIEW



CONSTRUCTION



THE BOTTOM OF TIE BAR.

0.10 C A B DETAIL B ф 0.05 C e/2 8X L E2 PIN 5

-D2

BOTTOM VIEW

DETAIL "B" SCALE 2:1

2X 0.50-4.56 -1.53-2X 0.48 PACKAGE 3.20 OUTLINE 1.33 2X 0.91-4X 1.00 0.97 1.27 PIN 1 ID PITCH 4X 0.75

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RECOMMENDED MOUNTING FOOTPRINT* *FOR ADDITIONAL INFORMATION ON OUR Pb—FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

(EXPOSED PAD)



= Assembly Location Α Υ = Year

W = Work Week 77 = Lot Traceability

XXXXXX = Specific Device Code *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION: DFNW5 4.90x5.90x1.00, 1.27P

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PAGE 1 OF 1

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