

# MOSFET - Power, Single N-Channel, STD Gate, SO8FL

80 V, 1.43 mΩ, 253 A

## NVMFWS1D5N08X

### Features

- Low  $Q_{RR}$ , Soft Recovery Body Diode
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

### Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

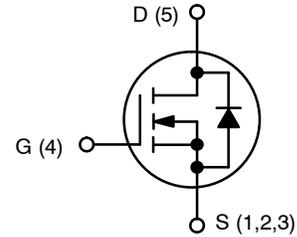
### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	80	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current (Note 1)	I <sub>D</sub>	T <sub>C</sub> = 25°C	253 A
		T <sub>C</sub> = 100°C	179
Power Dissipation (Note 1)	P <sub>D</sub>	194	W
Pulsed Drain Current	I <sub>DM</sub>	T <sub>C</sub> = 25°C, t <sub>p</sub> = 100 μs	1071
Pulsed Source Current (Body Diode)			I <sub>SM</sub>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)	I <sub>S</sub>	303	A
Single Pulse Avalanche Energy (I <sub>PK</sub> = 67 A) (Note 3)	E <sub>AS</sub>	225	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

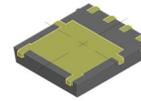
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. E<sub>AS</sub> of 225 mJ is based on started T<sub>J</sub> = 25°C, I<sub>AS</sub> = 67 A, V<sub>DD</sub> = 64 V, V<sub>GS</sub> = 10 V, 100% avalanche tested

V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
80 V	1.43 mΩ @ 10 V	253 A

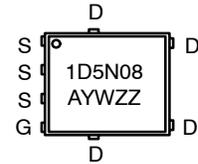


N-CHANNEL MOSFET



DFNW5  
(SO8FL WF)  
CASE 507BA

### MARKING DIAGRAM



1D5N08 = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMFWS1D5N08X

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.77	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Notes 4, 5)	$R_{\theta JA}$	39	

- Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 1 oz. Cu pad.
- $R_{\theta JA}$  is determined by the user's board design.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = 1 mA$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1 mA$ , Referenced to $25^{\circ}C$		17.8		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80 V, T_J = 25^{\circ}C$			1	$\mu A$
		$V_{DS} = 80 V, T_J = 125^{\circ}C$			250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = 20 V$			100	nA

## ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 50 A$		1.24	1.43	$m\Omega$
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 330 \mu A$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 330 \mu A$		-7.32		$mV/^{\circ}C$
Forward Transconductance	$g_{FS}$	$V_{DS} = 5 V, I_D = 50 A$		176		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz$		5880		$pF$	
Output Capacitance	$C_{OSS}$			1690			
Reverse Transfer Capacitance	$C_{RSS}$			25			
Output Charge	$Q_{OSS}$	$V_{GS} = 10 V, V_{DD} = 40 V; I_D = 50 A$		121		nC	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 6 V, V_{DD} = 40 V; I_D = 50 A$		51		
Total Gate Charge	$Q_{G(TOT)}$				83		
Threshold Gate Charge	$Q_{G(TH)}$				18		
Gate-to-Source Charge	$Q_{GS}$				27		
Gate-to-Drain Charge	$Q_{GD}$				13		
Gate Plateau Voltage	$V_{GP}$				4.6		V
Gate Resistance	$R_G$	$f = 1 MHz$		0.6		$\Omega$	

## SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10 V, V_{DD} = 64 V,$ $I_D = 50 A, R_G = 2.5 \Omega$		24		ns
Rise Time	$t_r$			10		
Turn-Off Delay Time	$t_{d(OFF)}$			45		
Fall Time	$t_f$			9		

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 V, I_S = 50 A, T_J = 25^{\circ}C$		0.81	1.2	V
		$V_{GS} = 0 V, I_S = 50 A, T_J = 125^{\circ}C$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0 V, I_S = 50 A,$ $di/dt = 1000 A/\mu s, V_{DD} = 64 V$		36		ns
Charge Time	$t_a$			19		
Discharge Time	$t_b$			18		
Reverse Recovery Charge	$Q_{RR}$			290		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

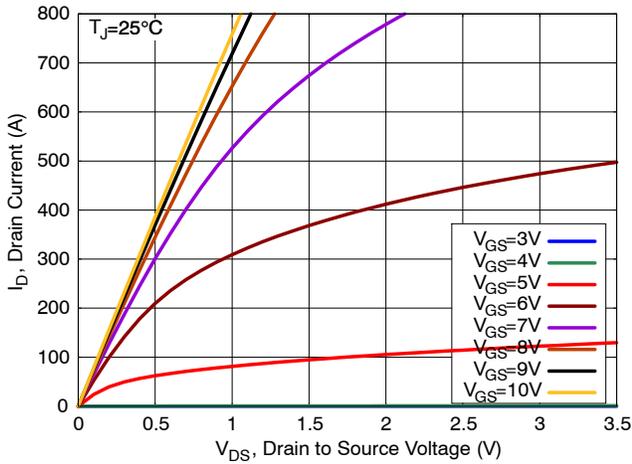


Figure 1. On-Region Characteristics

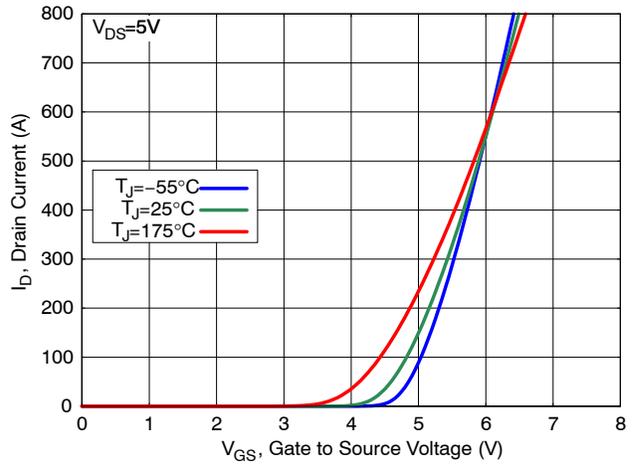


Figure 2. Transfer Characteristics

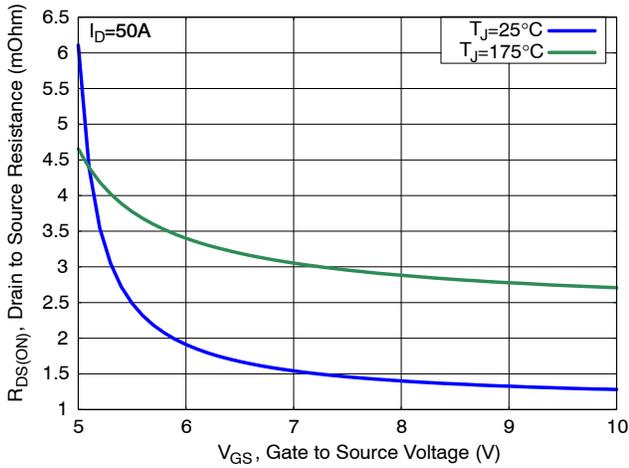


Figure 3. On-Resistance vs. Gate Voltage

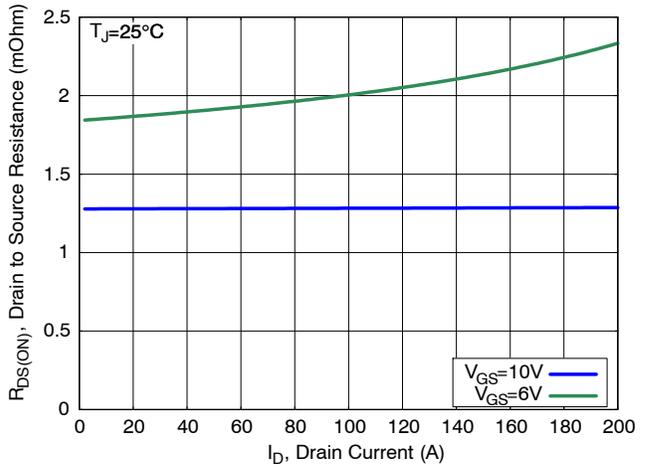


Figure 4. On-Resistance vs. Drain Current

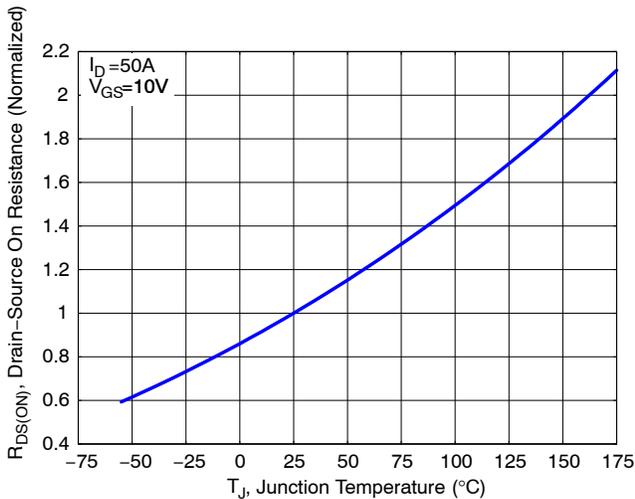


Figure 5. Normalized On-Resistance vs. Junction Temperature

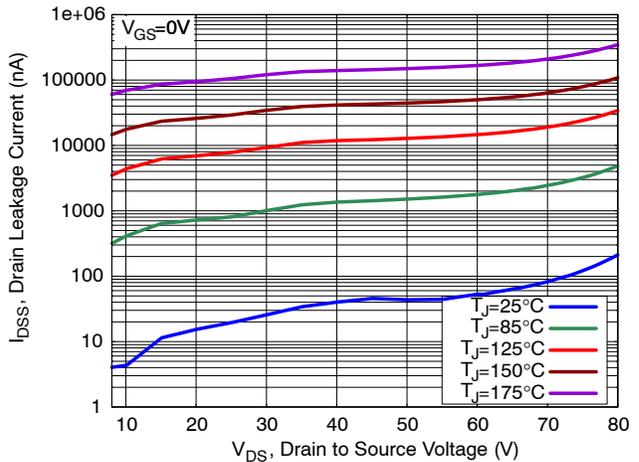


Figure 6. Drain Leakage Current vs. Drain Voltage

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## TYPICAL CHARACTERISTICS

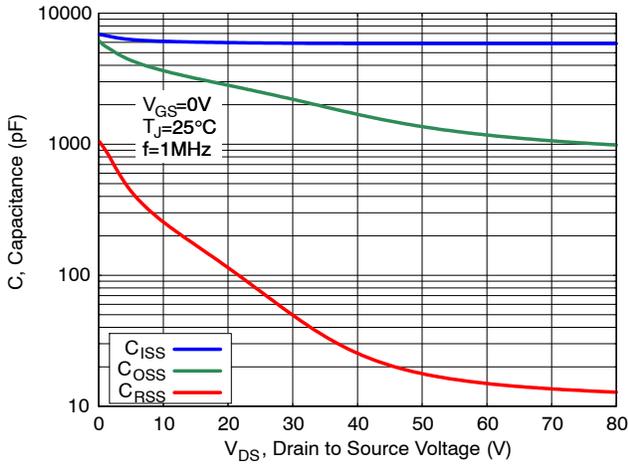


Figure 7. Capacitance Characteristics

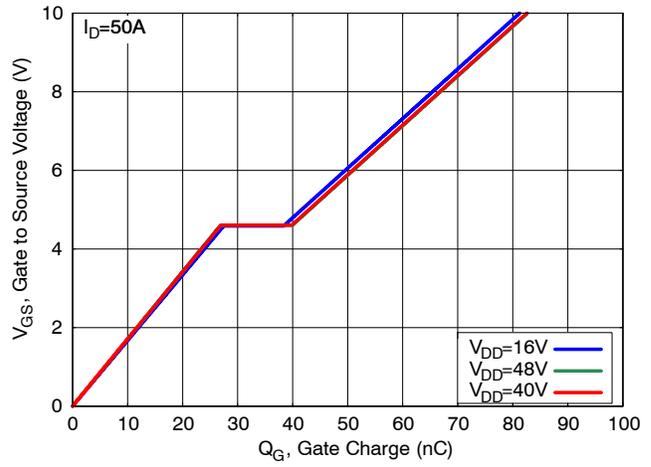


Figure 8. Gate Charge Characteristics

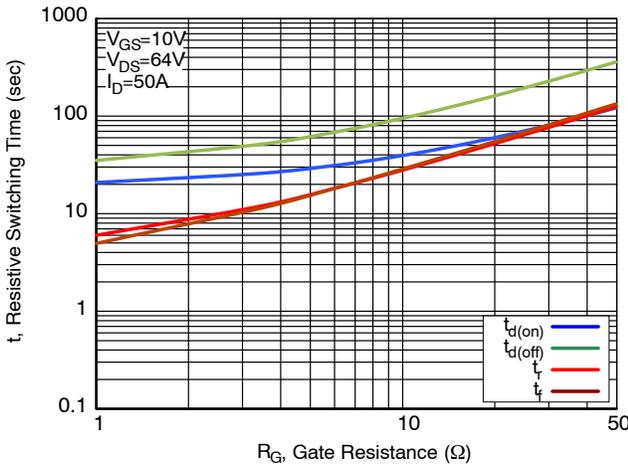


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

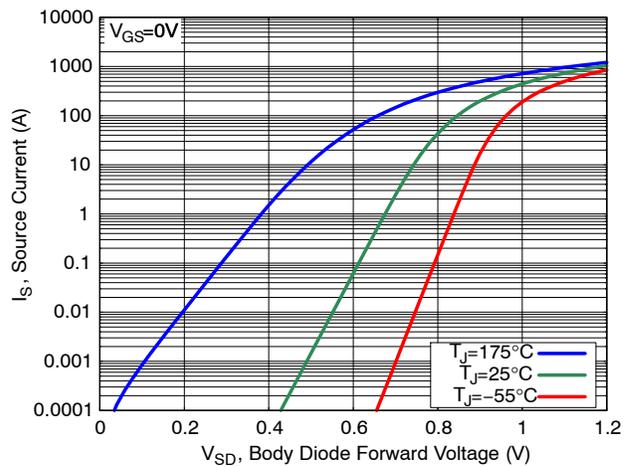


Figure 10. Diode Forward Characteristics

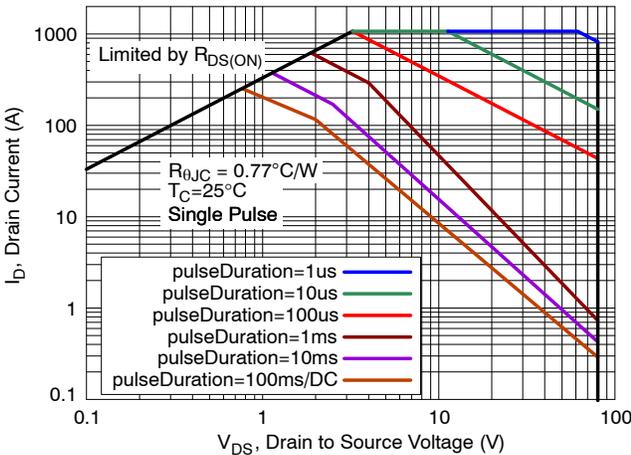


Figure 11. Safe Operating Area (SOA)

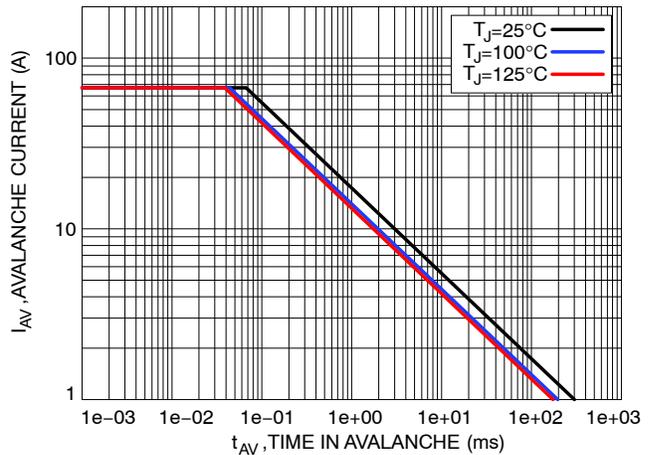
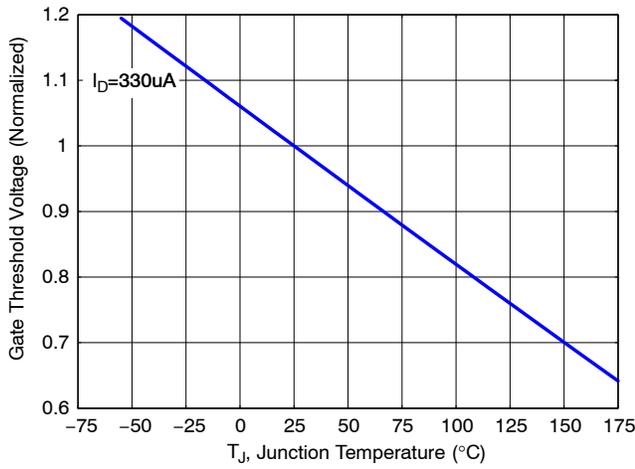


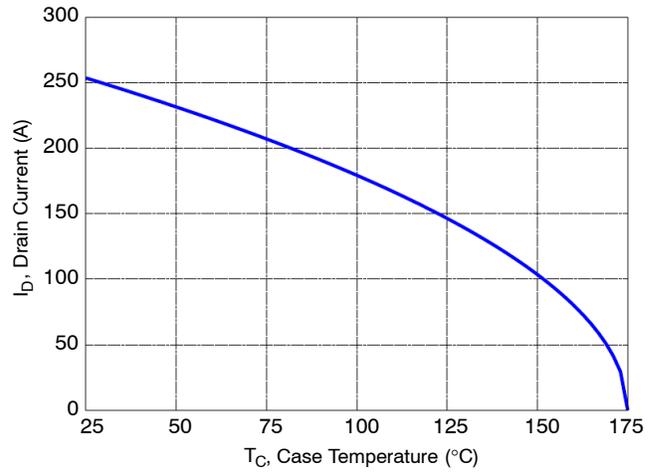
Figure 12. Avalanche Current vs. Pulse Time (UIS)

# NVMFWS1D5N08X

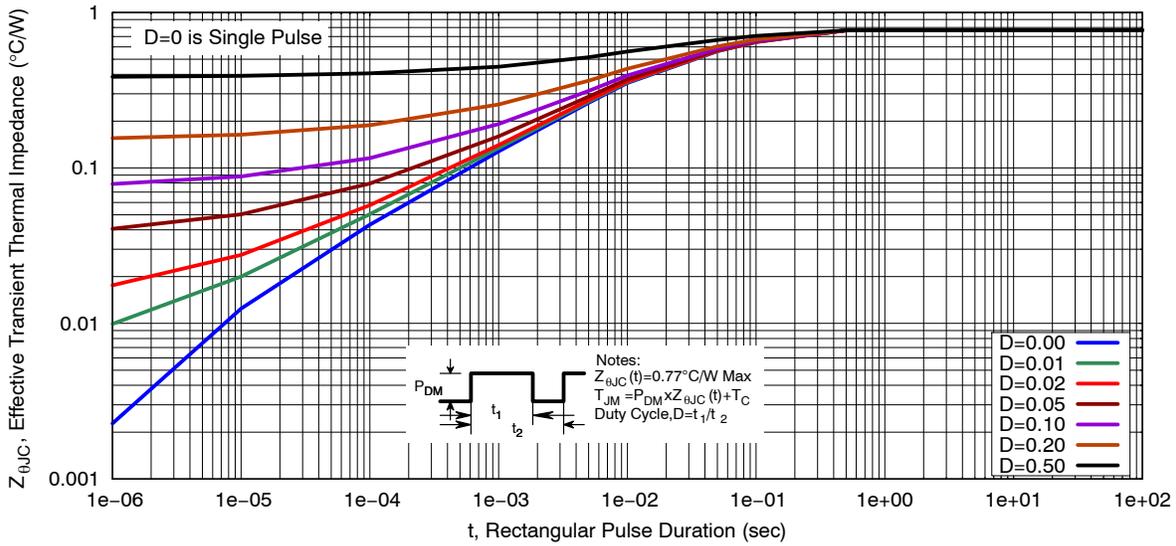
## TYPICAL CHARACTERISTICS



**Figure 13. Gate Threshold Voltage vs. Junction Temperature**



**Figure 14. Maximum Current vs. Case Temperature**



**Figure 15. Transient Thermal Response**

### DEVICE ORDERING INFORMATION

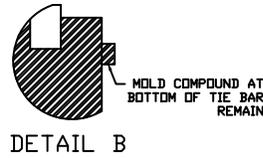
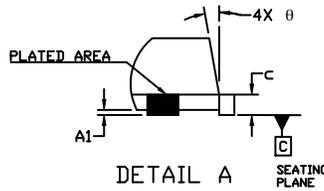
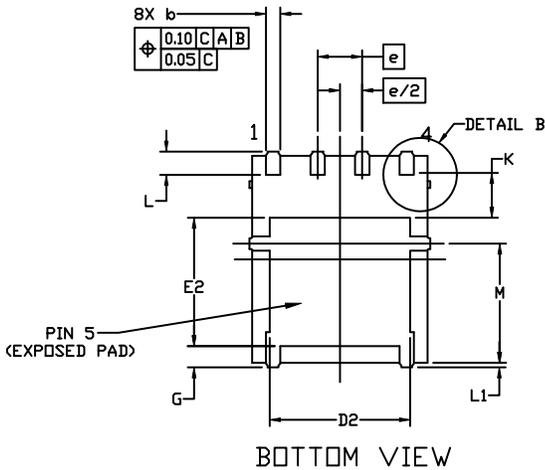
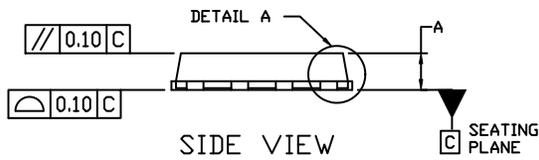
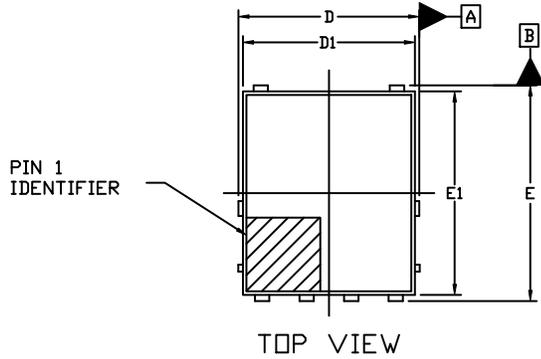
Device	Marking	Package	Shipping†
NVMFWS1D5N08XT1G	1D5N08	DFNW5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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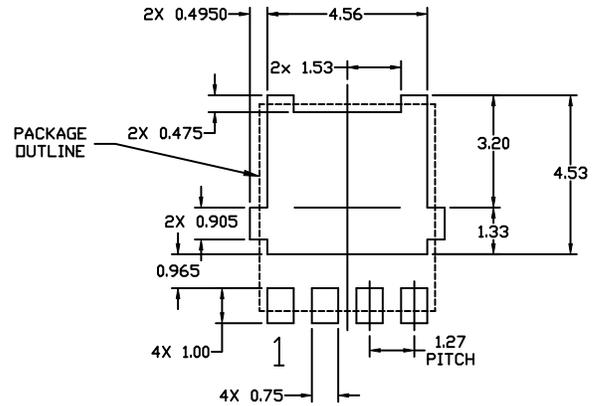
## PACKAGE DIMENSIONS

### DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
$\theta$	0°	---	12°



### RECOMMENDED MOUNTING FOOTPRINT

- \* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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