

# MOSFET – Power, Single N-Channel, STD Gate, SO8FL

80 V, 1.9 mΩ, 201 A

NVMFWS1D9N08X

## Features

- Low QRR, Soft Recovery Body Diode
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- AEC Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## Applications

- Synchronous Rectification (SR) in DC–DC and AC–DC
- Primary Switch in Isolated DC–DC Converter
- Motor Drives
- Automotive 48 V System

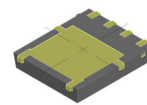
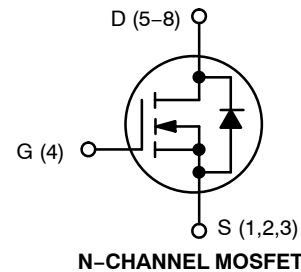
## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	80	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	201 A
		$T_C = 100^\circ\text{C}$	142
Power Dissipation (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	164 W
Pulsed Drain Current	$I_{DM}$	$T_C = 25^\circ\text{C}$ , $t_p = 100 \mu\text{s}$	866
Pulsed Source Current (Body Diode)			866
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	$-55$ to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	248	A
Single Pulse Avalanche Energy	$E_{AS}$	$I_{PK} = 58 \text{ A}$ (Note 3)	168 mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

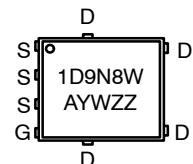
1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal and electromechanical application board design.
3. EAS of 168 mJ is based on started  $T_J = 25^\circ\text{C}$ ,  $I_{AS} = 58 \text{ A}$ ,  $V_{DD} = 64 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ , 100% avalanche tested.

$V_{(BR)DS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
80 V	1.9 mΩ @ 10 V	201 A



DFNW5 (SO-8FL)  
CASE 507BA

## MARKING DIAGRAM



1D9N8W = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NVMFWS1D9N08XT1G	DFNW5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVMFWS1D9N08X

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.91	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 4, 5)	$R_{\theta JA}$	39	

4. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

5.  $R_{\theta JA}$  is determined by the user's board design.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	80			V
Drain-to-Source Breakdown Voltage (transient)	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		31.6		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.7	1.9	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 252\text{ }\mu\text{A}$	2.4		3.6	V
Negative Threshold Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	$V_{GS} = V_{DS}, I_D = 252\text{ }\mu\text{A}$		-7.5		mV/°C
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		158		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4470		pF
Output Capacitance	$C_{OSS}$			1290		
Reverse Transfer Capacitance	$C_{RSS}$			20		
Output Charge	$Q_{OSS}$			93		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 40\text{ V}, I_D = 50\text{ A}, V_{GS} = 6\text{ V}$		39		nC
				63		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{DD} = 40\text{ V}, I_D = 50\text{ A}, V_{GS} = 10\text{ V}$		14		nC
Gate-to-Source Charge	$Q_{GS}$			21		
Gate-to-Drain Charge	$Q_{GD}$			10		
Gate Plateau Voltage	$V_{GP}$			4.7		
Gate Resistance	$R_G$	$f = 1\text{ MHz}$		0.8		Ω

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}$ , $V_{DD} = 64\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		28		ns
Rise Time	$t_r$			12		
Turn-Off Delay Time	$t_{d(OFF)}$			43		
Fall Time	$t_f$			7		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$I_S = 50\text{ A}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		0.82	1.2	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A},$ $dI_S/dt = 1000\text{ A}/\mu\text{s}, V_{DD} = 64\text{ V}$		26		ns	
Charge Time	$t_a$			15			
Discharge Time	$t_b$			12			
Reverse Recovery Charge	$Q_{RR}$			211			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NVMFWS1D9N08X

## TYPICAL CHARACTERISTICS

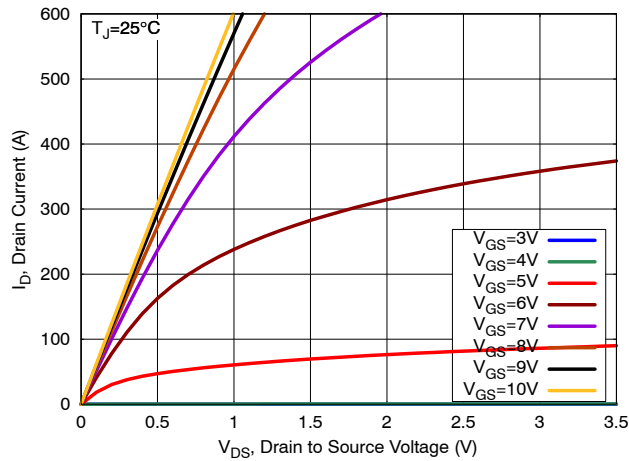


Figure 1. On-Region Characteristics

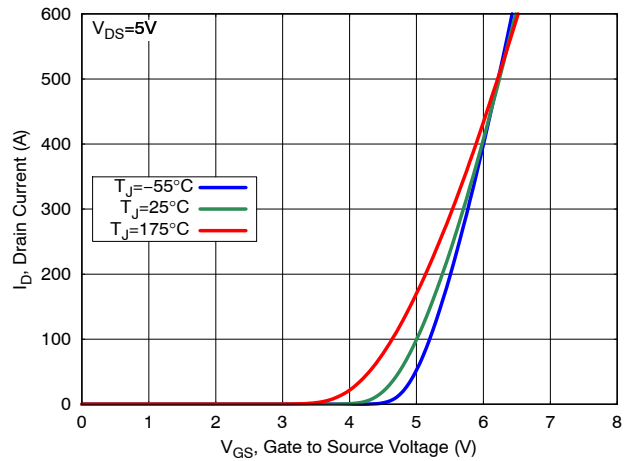


Figure 2. Transfer Characteristics

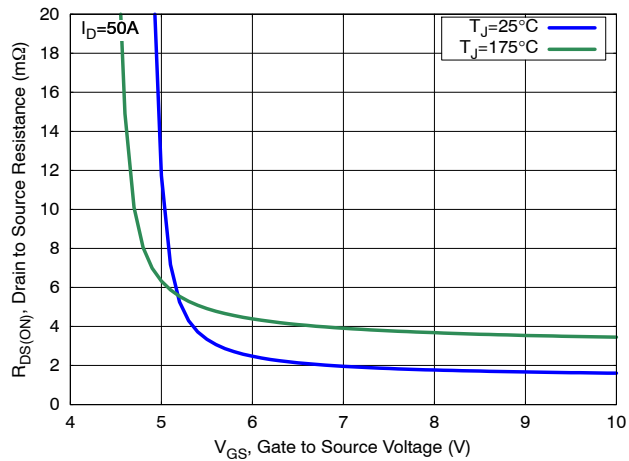


Figure 3. On-Resistance vs. Gate Voltage

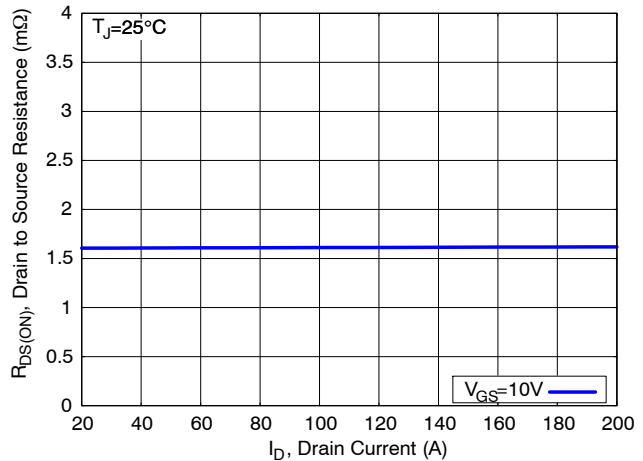


Figure 4. On-Resistance vs. Drain Current

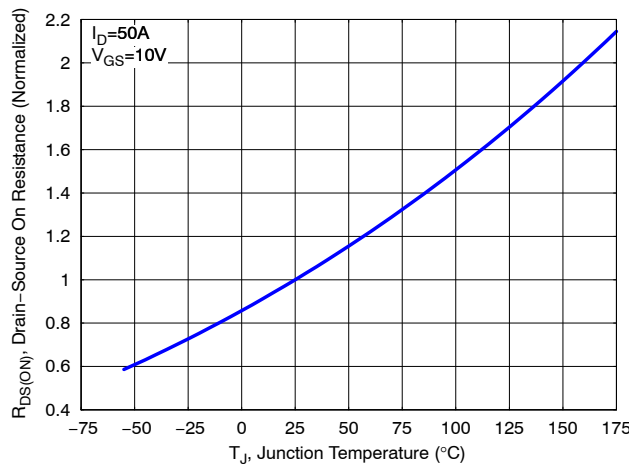


Figure 5. Normalized ON Resistance vs. Junction Temperature

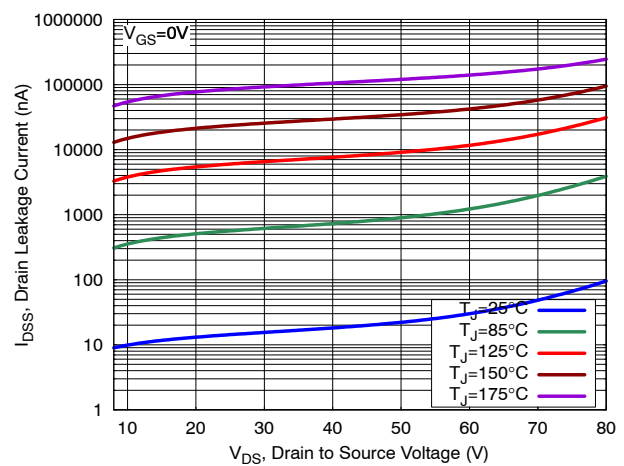


Figure 6. Drain Leakage Current vs. Drain Voltage

# NVMFWS1D9N08X

## TYPICAL CHARACTERISTICS

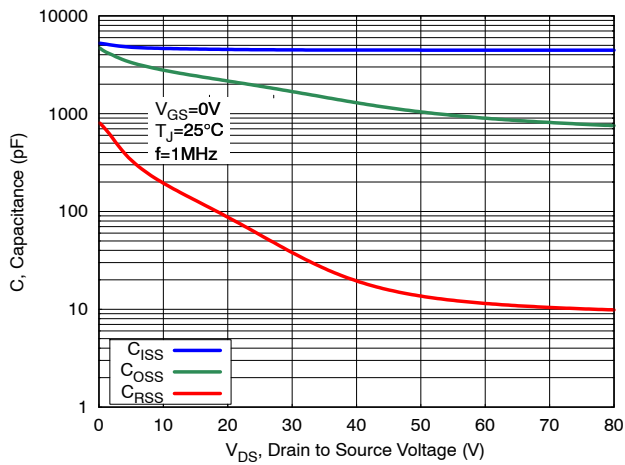


Figure 7. Capacitance Characteristics

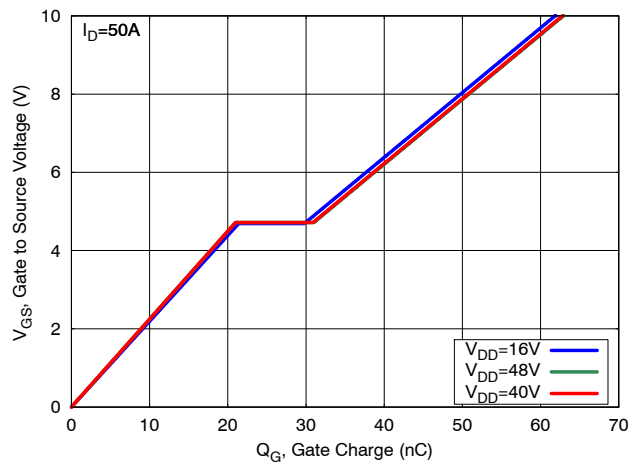


Figure 8. Gate Charge Characteristics

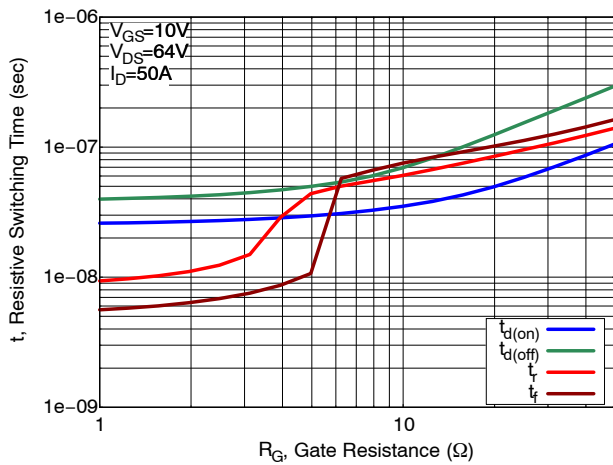


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

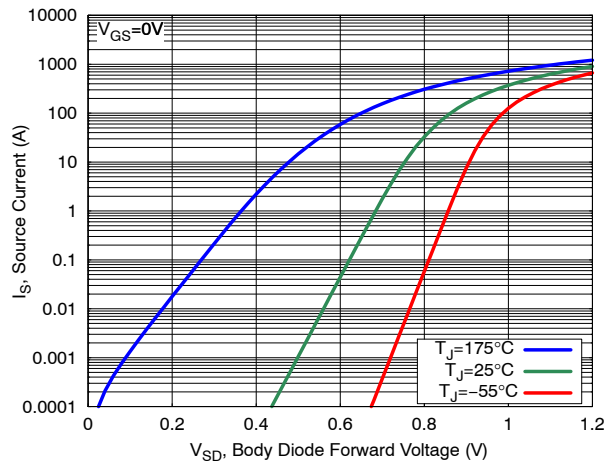


Figure 10. Diode Forward Characteristics

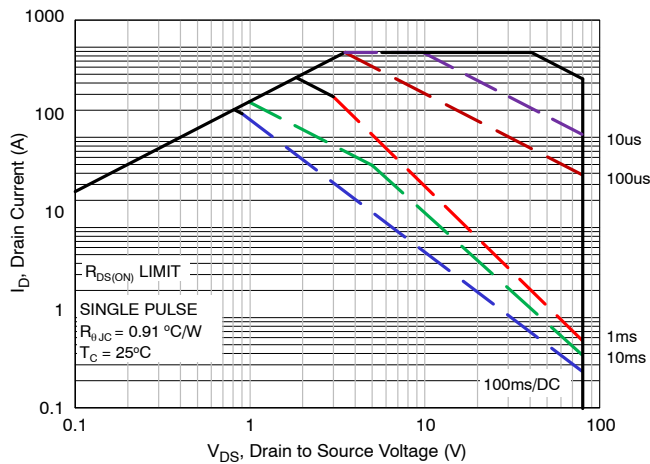


Figure 11. Safe Operating Area (SOA)

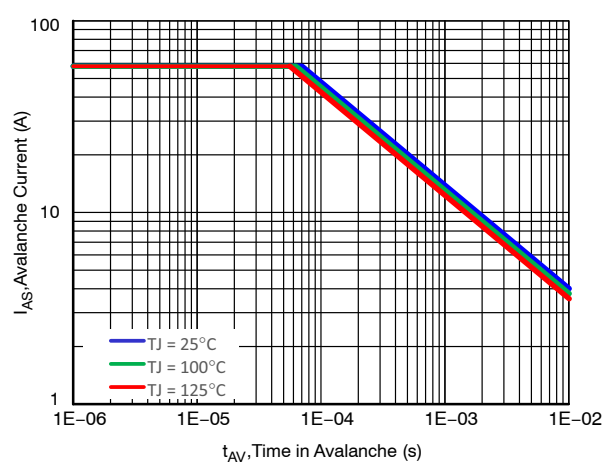
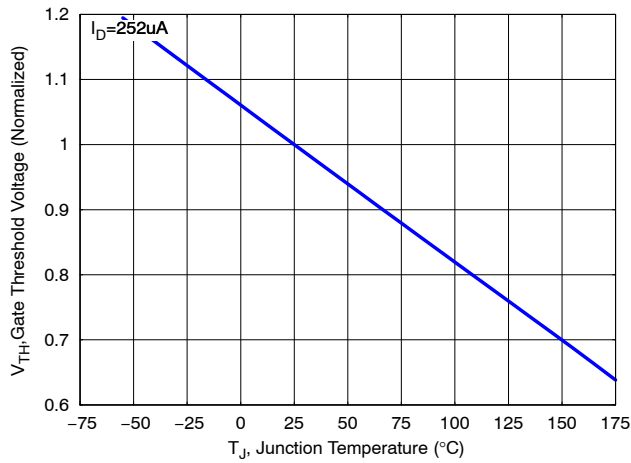


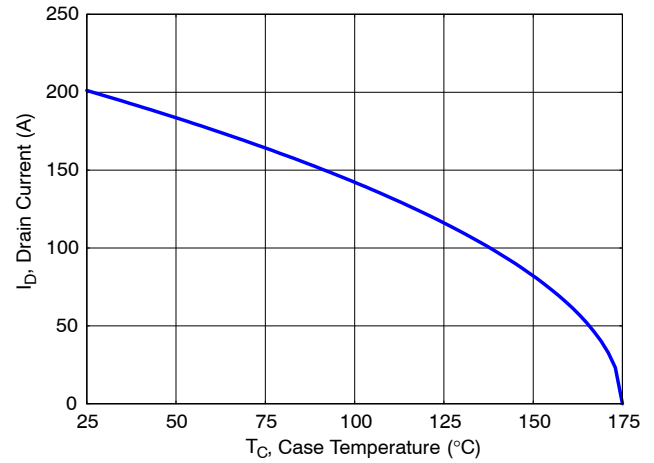
Figure 12. Avalanche Current vs Pulse Time (UIS)

# NVMFWS1D9N08X

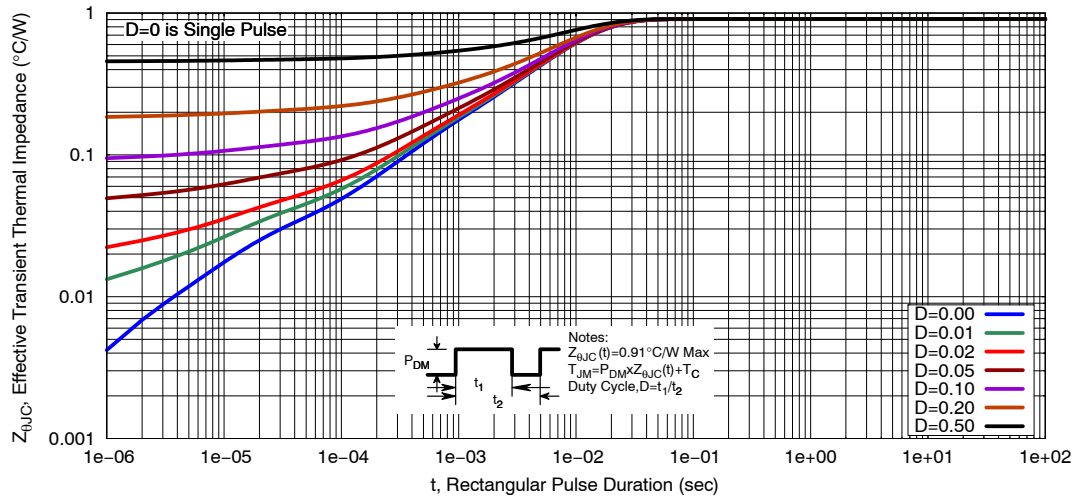
## TYPICAL CHARACTERISTICS



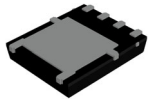
**Figure 13. Gate Threshold Voltage vs Junction Temperature**



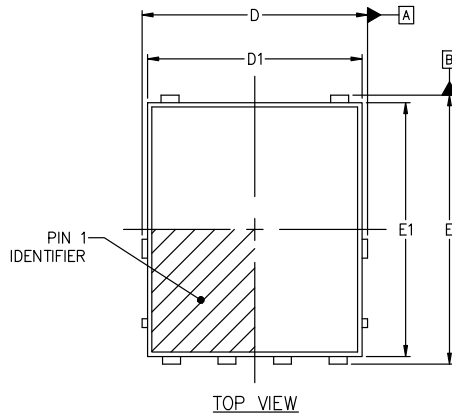
**Figure 14. Maximum Current vs. Case Temperature**



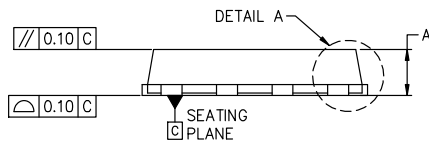
**Figure 15. Transient Thermal Response**


**DFNW5 4.90x5.90x1.00, 1.27P**  
**CASE 507BA**  
**ISSUE C**

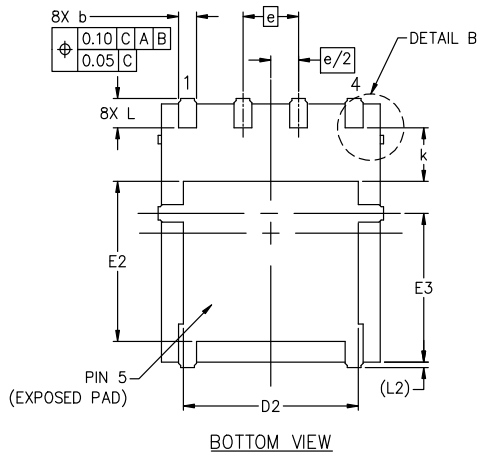
DATE 19 SEP 2024



TOP VIEW



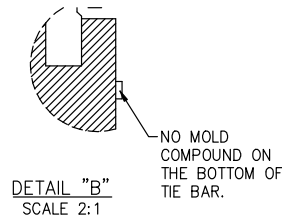
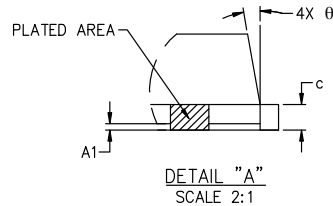
SIDE VIEW



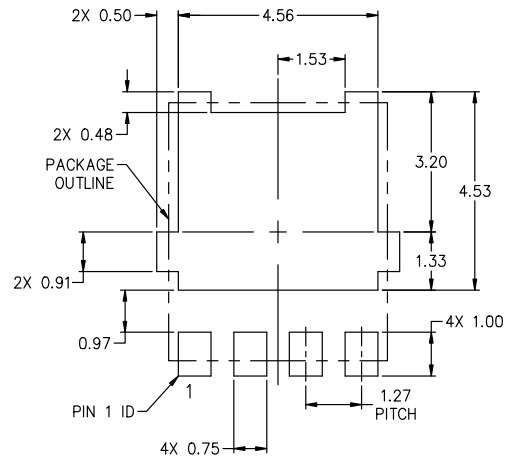
BOTTOM VIEW

## NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

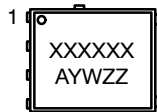


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



## RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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