

MOSFET - Power, Single N-Channel, STD Gate, PQFN88-3L

80 V, 1.0 mohms, 352 A

NVMTS1D1N08X

Features

- Low Q_{RR} , Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC-DC and AC-DC
- Primary Switch in Isolated DC-DC Converter
- Motor Drives
- Automotive 48 V System

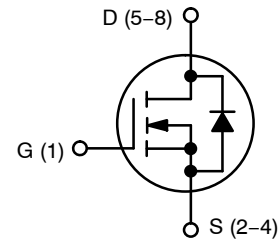
MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	352	A
	$T_C = 100\text{ }^{\circ}\text{C}$		249	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	250	W
Pulsed Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$	I_{DM}	2059	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Continuous Source-Drain Current (Body Diode)	$T_C = 25\text{ }^{\circ}\text{C}$, $V_{GS} = 0\text{ V}$	I_S	346	A
Single Pulse Avalanche Energy ($I_{PK} = 100\text{ A}$)		E_{AS}	500	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$

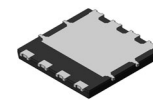
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in², 1 oz. Cu pad
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} is based on started $T_J = 25\text{ }^{\circ}\text{C}$, rated I_{AS} , $V_{DD} = 64\text{ V}$, $V_{GS} = 10\text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
80 V	1.0 m Ω @ $V_{GS} = 10\text{ V}$	352 A

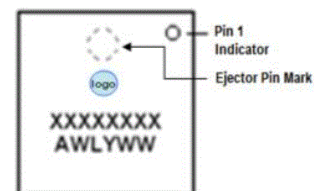


N-CHANNEL MOSFET



TDFNW8
SINGLE COOL
CASE 507AP

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.3	0.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	30		

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ °C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25\text{ °C}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25 °C		47		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, T_J = 25\text{ °C}$			1.0	μA
		$V_{DS} = 80\text{ V}, T_J = 125\text{ °C}$ (Note 4)			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}, T_J = 25\text{ °C}$		0.84	1.0	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 483\text{ μA}, T_J = 25\text{ °C}$	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 483\text{ μA}$		-6.4		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 32\text{ A}$		154		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		8608		pF
Output Capacitance	C_{OSS}			2495		
Reverse Transfer Capacitance	C_{RSS}			37		
Output Charge	Q_{OSS}			178		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DD} = 40\text{ V}, I_D = 32\text{ A}, V_{GS} = 10\text{ V}$		121		nC
Threshold Gate Charge	$Q_{G(TH)}$			26		
Gate-to-Source Charge	Q_{GS}			38		
Gate-to-Drain Charge	Q_{GD}			19		
Gate Plateau Voltage	V_{GP}			4.5		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.5		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 64\text{ V}, I_D = 32\text{ A}, R_G = 2.5\text{ Ω}$		35		ns
Rise Time	t_r			24		
Turn-Off Delay Time	$t_{d(OFF)}$			65		
Fall Time	t_f			13		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}, T_J = 25\text{ °C}$		0.76	0.93	V
		$V_{GS} = 0\text{ V}, I_S = 32\text{ A}, T_J = 125\text{ °C}$		0.60		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = 32\text{ A}, dI/dt = 1000\text{ A/μs}, V_{DD} = 64\text{ V}, T_J = 25\text{ °C}$		34		ns
Charge Time	t_a			19		
Discharge Time	t_b			15		
Reverse Recovery Charge	Q_{RR}			316		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design and is not production tested.

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TYPICAL CHARACTERISTICS

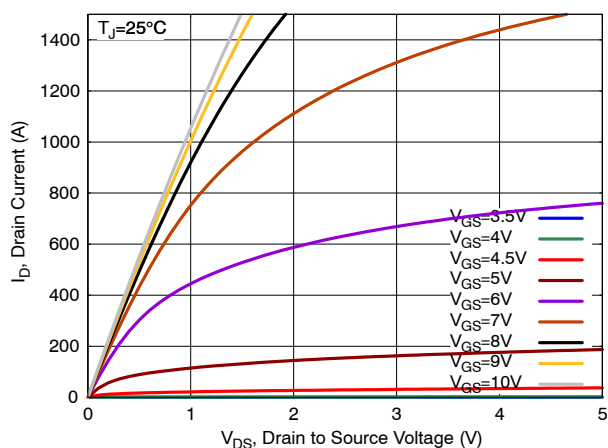


Figure 1. On-Region Characteristics

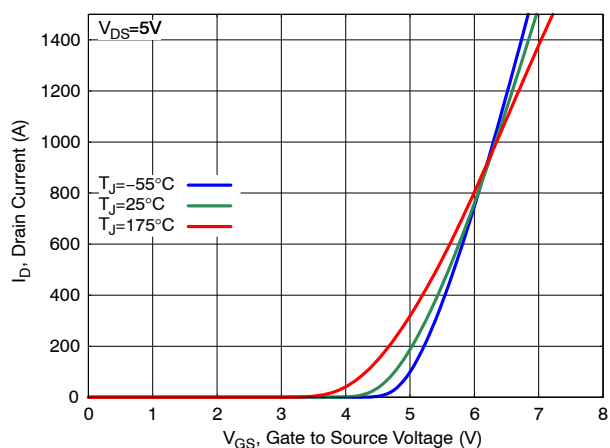


Figure 2. Transfer Characteristics

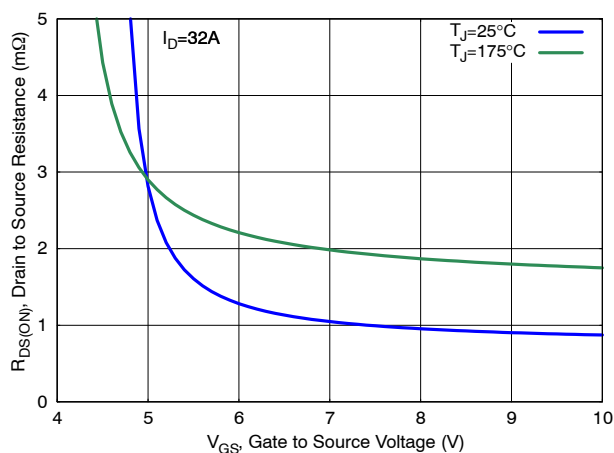


Figure 3. On-Resistance vs. Gate Voltage

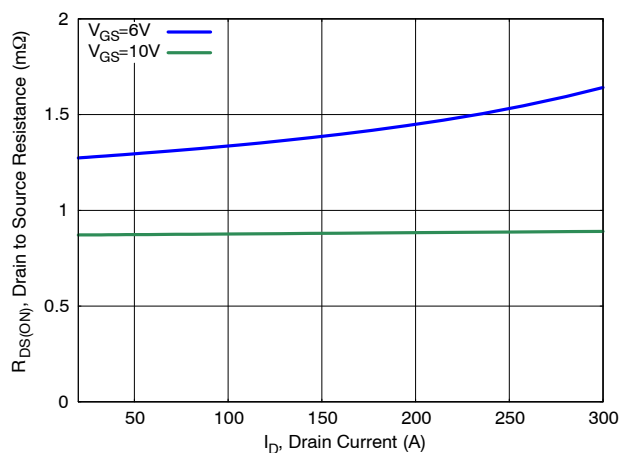


Figure 4. On-Resistance vs. Drain Current

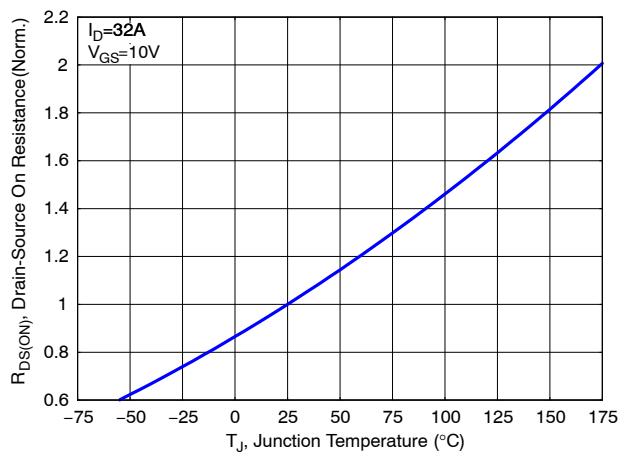


Figure 5. Normalized ON Resistance vs. Junction Temperature

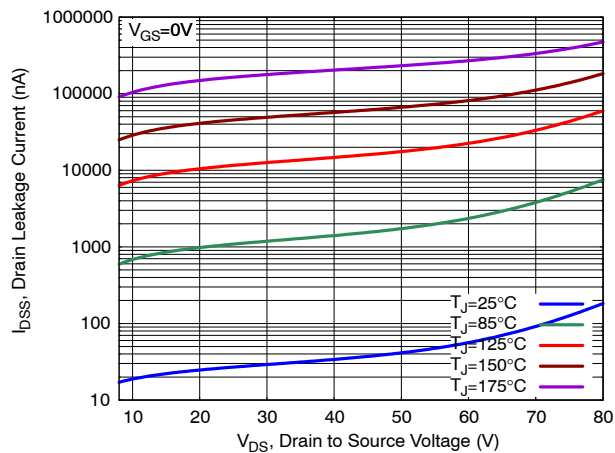


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

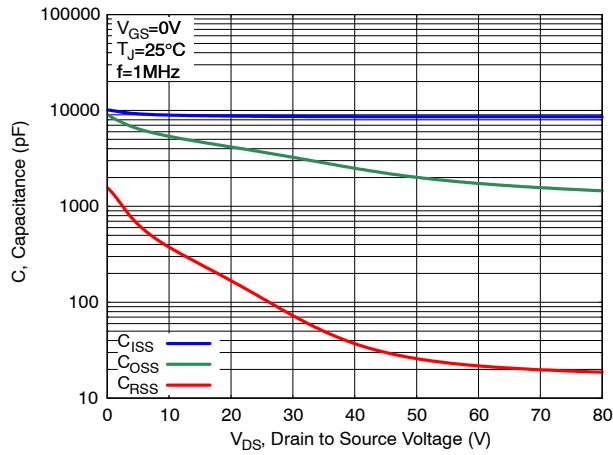


Figure 7. Capacitance Characteristics

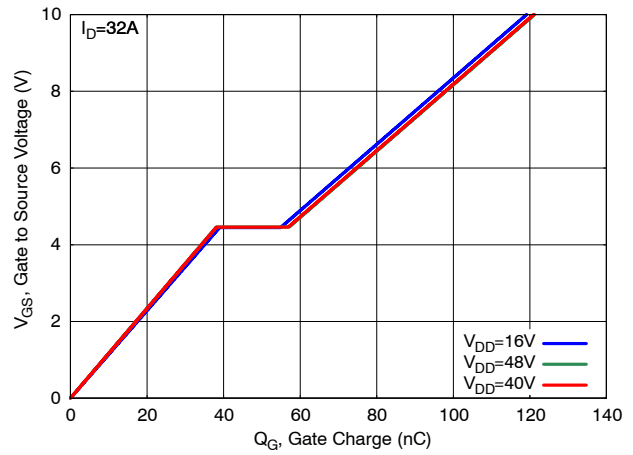


Figure 8. Gate Charge Characteristics

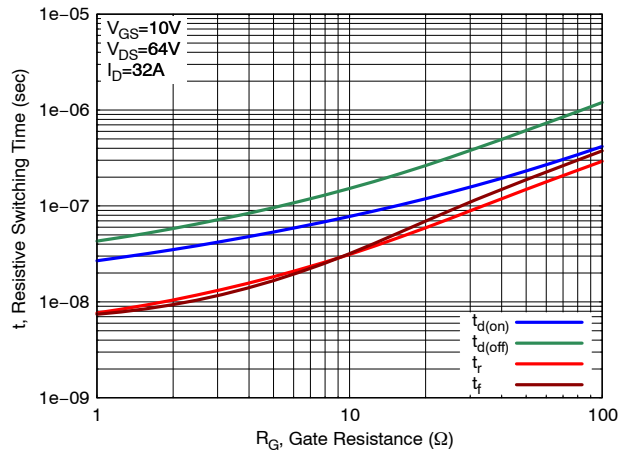


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

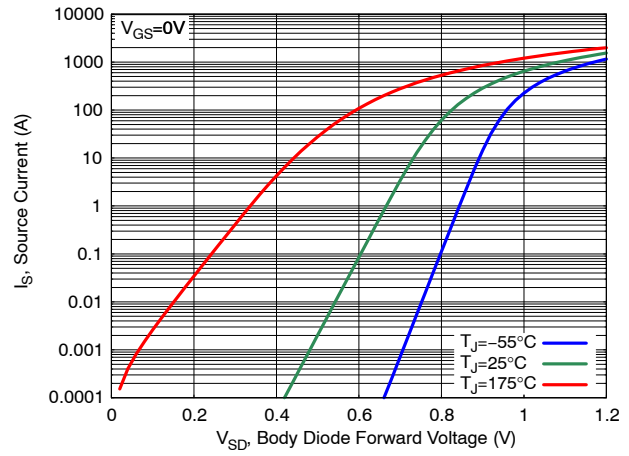


Figure 10. Diode Forward Characteristics

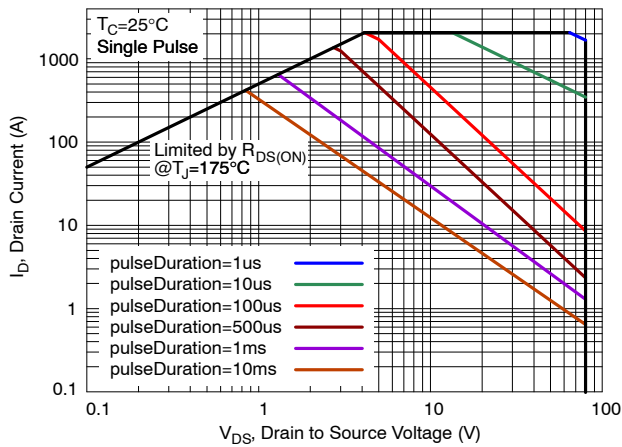


Figure 11. Safe Operating Area (SOA)

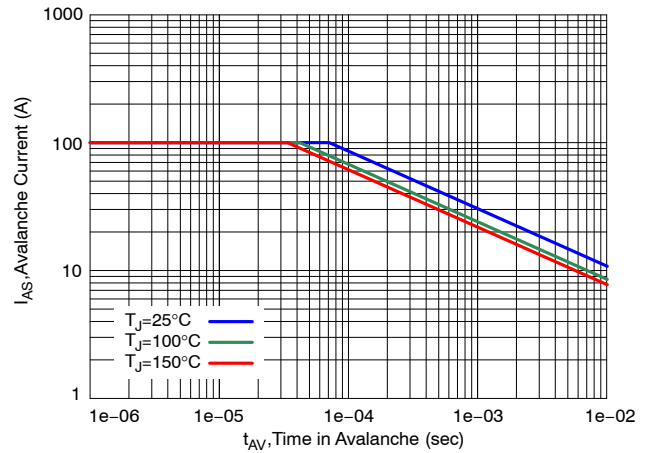


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

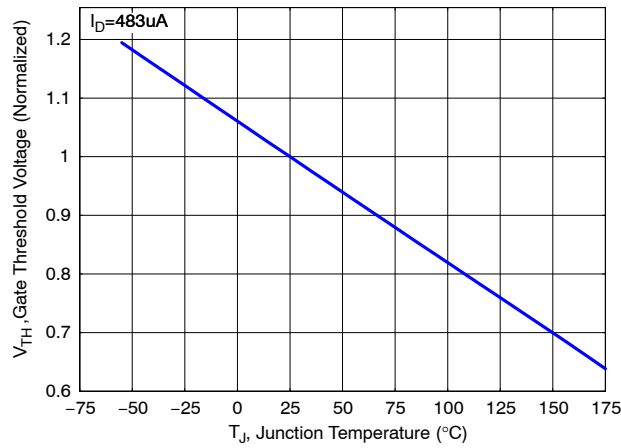


Figure 13. Gate Threshold Voltage vs. Junction Temperature

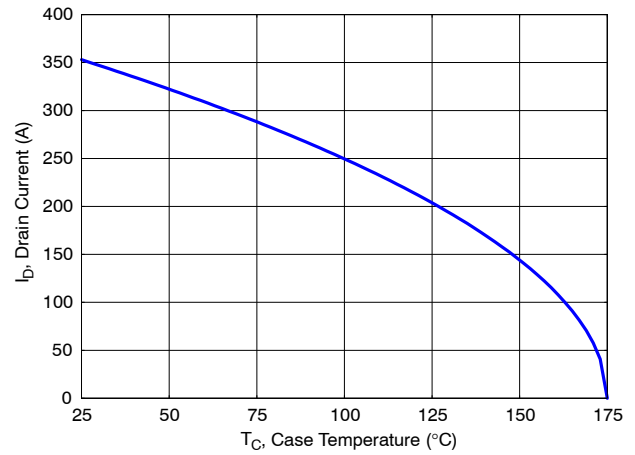


Figure 14. Maximum Current vs. Case Temperature

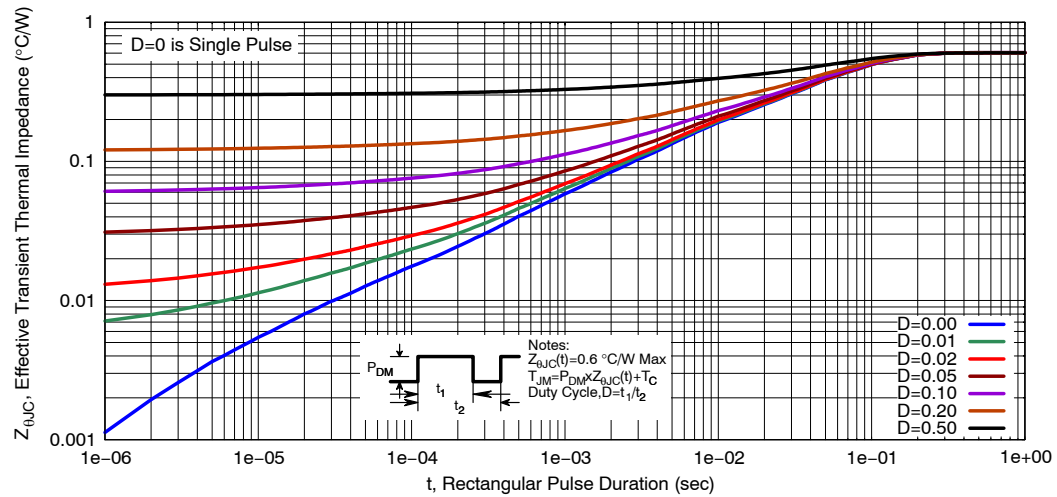


Figure 15. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMTS1D1N08XTXG	1D1N08X	TDFNW8	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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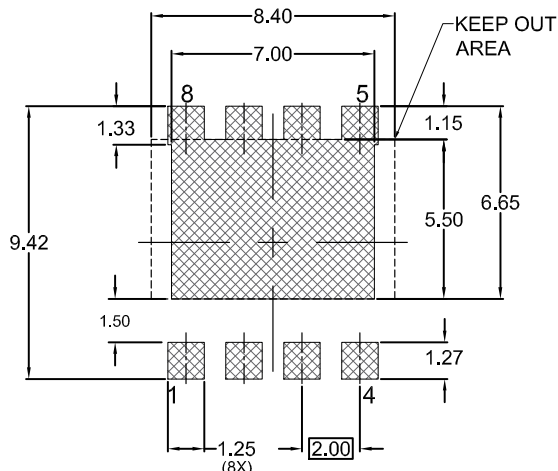
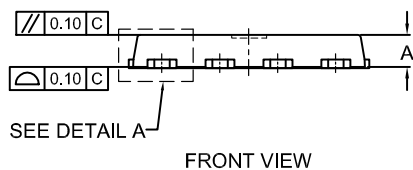
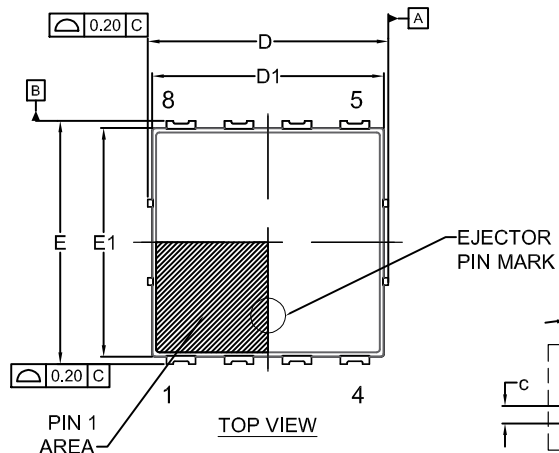
REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release	7/20/2026

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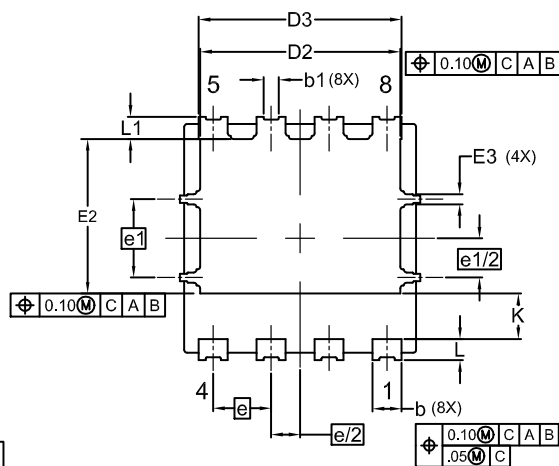
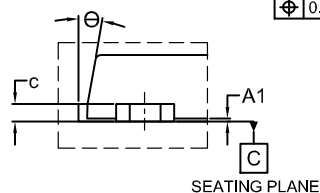
PACKAGE DIMENSIONS

TDFNW8 8.3x8.4, 2.0P, SINGLE COOL
CASE 507AP
ISSUE D



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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