

MOSFET – Power, Single N-Channel

60 V, 4.0 mΩ, 100 A



ON Semiconductor®

www.onsemi.com

NVMYS4D1N06CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPACK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 100 | A |
| | | $T_C = 100^\circ\text{C}$ | 71 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 79 | W |
| | | $T_C = 100^\circ\text{C}$ | 40 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 22 | A |
| | | $T_A = 100^\circ\text{C}$ | 15 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 3.7 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.8 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 820 | A | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 100 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_{L(pk)} = 5 \text{ A}$) | E_{AS} | 185 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

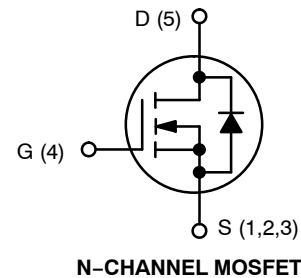
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State | $R_{\theta JC}$ | 1.9 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 39 | |

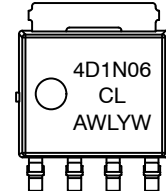
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(ON) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 60 V | 4.0 mΩ @ 10 V | 100 A |
| | 5.7 mΩ @ 4.5 V | |



LFPACK4
CASE 760AB

MARKING DIAGRAM



4D1N06CL = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMYS4D1N06CL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|---|---------------------------|-----|-----|----------------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | 28 | | mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 10 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 250 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|--|------------------|--|-----|------|-----|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 80\ \mu\text{A}$ | 1.2 | | 2.0 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | -5.4 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ | | 3.3 | 4.0 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$ | | 4.6 | 5.7 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 15\text{ V}, I_D = 50\text{ A}$ | | 105 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|--------------|--|--|------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$ | | 2200 | | pF |
| Output Capacitance | C_{OSS} | | | 900 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 17 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 16 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 34 | | |
| Threshold Gate Charge | $Q_{G(TH)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 1.5 | | |
| Gate-to-Source Charge | Q_{GS} | | | 5.6 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 5.1 | | |
| Plateau Voltage | V_{GP} | | | 2.8 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|--------------|---|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\ \Omega$ | | 10 | | ns |
| Rise Time | t_r | | | 15 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 24 | | |
| Fall Time | t_f | | | 5.0 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|--|------|-----|----|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.88 | 1.2 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.78 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$ | | | 41 | | ns |
| Charge Time | t_a | | | | 21 | | |
| Discharge Time | t_b | | | | 20 | | |
| Reverse Recovery Charge | Q_{RR} | | | | 32 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

NVMYS4D1N06CL

TYPICAL CHARACTERISTICS

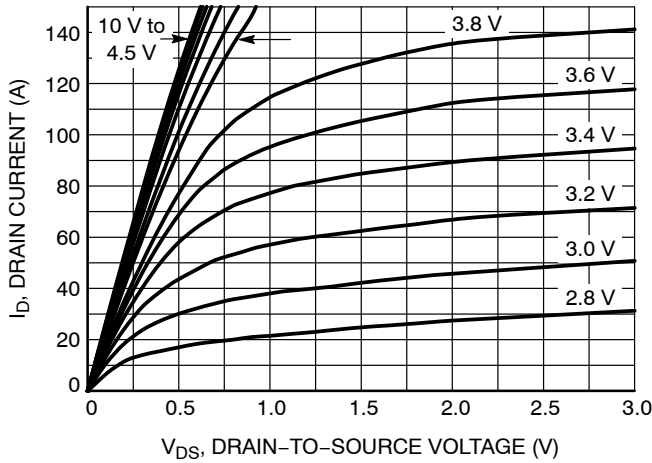


Figure 1. On-Region Characteristics

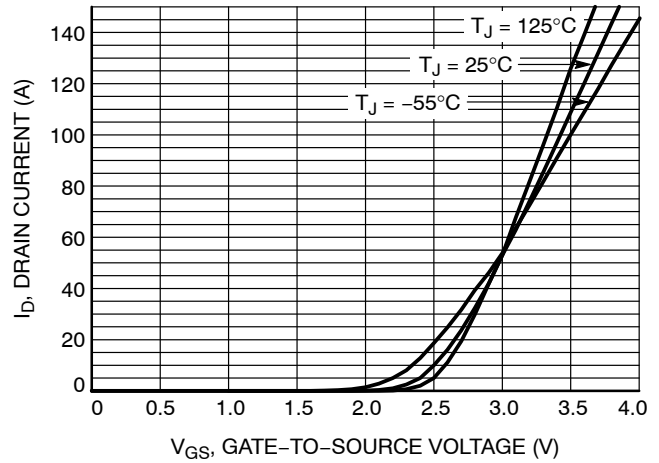


Figure 2. Transfer Characteristics

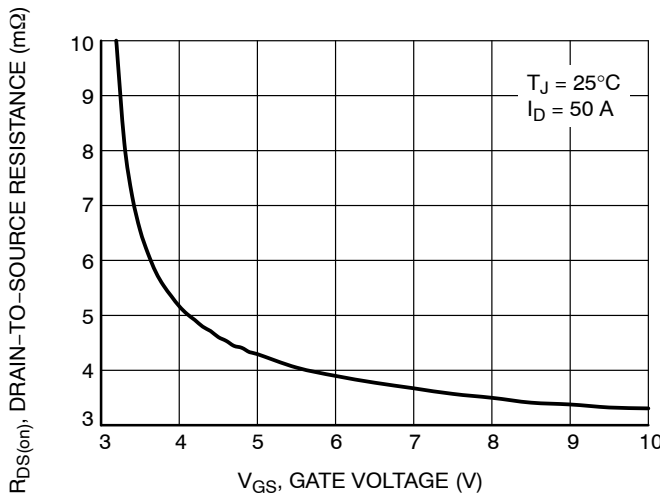


Figure 3. On-Resistance vs. Gate-to-Source Voltage

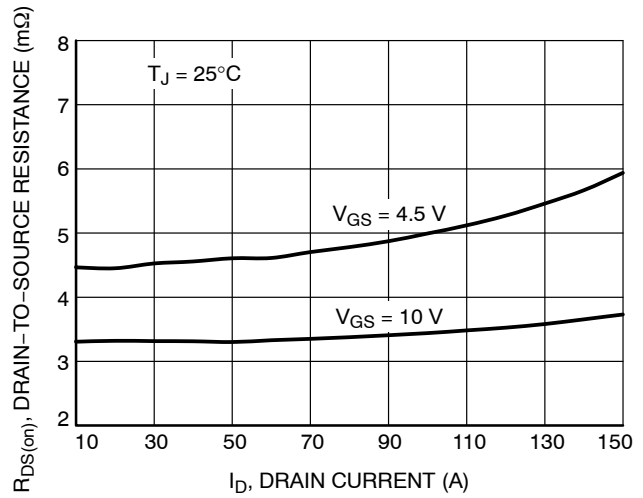


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

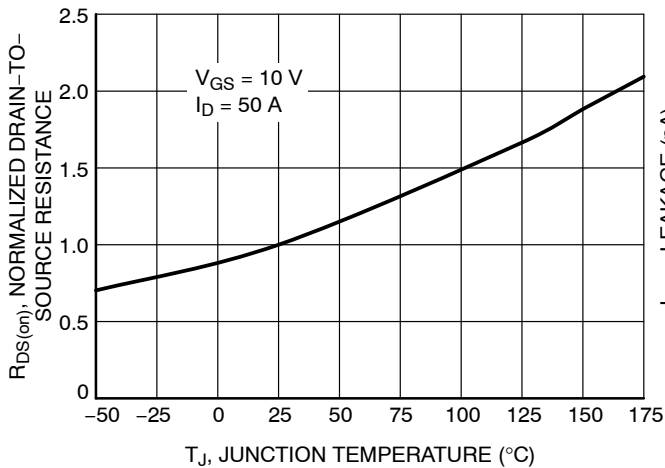


Figure 5. On-Resistance Variation with Temperature

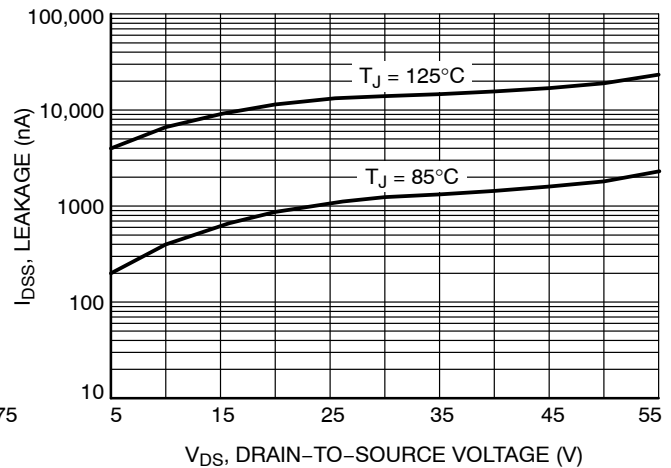


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

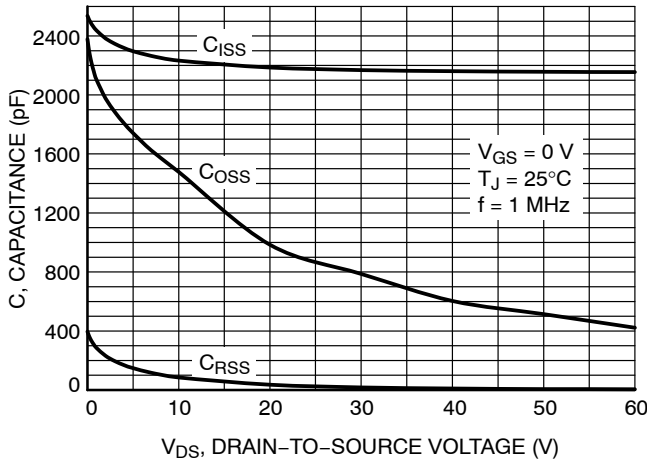


Figure 7. Capacitance Variation

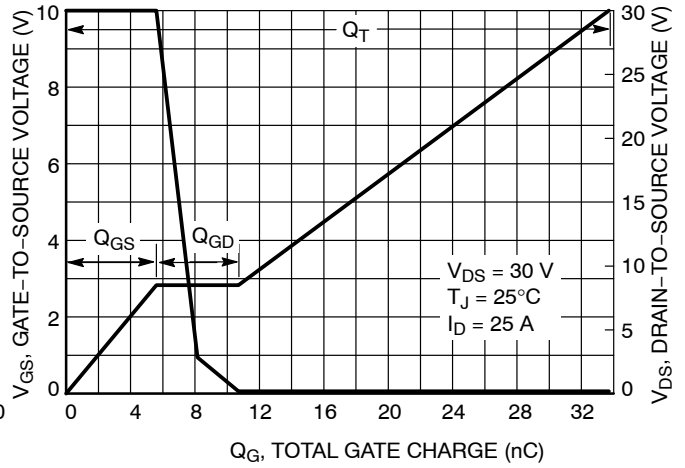


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

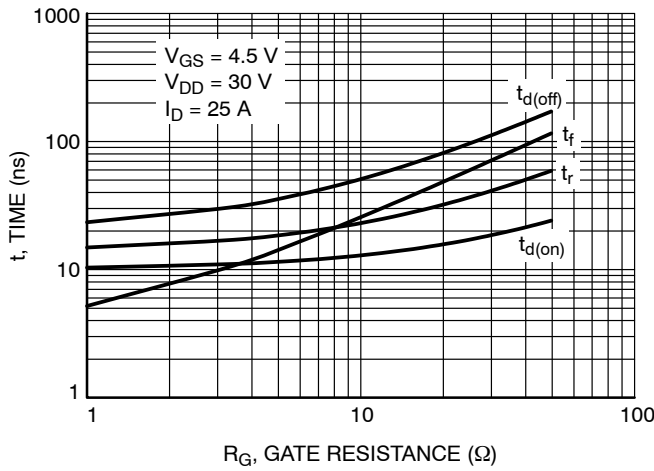


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

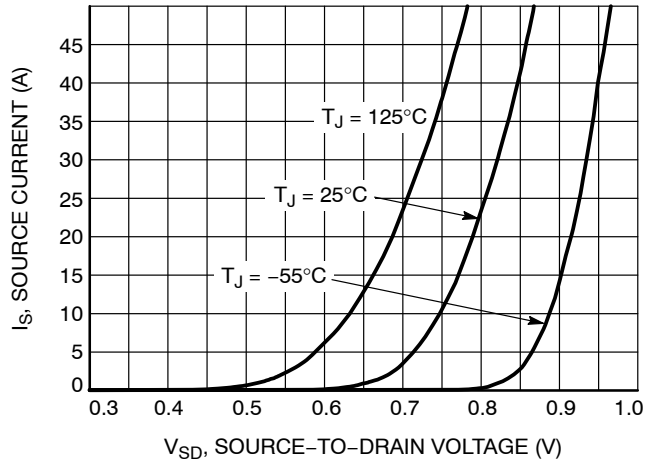


Figure 10. Diode Forward Voltage vs. Current

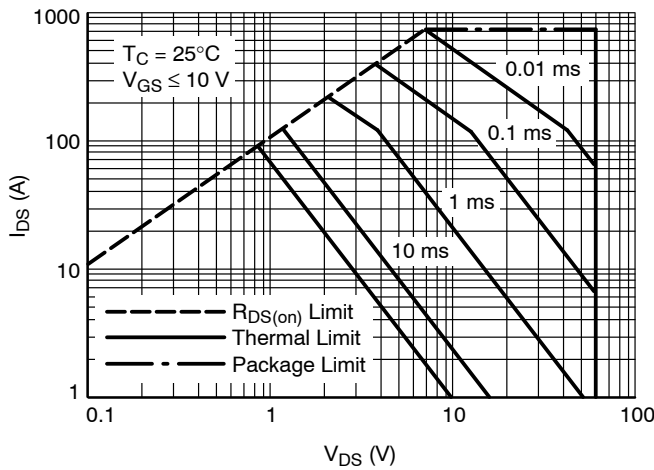


Figure 11. Safe Operating Area

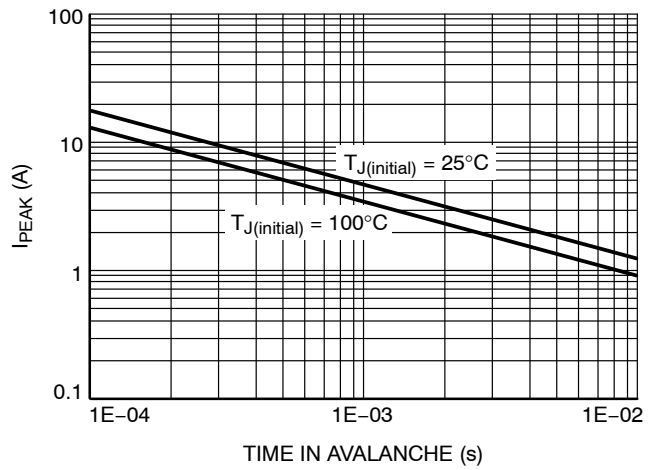


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMYS4D1N06CL

TYPICAL CHARACTERISTICS

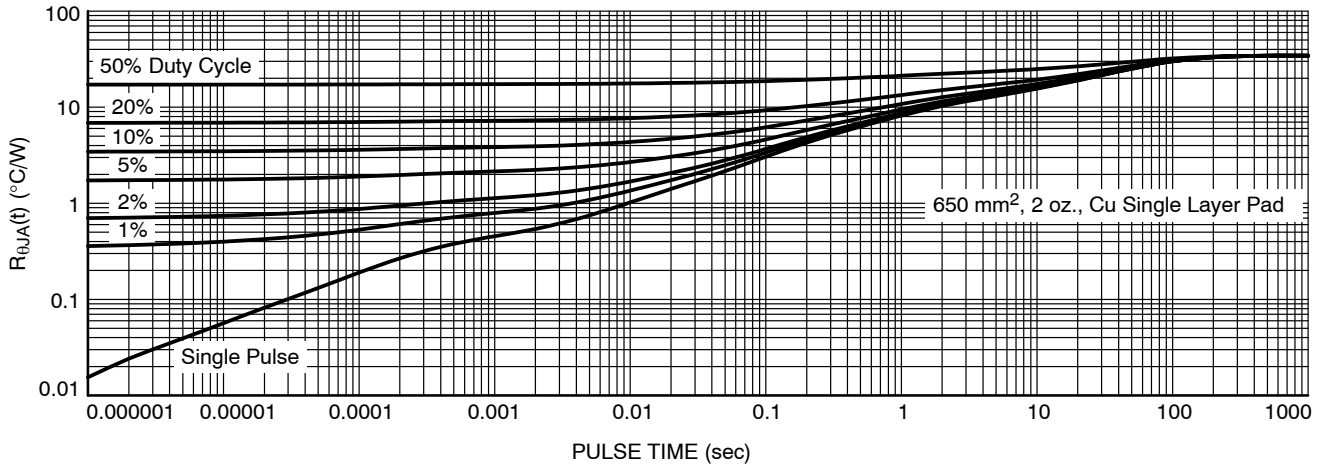


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|----------|---------------------|-----------------------|
| NVMYS4D1N06CLTWG | 4D1N06CL | LFP4K4 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

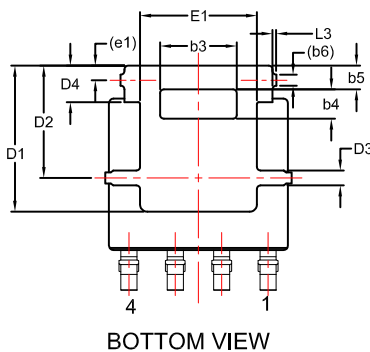
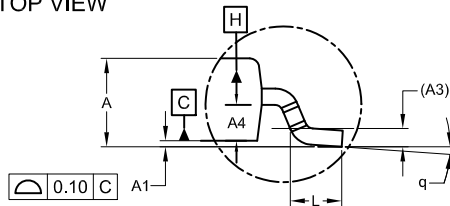


LFPAK4 5x6 CASE 760AB ISSUE C

DATE 19 NOV 2019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.



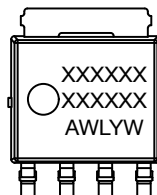
DETAIL 'A'
SCALE: 2:1



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

| UNIT IN MILLIMETER | | | |
|--------------------|-----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.10 | 1.20 | 1.30 |
| A1 | 0.00 | 0.08 | 0.15 |
| A2 | 1.10 | 1.15 | 1.20 |
| A3 | 0.25 REF | | |
| A4 | 0.45 | 0.50 | 0.55 |
| b | 0.40 | 0.45 | 0.50 |
| b2 | 3.80 | 4.10 | 4.40 |
| b3 | 2.00 | 2.10 | 2.20 |
| b4 | 0.70 | 0.80 | 0.90 |
| b5 | 0.55 | 0.65 | 0.75 |
| b6 | 0.31 REF | | |
| c | 0.19 | 0.22 | 0.25 |
| c2 | 0.19 | 0.22 | 0.25 |
| D | 4.05 | 4.15 | 4.25 |
| D1 | 3.80 | 4.00 | 4.20 |
| D2 | 3.00 | 3.10 | 3.20 |
| D3 | 0.30 | 0.40 | 0.50 |
| D4 | 0.90 | 1.00 | 1.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 3.10 | 3.20 | 3.30 |
| E2 | 5.00 | 5.15 | 5.30 |
| e | 1.27 BSC | | |
| 1/2e | 0.635 BSC | | |
| e1 | 0.40 REF | | |
| H | 6.00 | 6.15 | 6.30 |
| L | 0.40 | 0.65 | 0.85 |
| L1 | 0.80 | 0.90 | 1.00 |
| L2 | 0.90 | 1.10 | 1.30 |
| L3 | 0.00 | 0.10 | 0.20 |
| q | 0° | 4° | 8° |

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98AON82777G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | LFPAK4 5x6 | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales