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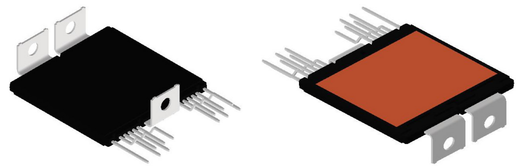
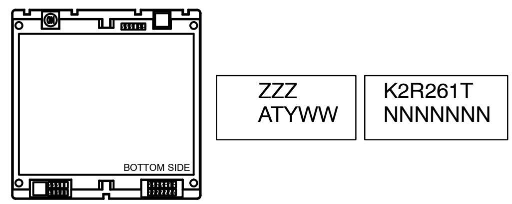
Silicon Carbide (SiC) Module – EliteSiC Power Module for Traction Inverter, Single-Side Cooling, 2.6 mohm, 1200 V, Half-Bridge, 90° Power Tabs

NVVR26A120M1WST



AHPM15−CDA MODULE
CASE MODHG

MARKING DIAGRAM



ZZZ	=	Assembly Lot Code
K2R261T	=	Marking Value
AT	=	Assembly & Test Location
Y	=	Year
WW	=	Work Week
NNNN	=	Serial Number

Product Description

The NVVR26A120M1WST is part of the EliteSiC power module for traction inverter, a revolutionary high mobility compound semiconductor product family that offers increased performance, better efficiency, and higher power density in similar and highly compatible packaging solutions. The module integrates 1200 V SiC MOSFET in a half−bridge configuration. To enhance reliability and thermal performance, sintering technology is applied for die attach. The module is designed to meet the AQG324 standard.

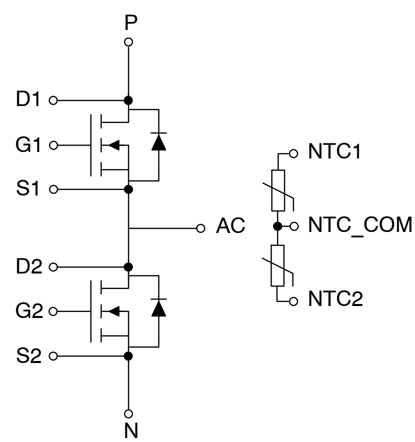
Features

- Ultra Low $R_{DS(on)}$
- Aluminum Nitride Isolator
- Ultra−low Stray Inductance ~ 7.1 nH
- $T_{vj.Max}$ = 175°C for Continuous Operation
- Automotive Grade SiC MOSFET Chip Technologies
- Sintered Die Technology for High Reliability Performance
- Automotive Module AQG324 Compliant
- PPAP Capable

Applications

- Automotive EV/HEV− Traction Inverter

PIN CONFIGURATION



ORDERING INFORMATION

Device	Package	Shipping
NVVR26A120M1WST	A1HPM	Tube

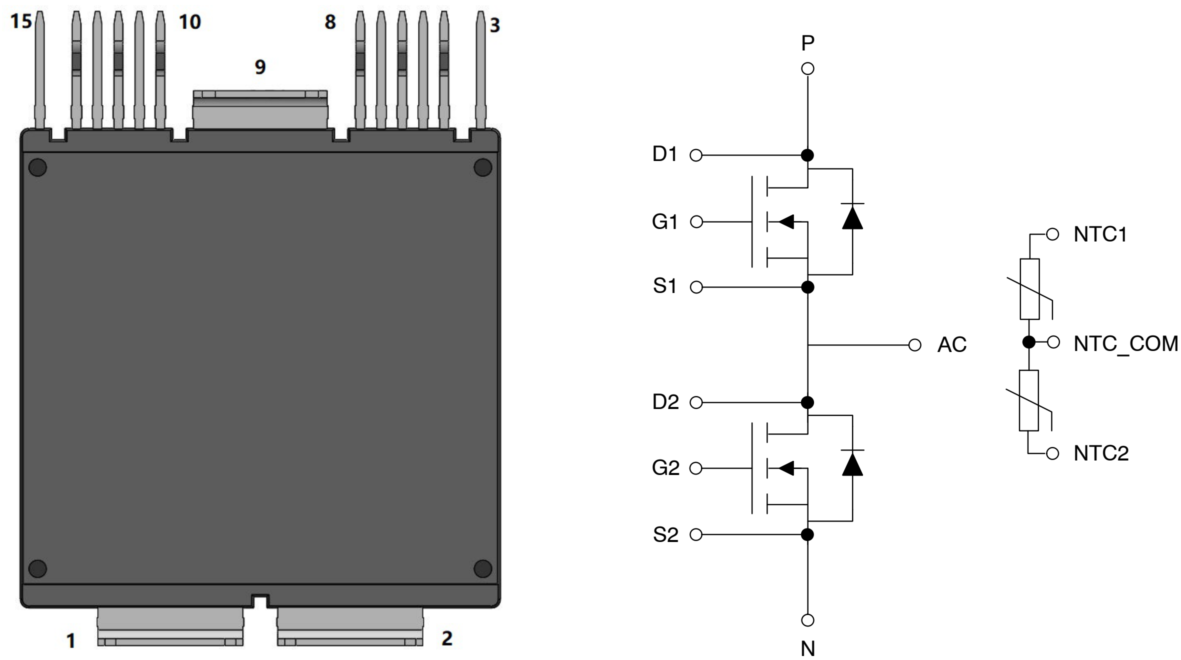


Figure 1. Pin Description

PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Name	Pin Functional Description
1	N	Negative Power Terminal
2	P	Positive Power Terminal
3	D1	High Side MOSFET (Q1) Drain Sense
4	N/C	No Connection
5	S1	High Side MOSFET (Q1) Source
6	G1	High Side MOSFET (Q1) Gate
7	N/C	No Connection
8	N/C	No Connection
9	AC	Phase Output
10	NTC1	NTC 1
11	S2	Low Side MOSFET (Q2) Source
12	G2	Low Side MOSFET (Q2) Gate
13	NTC2	NTC 2
14	NTC_COM	NTC common
15	D2	Low Side MOSFET (Q2) Drain Sense

Materials

DBC Substrate: AlN isolated substrate, basic isolation, and copper on both sides
Lead frame: Copper, with tin electro−plating

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0

MODULE CHARACTERISTICS (T_{vj} = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Rating	Unit
T_{vj}	Operating Junction Temperature	−40 to 175	°C
T_{STG}	Storage Temperature Range	−40 to 125	°C
V_{ISO}	Isolation Voltage (AC, 50 Hz, 5 s)	4200	V
Ls_{DS}	Stray Inductance	7.1	nH
$R_{DD'+SS'}$	Module Lead Resistance, Terminal to Chip	0.3	mΩ
G	Module Weight	48	g
CTI	Comparative Tracking Index	>600	–
Creepage	Minimum: Terminal to Terminal	5.0	mm
Clearance	Minimum: (Note 1) Terminal to Terminal	3.2	mm
M	M5 DIN 439B Screws for Module Terminals, Max. Torque	2.2	Nm

1. Verified by design/characterization, not tested.

ABSOLUTE MAXIMUM RATINGS (T_{vj} = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Rating	Unit
V_{DS}	Drain−Source Voltage	1200	V
V_{GS}	Gate−Source Voltage	+25/−10	V
I_{DS}	Continuous DC Current, V_{GS} = 20 V, T_{vj} = 175°C, T_F = 65°C @ 10LPM, using Ref. Heatsink (Note 2)	400	A
$I_{DS.pulsed}$	Pulsed Drain−Source Current, V_{GS} = 20 V, limited by $T_{vj.Max}$	800	A
$I_{SD.BD}$	DC Current in Body Diode, V_{GS} = −5 V, T_{vj} = 175°C, T_F = 65°C @ 10LPM, using Ref. Heatsink (Note 2)	270	A
$I_{SD.pulsed}$	Pulsed Body Diode Current, V_{GS} =−5 V, limited by $T_{vj.Max}$	800	A
Ptot	Total Power Dissipation $T_{vj.Max}$ = 175°C, T_F = 65°C, Ref. Heatsink (typ)	1000	W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Verified by design / not by test.

MOSFET CHARACTERISTICS (T_{vj} = 25°C, Unless Otherwise Specified)

Parameter		Conditions		Min	Typ	Max	Unit
$R_{DS(ON)}$	Drain–to–Source On Resistance (Terminal)	V_{GS} = 20V, I_D = 400A	T_{vj} = 25°C T_{vj} = 175°C	–	2.6 4.6	–	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS} , I_D = 150 mA		2.1	3.2	–	V
g_{fs}	Forward Transconductance	V_{DS} = 10 V, I_D = 400 A		–	170	–	S
Q_G	Total Gate Charge	V_{GS} = –5/+20 V, V_{DS} = 800 V, I_D = 400 A		–	1.75	–	µC
$R_{g.int}$	Internal Gate Resistance			–	2.1	–	Ω
C_{iss}	Input Capacitance	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz		–	31.7	–	nF
C_{oss}	Output Capacitance			–	2.2	–	nF
C_{rss}	Reverse Transfer Capacitance			–	0.22	–	nF
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V	T_{vj} = 25°C T_{vj} = 175°C	–	– 13.1	250 –	µA
I_{GSS}	Gate–Source Leakage Current	V_{GS} = 20/–5 V, V_{DS} = 0 V				±700	nA
$T_{d.on}$	Turn On Delay, Inductive Load	I_{DS}= 400 A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Rg.on = 3 Ω	T_{vj} = 25°C T_{vj} = 175°C	–	125 115	–	ns
T_r	Rise Time, Inductive Load	I_{DS} = 400 A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Rg.on = 3Ω	T_{vj} = 25°C T_{vj} = 175°C	–	59 54	–	ns
$T_{d.off}$	Turn Off Delay, Inductive Load	I_{DS} = 400 A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Rg.off = 1 Ω	T_{vj} = 25°C, T_{vj} = 175°C	–	220 228	–	ns
T_f	Fall Time, Inductive Load	I_{DS} = 400 A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Rg.off = 1 Ω	T_{vj} = 25°C T_{vj} = 175°C	–	51 61	–	ns
E_{ON}	Turn–On Switching Loss (including diode reverse recovery loss)	I_{DS} = 400 A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Ls = 17 nH, Rg.on = 3Ω	di/dt = 8.4 A/ns, T_{vj} = 25°C di/dt = 9.7 A/ns, T_{vj} = 175°C	–	26 28	–	mJ
E_{OFF}	Turn–Off Switching Loss	I_{DS} = 400A, V_{DS} = 800 V, V_{GS} = +20/–5 V, Ls =17 nH, Rg.off = 1 Ω	dv/dt = 19.8 V/ns, T_{vj} = 25°C dv/dt = 16.8 V/ns, T_{vj} = 175°C	–	14 17	–	mJ
E_{sc}	Short Circuit Energy Withstand	V_{GS} = 20 V, V_{DS} = 800 V	T_{vj} = 25°C T_{vj} = 175°C	–	12 11	–	J

BODY DIODE CHARACTERISTICS (T_{vj} = 25°C, Unless Otherwise Specified)

Parameters		Conditions		Min	Typ	Max	Unit
V_{SD}	Diode Forward Voltage (Terminal)	V_{GS} = −5 V, I_{SD} = 400 A	T_{vj} = 25°C T_{vj} = 175°C	–	3.8 3.3	–	V
E_{rr}	Reverse Recovery Energy	I_{SD} = 400 A, V_R = 800 V, V_{GS} = −5 V, Ls = 17 nH, Rg.on = 3 Ω	di/dt = 8.4 A/ns, T_{vj} = 25°C di/dt = 9.7 A/ns, T_{vj} = 175°C	–	0.4 2.1	–	mJ
Q_{RR}	Recovered Charge	I_{SD} = 400 A, V_R = 800 V, V_{GS} = −5 V, Rg.on = 3 Ω	T_{vj} = 25°C T_{vj} = 175°C	–	2.3 8.6	–	μC
I_{RR}	Peak Reverse Recovery Current	I_{SD} = 400 A, V_R = 800 V, V_{GS} = −5 V, Rg.on = 3 Ω	T_{vj} = 25°C T_{vj} = 175°C	–	527 650	–	A

NTC SENSOR CHARACTERISTICS (T_{vj} = 25°C, Unless Otherwise Specified)

Parameters		Conditions	Min	Typ	Max	Unit
R25	Rated Resistance	Tc = 25°C	–	10	–	kΩ
ΔR/R	Deviation of R100	Tc = 100°C, R100 = 877 Ω	−3	–	+3	%
P25	Power Dissipation	Tc = 25°C	–	–	125	mW
B25/85	B−Value	R = R25 exp [B25/85 (1/T−1/298)]	−1%	3610	+1%	K

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{th,J-C}$	FET Junction to Case		–	0.025	0.028	°C/W
$R_{th,J-F}$	FET Junction to Fluid	R_{th}, Junction to Fluid, 10 L/min, 65°C, 50/50 EGW, Ref. Heatsink	–	0.11	–	°C/W

TYPICAL CHARACTERISTICS

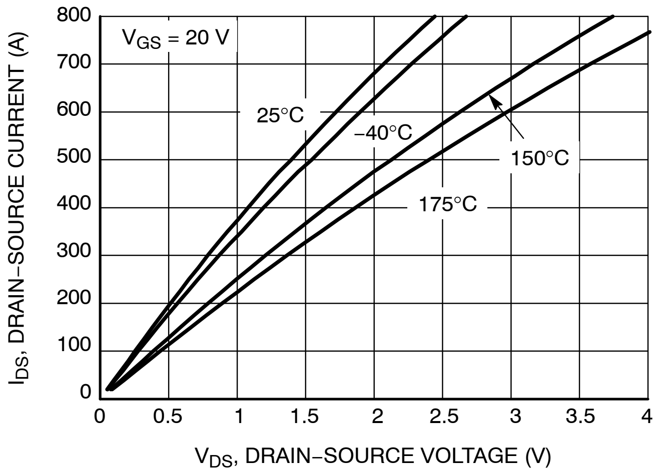


Figure 2. Output Characteristics

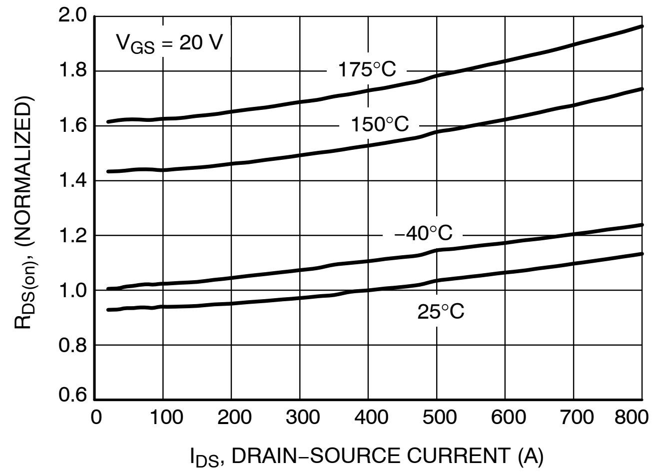


Figure 3. Normalized On−state Resistance vs. Drain Current

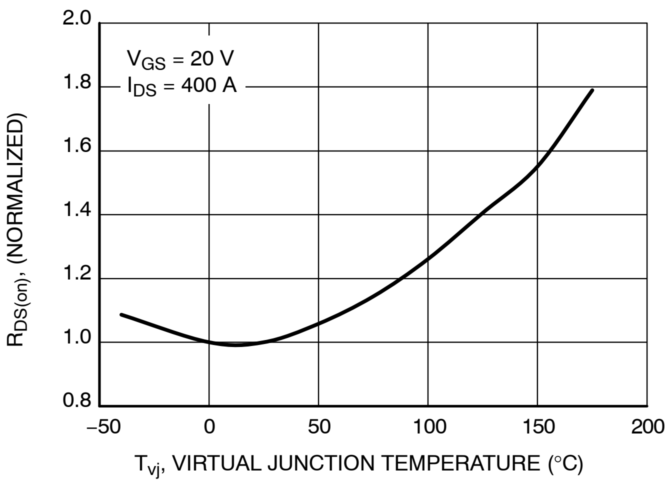


Figure 4. Normalized On−state Resistance vs. Temperature

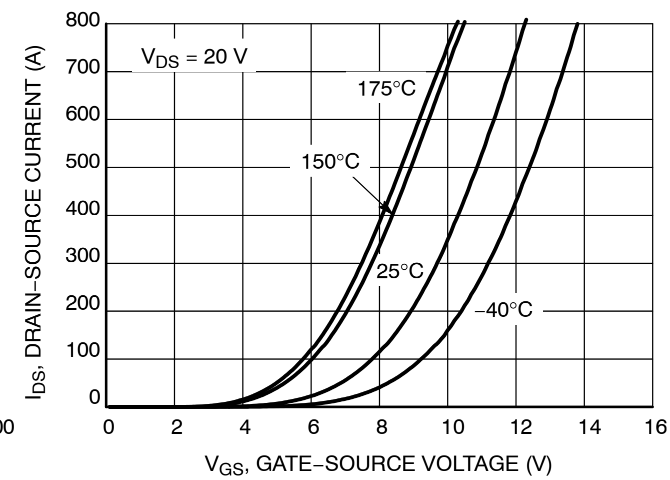


Figure 5. Transfer Characteristic

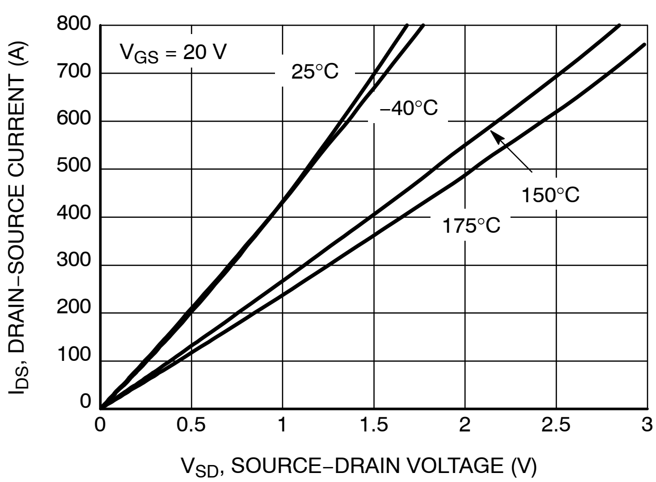


Figure 6. 3rd Quadrant Characteristic at V_{GS} = 20 V

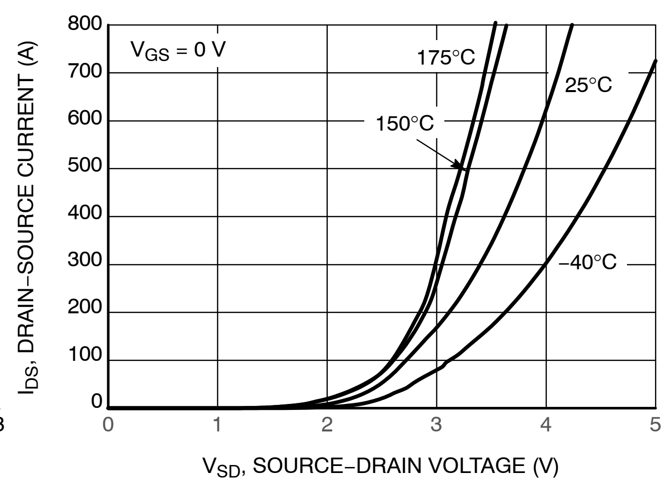


Figure 7. 3rd Quadrant Characteristic at V_{GS} = 0 V

TYPICAL CHARACTERISTICS

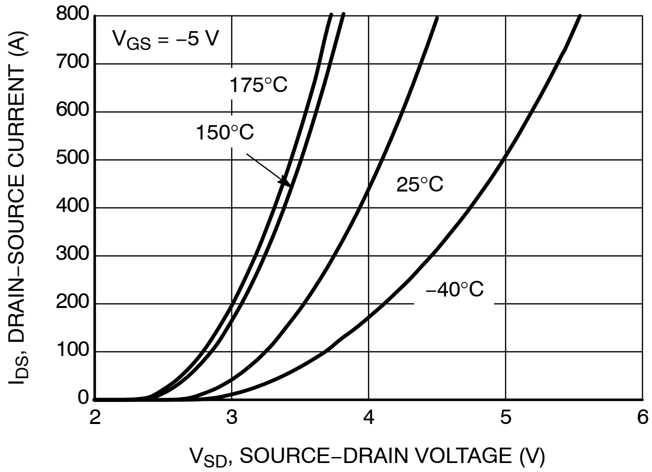


Figure 8. 3rd Quadrant Characteristic at V_{GS} = −5 V

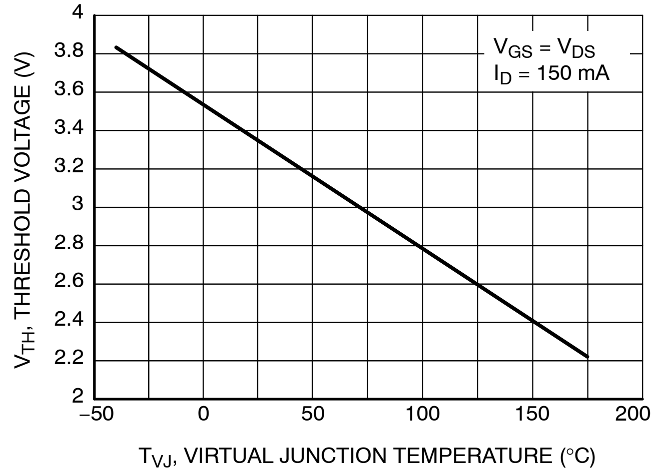


Figure 9. Gate Threshold Voltage vs. Temperature

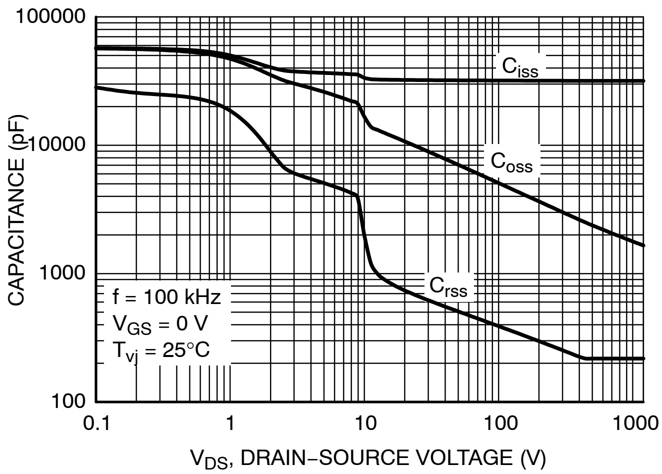


Figure 10. Typical Capacitance vs. Drain−Source Voltage

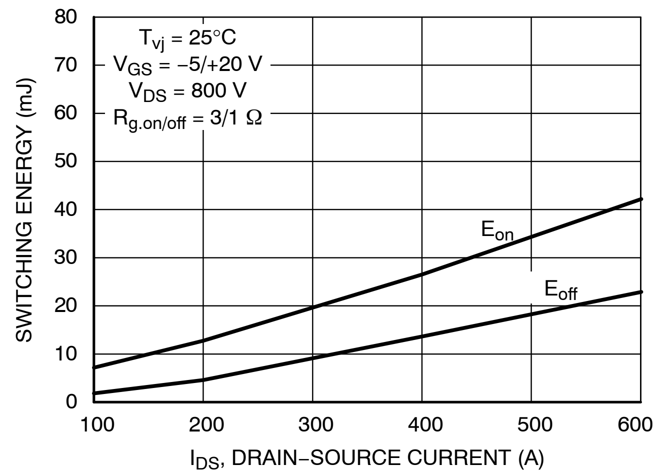


Figure 11. Switching Energies at 25°C

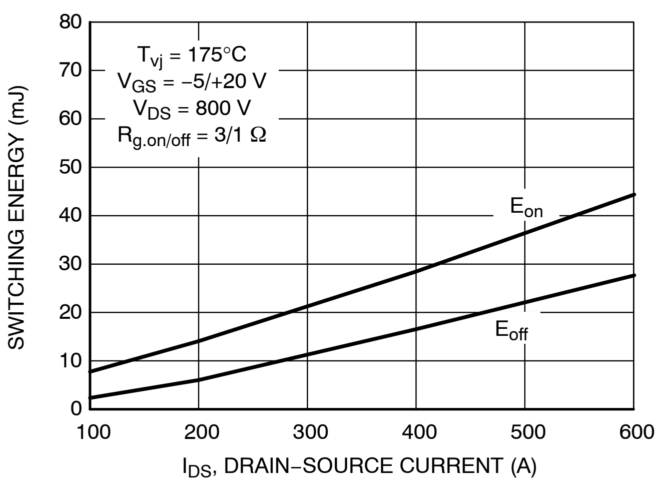


Figure 12. Switching Energies at 175°C

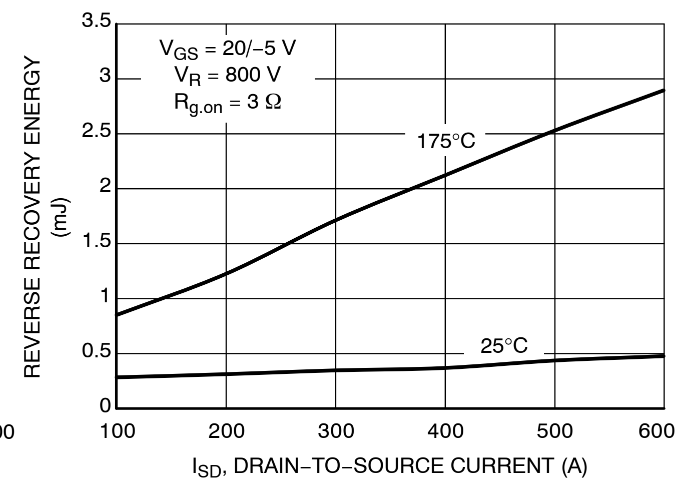


Figure 13. Reverse Recovery Energy vs. Drain−Source Current

TYPICAL CHARACTERISTICS

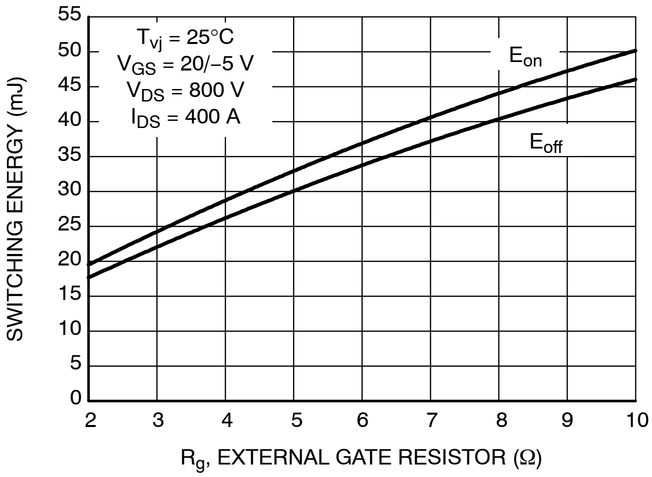


Figure 14. Switching Energies vs. External Gate Resistor

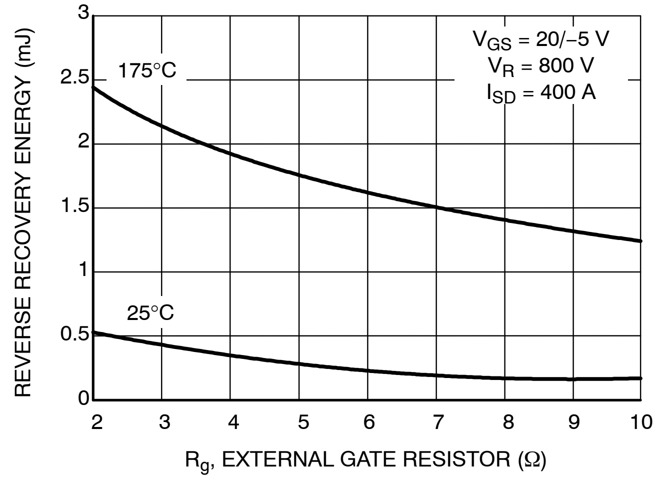


Figure 15. Reverse Recovery Energy vs External Gate Resistor

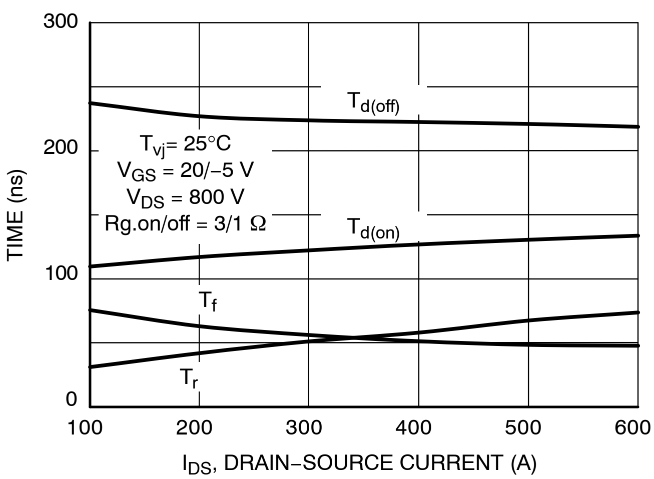


Figure 16. Timing Characteristics vs. Drain−Source Current

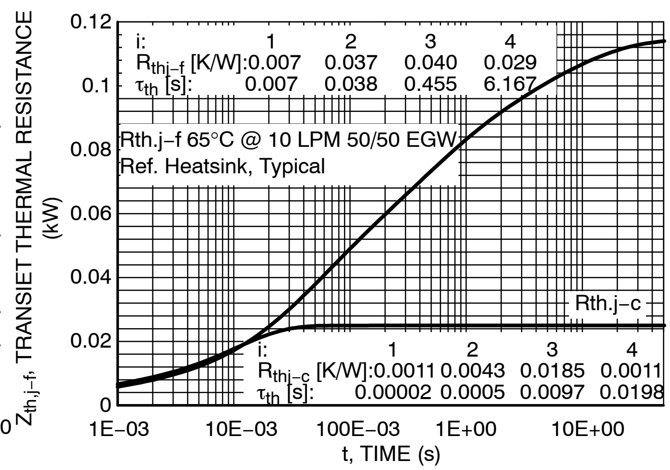


Figure 17. Typical Thermal Impedance

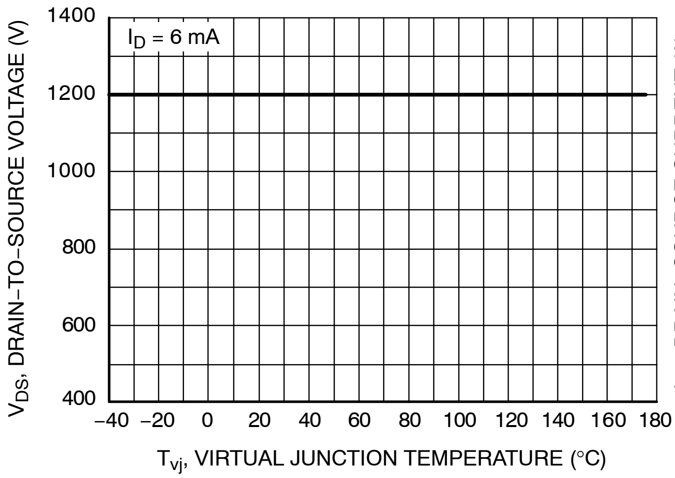


Figure 18. MOSFET Breakdown Voltage vs. T_{VJ}

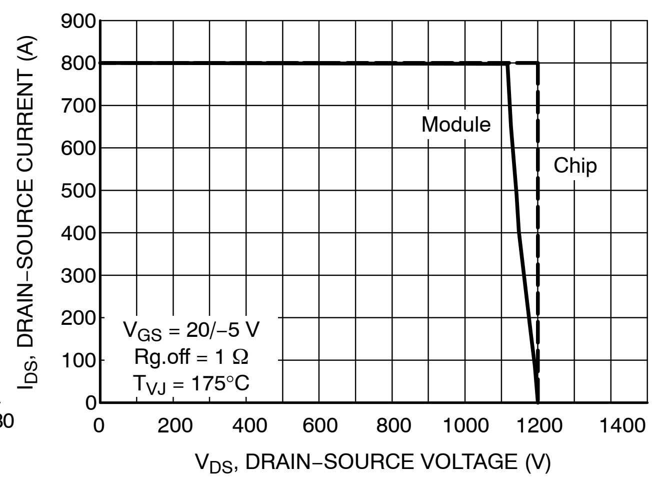


Figure 19. MOSFET RBSOA of Chip and Module

TYPICAL CHARACTERISTICS

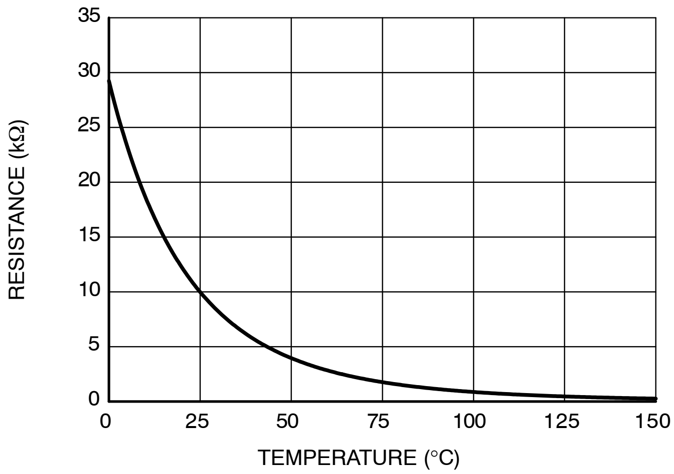


Figure 20. NTC Resistance vs. Temperature

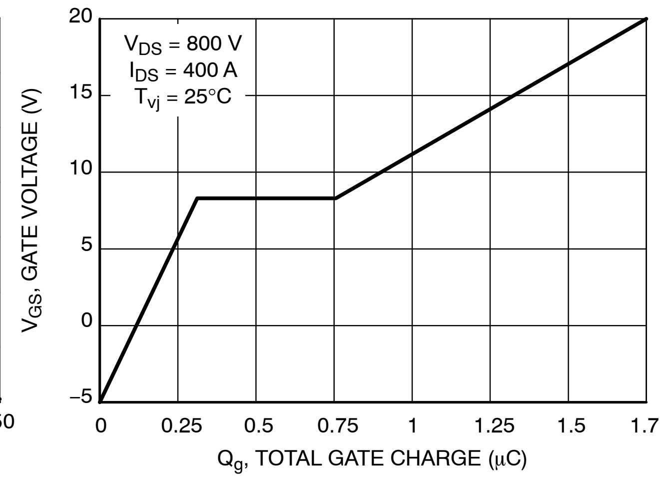


Figure 21. Gate Charge vs. Gate−Source

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