MOSFET – Power, N-Channel

60 V, 0.95 mΩ

PCFA86561F

ON Semiconductor®

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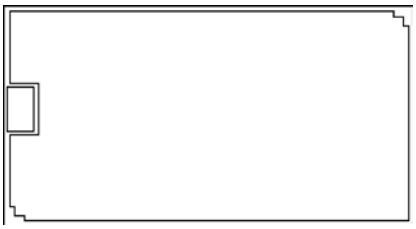
Features

- Typical $R_{DS(on)}$ = 0.75 mΩ at V_{GS} = 10 V
- Typical $Q_{g(tot)}$ = 170 nC at V_{GS} = 10 V
- AEC−Q101 Qualified and PPAP Capable
- RoHS Compliant



DIMENSION (μm)

Die Size	6604 x 3683
Die Size (Sawn)	6584 ±15 x 3663 ±15
Source Attach Area	6405 x 3455
Gate Attach Area	446.3 x 715
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu
Drain: Ti−NiV−Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch
Wafer sawn on UV Tape
Bad dice identified in inking
Gross Die Counts: 1038

The Chip is 100% Probed to Meet the Conditions and Limits Specified at T_J = 25°C.

ORDERING INFORMATION

Device	Package
PCFA86561F	Wafer Sawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 60 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
*$R_{DS(on)}$	Bare Die Drain to Source On Resistance	I_D = 5 A, V_{GS} = 10 V	–	0.75	0.95	mΩ
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 5 A, V_{GS} = 0 V	–	–	1.25	V

*Accurate $R_{DS(on)}$ test at die level is not feasible as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

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ABSOLUTE MAXIMUM RATINGS in Reference to the FDBL86561−F085 electrical data in TOLL (T_J = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain to Source Voltage		60	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (V_{GS} = 10 V) (Note 1)	T_C = 25°C	441	A
		T_C = 100°C	312	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		1167	mJ
P_D	Power Dissipation $R_{\theta JC}$		429	W
	Derate above 25°C		2.86	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)		43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting T_J = 25°C, L = 0.57 mH, I_{AS} = 64 A
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

ELECTRICAL CHARACTERISTICS in Reference to the FDBL86561−F085 electrical data in TOLL (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		60	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 60 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
			T_J = 175°C (Note 4)	–	–	3	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On−Resistance	I_D = 80 A, V_{GS} = 10 V	T_J = 25°C	–	0.85	1.1	mΩ
			T_J = 175°C (Note 4)	–	1.5	2.2	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		–	13650	–	pF
C_{oss}	Output Capacitance			–	3375	–	pF
C_{rss}	Reverse Transfer Capacitance			–	255	–	pF
R_g	Gate Resistance	f = 1 MHz		–	2.3	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V, V_{DD} = 48 V, I_D = 80 A		–	170	–	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 48 V, I_D = 80 A		–	24	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 48 V, I_D = 80 A		–	56	–	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	24	–	nC
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	45	–	ns
t_r	Rise Time			–	61	–	ns
$t_{d(off)}$	Turn−Off Delay Time			–	80	–	ns
t_f	Fall Time			–	41	–	ns

ELECTRICAL CHARACTERISTICS in Reference to the FDBL86561−F085 electrical data in TOLL (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DRAIN−SOURCE DIODE CHARACTERISTIC						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V	–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V	–	–	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 48 V	–	107	–	ns
Q_{rr}	Reverse Recovery Charge		–	183	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

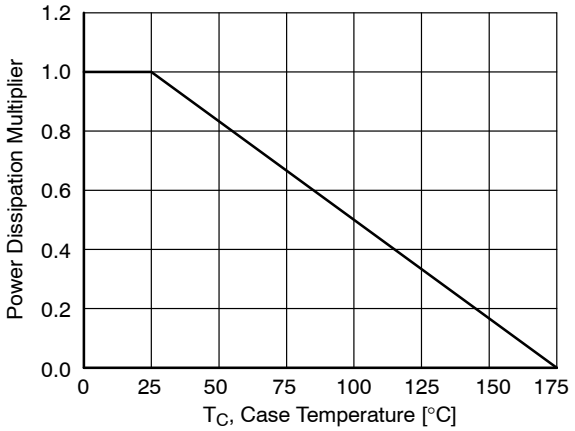


Figure 1. Normalized Power Dissipation vs. Case Temperature

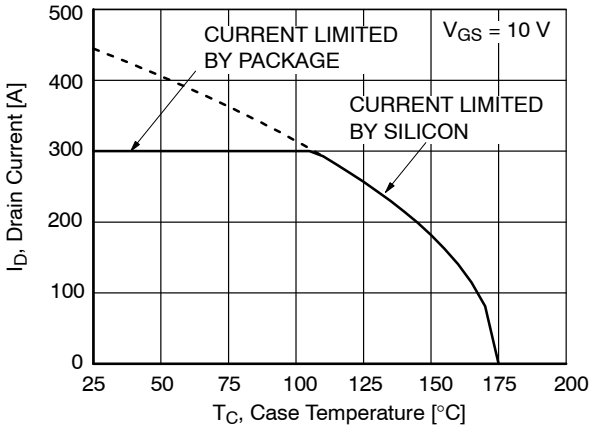


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

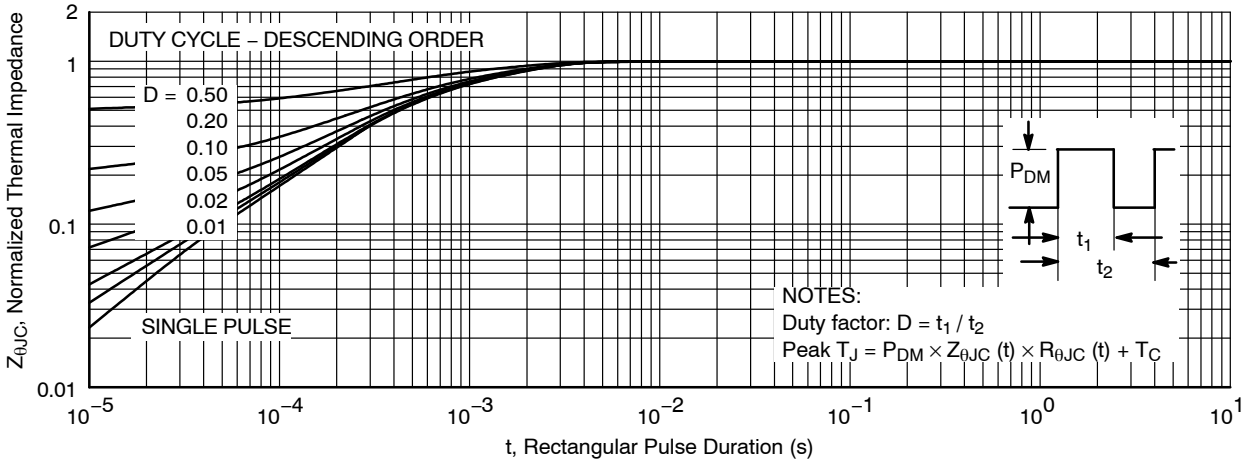


Figure 3. Normalized Maximum Transient Thermal Impedance

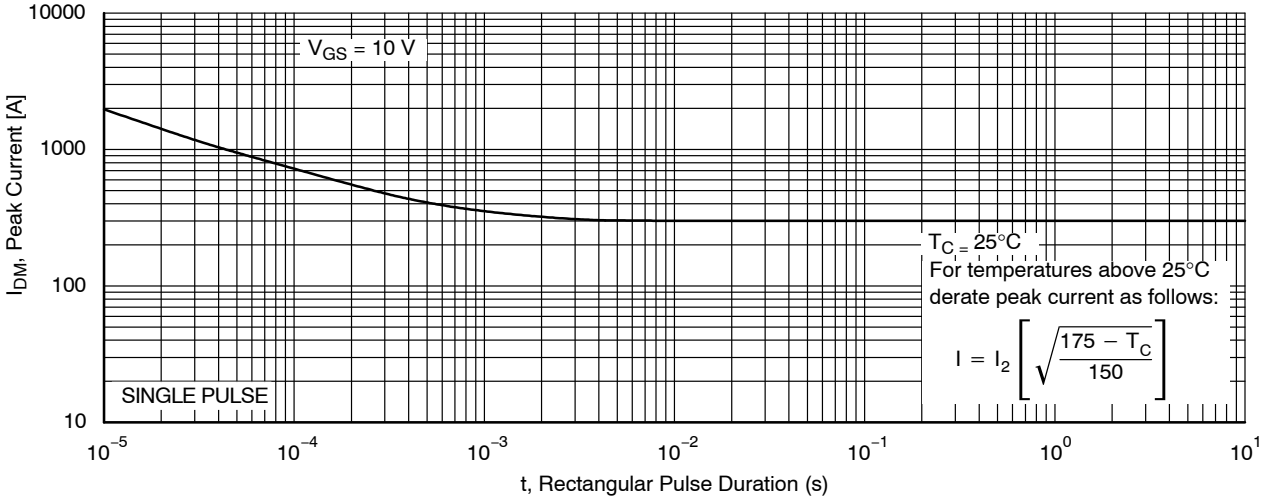


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

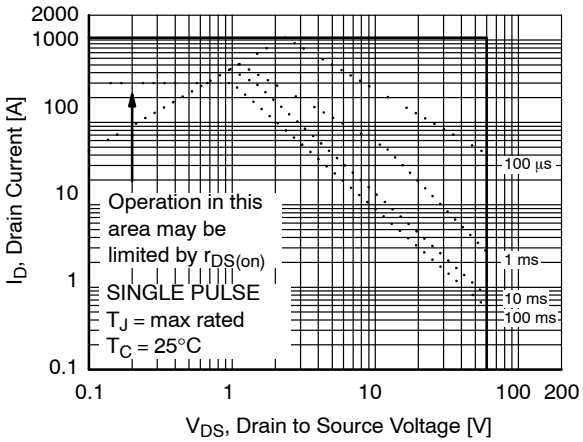
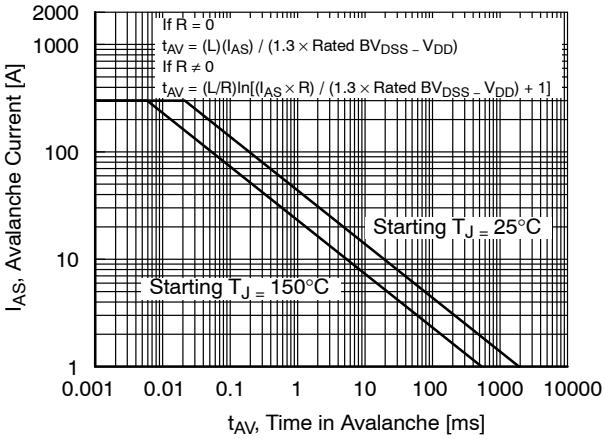


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

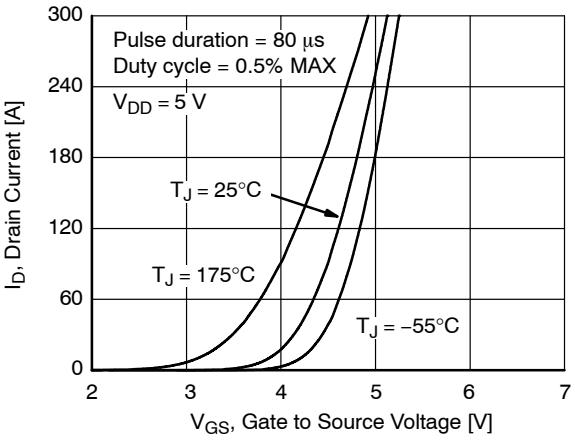


Figure 7. Transfer Characteristics

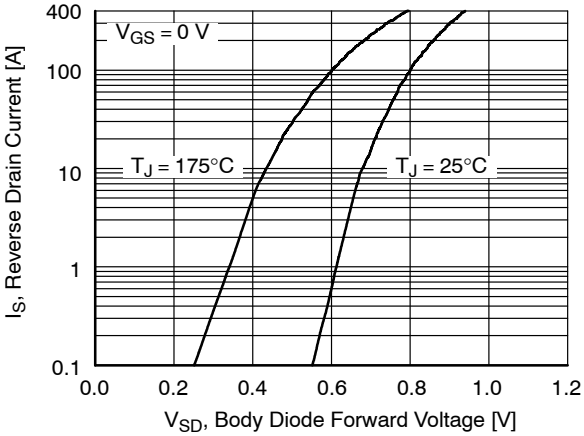


Figure 8. Forward Diode Characteristics

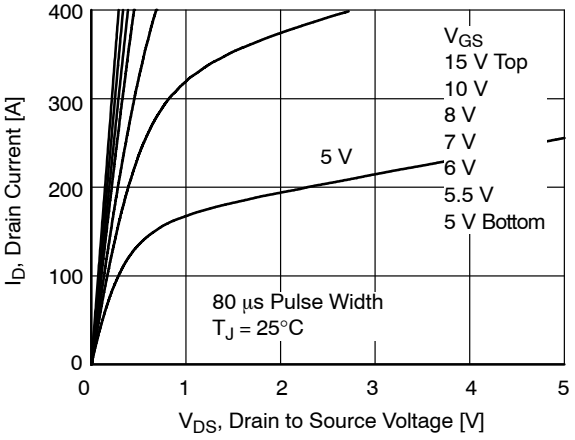


Figure 9. Saturation Characteristics

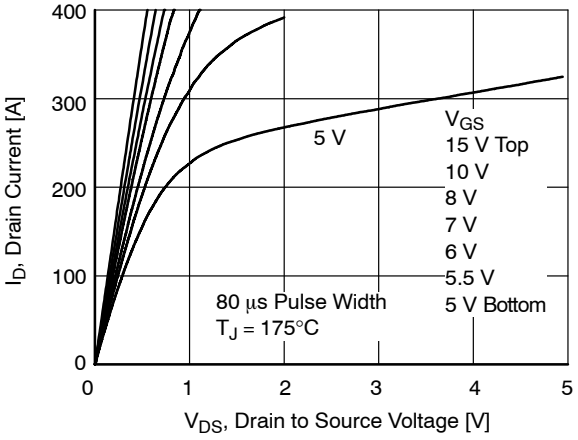


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

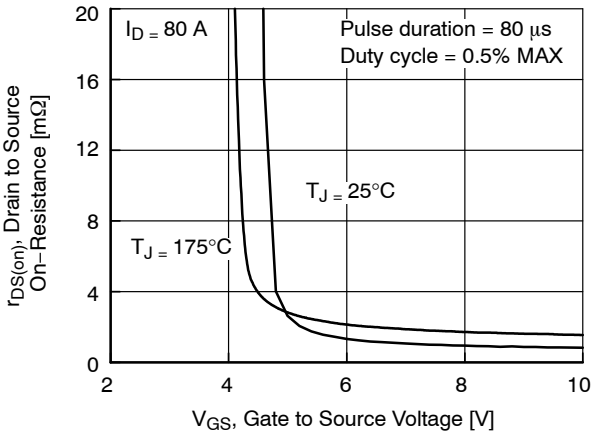


Figure 11. R_{DSON} vs. Gate Voltage

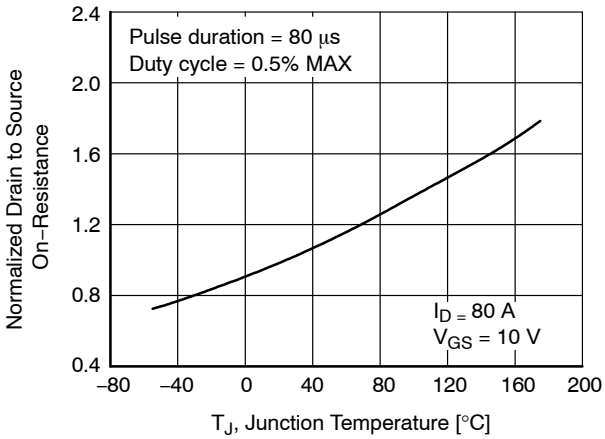


Figure 12. Normalized R_{DSON} vs. Junction Temperature

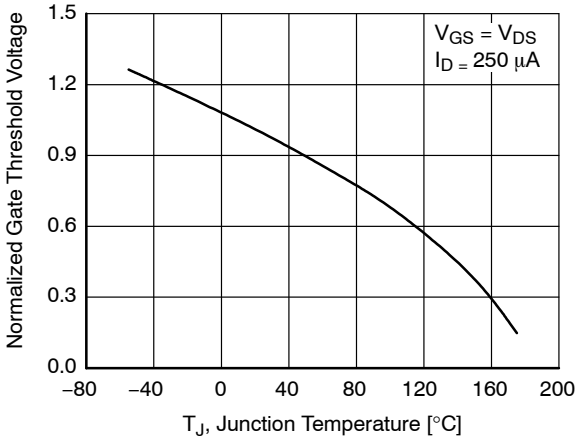


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

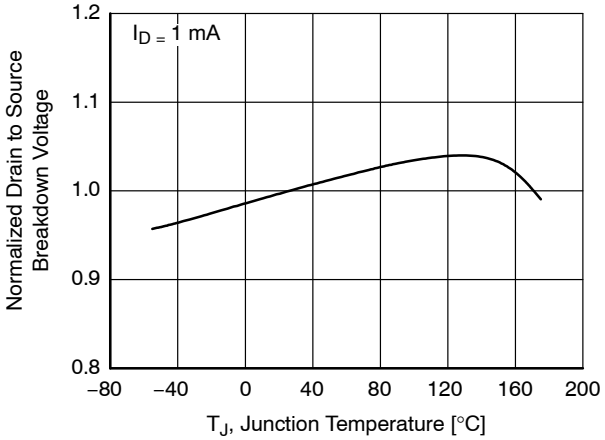


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

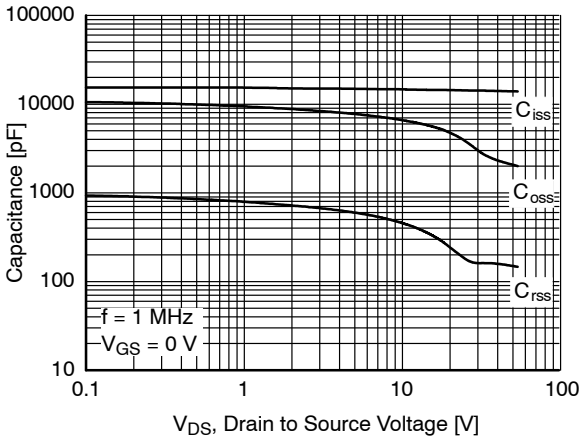


Figure 15. Capacitance vs. Drain to Source Voltage

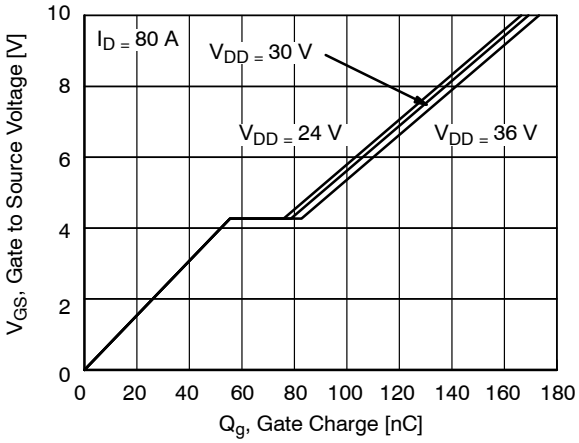


Figure 16. Gate Charge vs. Gate to Source Voltage

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