Intelligent Power Module (IPM), 600 V, 10 A

STK544UC63K-E

The STK544UC63K−E is a fully−integrated inverter power stage consisting of a high−voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless−DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3−phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm. The power stage has a full range of protection functions including cross−conduction protection, external shutdown and under−voltage lockout functions. An internal comparator and reference connected to the over−current protection circuit allows the designer to set the over−current protection level.

Features

- Three−phase 10 A/600 V IGBT Module with Integrated Drivers
- Built−in Under Voltage Protection
- Cross−conduction Protection
- ITRIP Input to Shut Down All IGBTs
- Integrated Bootstrap Diodes and Resistors
- Thermistor for Substrate Temperature Measurement
- UL1557 Certification (File Number: E339285)
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

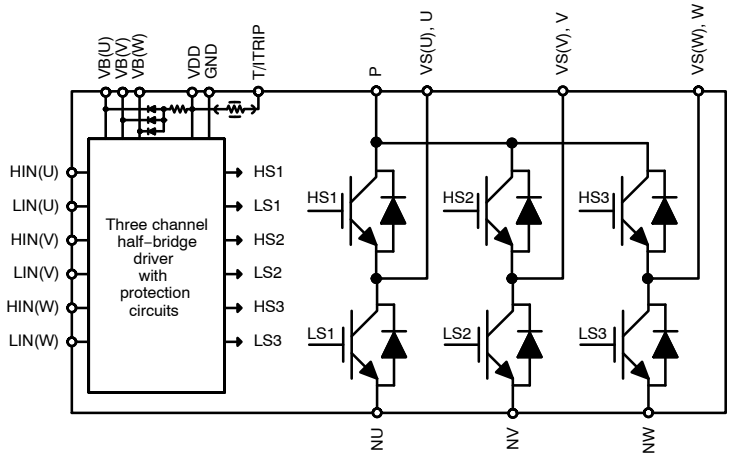
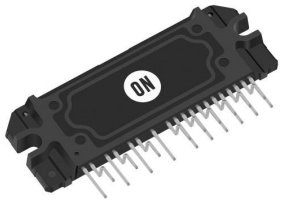


Figure 1. Functional Diagram



SIP23 62x21.8
CASE 127FC

MARKING DIAGRAM

STK544UC63K	= Specific Device Code
ZZZ	= Assembly Lot Code
A	= Assembly Location
T	= Test Location
Y	= Year
WW	= Work Week

Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Qty/Packing)
STK544UC63K−E	SIP23 62x21.8FP−4 (Pb−Free)	80/Box

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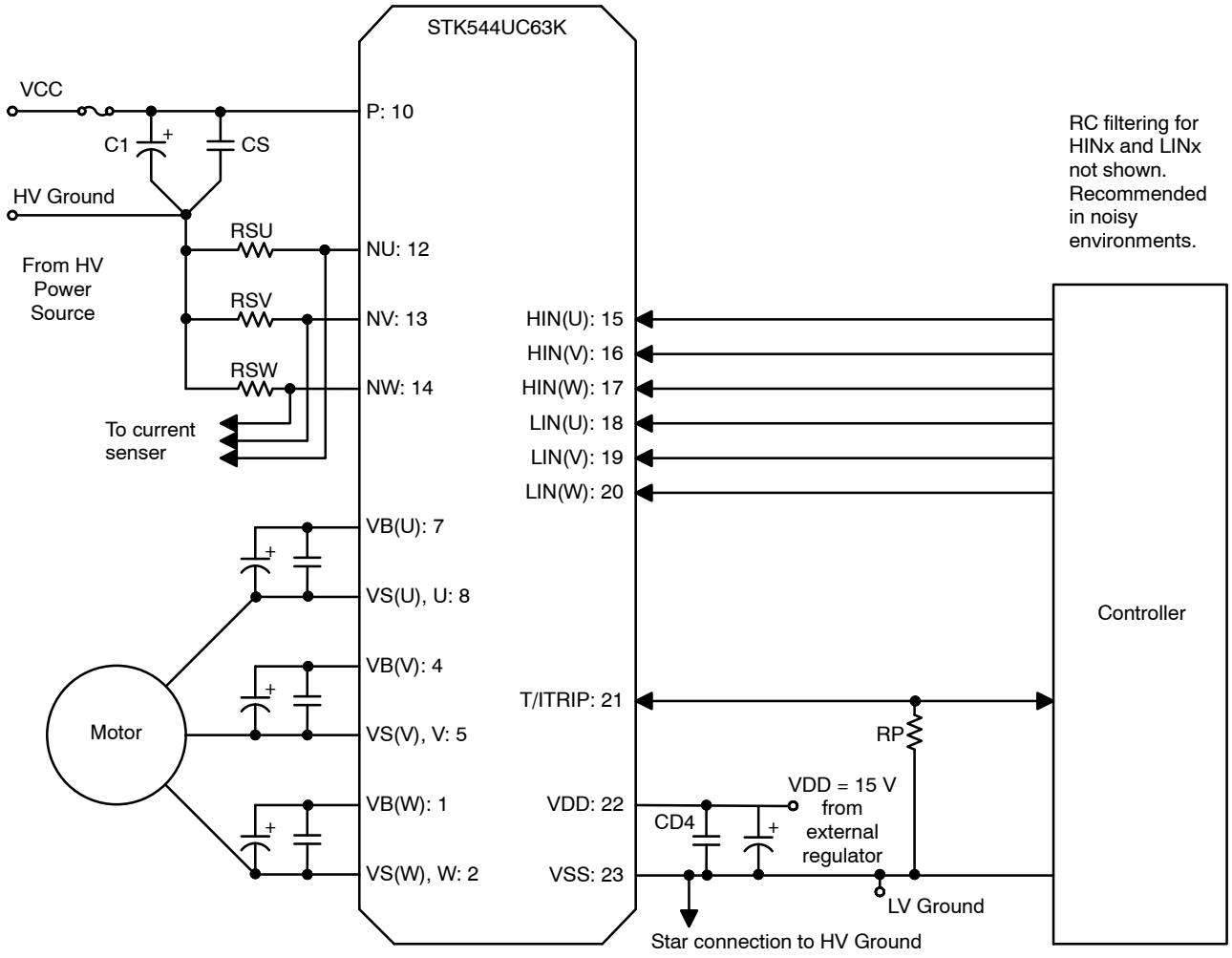


Figure 2. Application Schematic

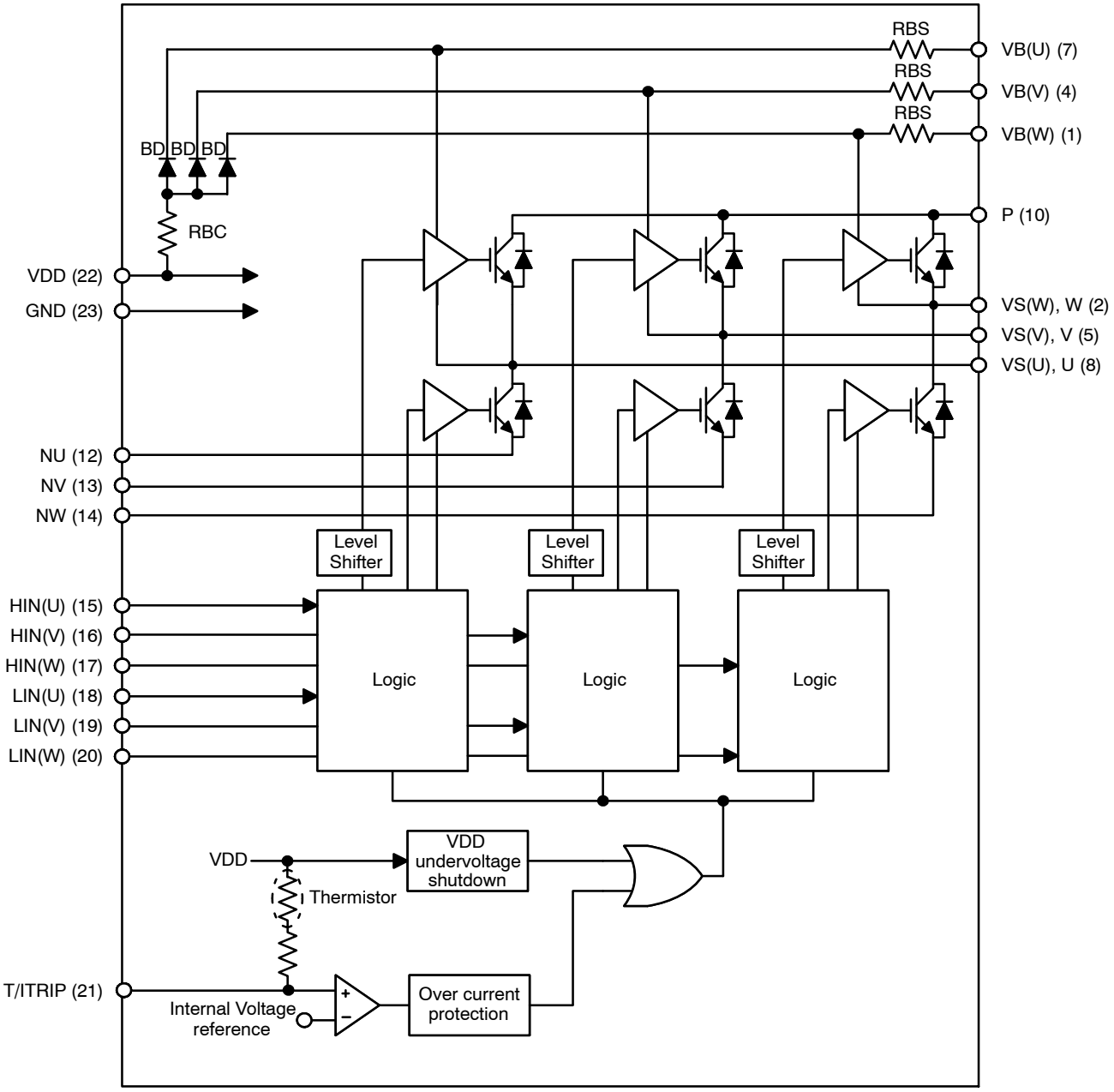


Figure 3. Simplified Block Diagram

PIN DESCRIPTION

Pin No.	Name	Description
1	VB(W)	High Side Floating Supply Voltage for W phase
2	VS(W), W	Internally connected to W phase high side driver ground. W phase output
4	VB(V)	High Side Floating Supply voltage for V phase
5	VS(V), V	Internally connected to V phase high side driver ground. V phase output
7	VB(U)	High Side Floating Supply voltage for U phase
8	VS(U), U	Internally connected to U phase high side driver ground. U phase output
10	P	Positive Bus Input Voltage
12	NU	Low Side Emitter Connection − Phase U
13	NV	Low Side Emitter Connection − Phase V
14	NW	Low Side Emitter Connection − Phase W
15	HIN(U)	Logic Input High Side Gate Driver − Phase U
16	HIN(V)	Logic Input High Side Gate Driver − Phase V
17	HIN(W)	Logic Input High Side Gate Driver − Phase W
18	LIN(U)	Logic Input Low Side Gate Driver − Phase U
19	LIN(V)	Logic Input Low Side Gate Driver − Phase V
20	LIN(W)	Logic Input Low Side Gate Driver − Phase W
21	T/ITRIP	Temperature Monitor and Shut−down pin
22	VDD	+15 V Main Supply
23	VSS	Negative Main Supply

1. Pins 3, 6, 9 and 11 are not present

ABSOLUTE MAXIMUM RATINGS (at Tc = 25°C) (Note 2)

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	P to NU, NV, NW, surge < 500 V (Note 3)	450	V
V_{CE}	Collector−emitter voltage	P to U, V, W; U to NU; V to NV; W to NW	600	V
Io	Output current	P, U, V, W, NU, NV, NW terminal current	±10	A
		P, U, V, W, NU, NV, NW terminal current, Tc = 100°C	±5	A
Iop	Output peak current	P, U, V, W, NU, NV, NW terminal current, pulse width 1 ms	±20	A
Pd	Maximum power dissipation	IGBT per 1 channel	20	W
V_{BS}	Gate driver supply voltage	VB(U) to VS(U), VB(V) to VS(V), VB(W) to VS(W), VDD to VSS (Note 4)	−0.3 to +20.0	V
VIN	Input signal voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)	−0.3 to +7.0	V
VITRIP	ITRIP terminal voltage	T/ITRIP terminal	VSS to +5.0	V
Tj	Junction temperature	IGBT, FRD	150	°C
Tstg	Storage temperature		−40 to +125	°C
Tc	Operating case temperature	IPM case temperature	−40 to +100	°C
MT	Tightening torque	Case mounting screws	0.9	Nm
Vis	Isolation voltage	50 Hz sine wave AC 1 minute (Note 5)	2000	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
4. VBS = VB(U) to VS(U), VB(V) to VS(V), VB(W) to VS(W).
5. Test conditions: AC2500V, 1 s.

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	P to NU, NV, NW	0	280	450	V
VBS	Gate driver supply voltage	VB(U) to VS(U), VB(V) to VS(V), VB(W) to VS(W)	13.0	15	17.5	V
V_{DD}		VDD to VSS	14.0	15	16.5	V
VIN(ON)	ON−state input voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)	0	−	0.3	V
VIN(OFF)	OFF−state input voltage		3.0	−	5.0	V
f_{PWM}	PWM frequency		1	−	20	kHz
DT	Dead time	Turn−off to Turn−on (external)	0.5	−	−	μs
PWIN	Allowable input pulse width	ON and OFF	1	−	−	μs
	Tightening torque	‘M3’ type screw	0.6	−	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_c = 25°C, V_{BIAS} (V_{BS}, V_{DD}) = 15 V unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
POWER OUTPUT SECTION						
I_{CE}	Collector−emitter leakage current	V_{CE} = 600 V	−	−	0.1	mA
IR(BD)	Bootstrap diode reverse current	VR(DB) = 600 V	−	−	0.1	mA
V_{CE}(SAT)	Collector to emitter saturation voltage	IC = 10 A, Tj = 25°C	−	2.1	2.7	V
		IC = 5 A, Tj = 100°C	−	1.7	−	V
VF	Diode forward voltage	IF = 10 A, Tj = 25°C	−	2.2	2.8	V
		IF = 5 A, Tj = 100°C	−	1.7	−	V
VF(BD)	Bootstrap diode forward voltage	IF = 0.1 A	−	2.0	−	V
R_{BC}	Bootstrap circuit resistance	Resistor value for common boot charge line	−	2	−	Ω
R_{BS}		Resistor value for separate boot charge line	−	10	−	Ω
θj−c(T)	Junction to case thermal resistance	IGBT	−	4.9	6.2	°C/W
θ−c(D)		FRD	−	8.5	10.6	°C/W
DRIVER SECTION						
ID	Gate driver consumption current	V_{BS} = 15 V (Note 6), per driver	−	0.08	0.4	mA
ID		V_{DD} = 15 V, total	−	2.0	4.0	mA
VIN H	High level Input voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) to VSS	2.5	−	−	V
VIN L	Low level Input voltage		−	−	0.8	V
I_{IN+}	Logic 0 input leakage current		76	118	160	μA
$I_{IN−}$	Logic 1 input leakage current		97	150	203	μA
V_{ITRIP}	ITRIP threshold voltage	T/ITRIP to VSS	3.67	4.17	4.67	V
t_{ITRIP}	ITRIP to shutdown propagation delay		0.8	1.1	1.4	μs
$t_{ITRIPBL}$	ITRIP blanking time		−	0.9	−	μs
FLTCLR	FAULT clearance delay time	Automatic reset after protection	6	9	12	ms
DT	Dead time (Internal dead time injected by driver)		220	300	380	μs
V_{CCUV+} V_{BSUV+}	V_{DD} and V_{BS} supply undervoltage positive going input threshold		10.5	11.1	11.7	V

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{BIAS} (V_{BS}, V_{DD}) = 15 V unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CCUV-} V_{BSUV-}	V_{DD} and V_{BS} supply undervoltage negative going input threshold		10.3	10.9	11.5	V
V_{CCUVH} V_{BSUVH}	V_{DD} and V_{BS} supply undervoltage lockout hysteresis		0.14	0.2	–	V

SWITCHING CHARACTER

t_{ON}	Switching time	IC = 10 A, Tj = 25°C	–	0.35	0.7	μs
t_{OFF}			–	0.45	0.8	μs
E_{ON}	Turn−on switching loss	IC = 5 A, Tj = 25°C	–	89	–	μJ
E_{OFF}	Turn−off switching loss		–	74	–	μJ
E_{TOT}	Total switching loss		–	163	–	μJ
E_{ON}	Turn−on switching loss	IC = 5 A, Tj = 100°C	–	125	–	μJ
E_{OFF}	Turn−off switching loss		–	82	–	μJ
E_{TOT}	Total switching loss		–	207	–	μJ
E_{REC}	Diode reverse recovery energy	IC = 5 A, Tj = 100°C	–	40	–	μJ
t_{RR}	Diode reverse recovery time		–	150	–	ns
RBSOA	Reverse bias safe operating area	IC = 20 A, V_{CE} = 450 V	Full Square			
SCSOA	Short circuit safe operating area	V_{CE} = 400 V, Tj = 150°C	5	–	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. VBS = VBU to U, VBV to V, VBW to W

TYPICAL CHARACTERISTICS INV SECTION

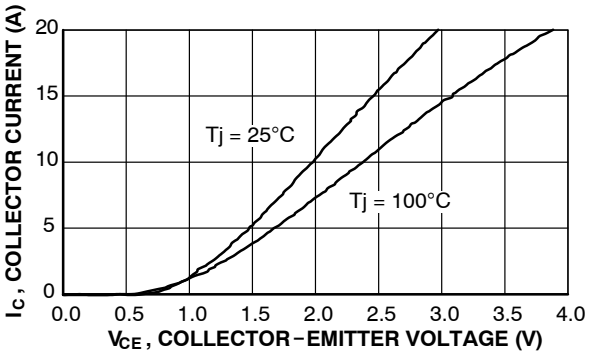


Figure 4. V_{CE} versus I_C for Different Temperatures (V_{DD} = 15 V)

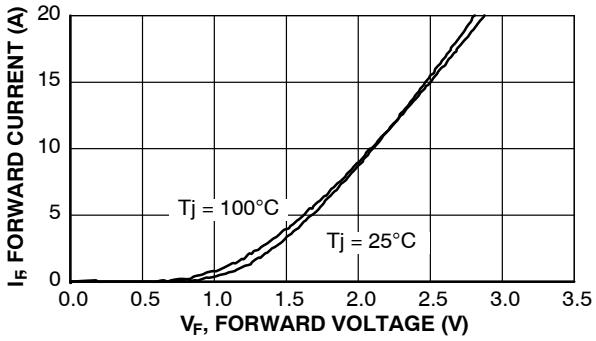


Figure 5. V_F versus I_F for Different Temperatures

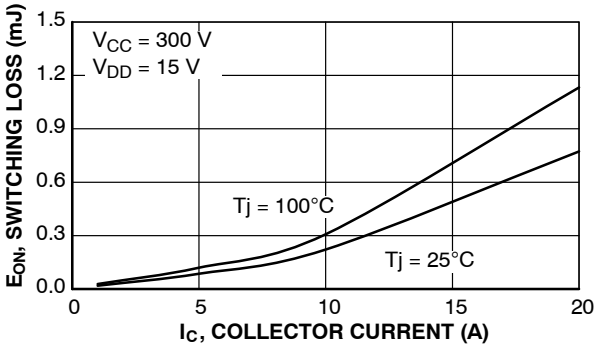


Figure 6. E_{ON} versus I_C for Different Temperatures

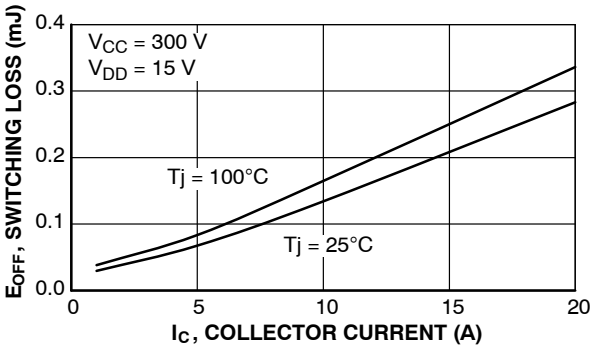


Figure 7. E_{OFF} versus I_C for Different Temperatures

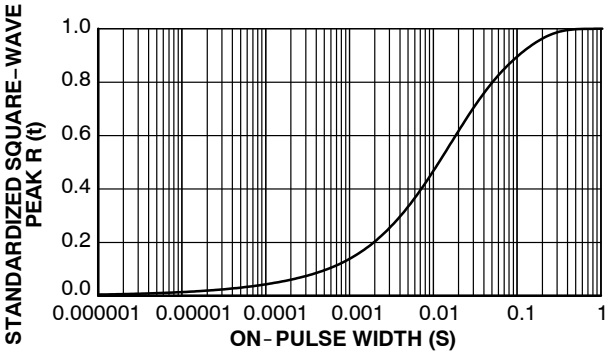


Figure 8. Thermal Impedance Plot

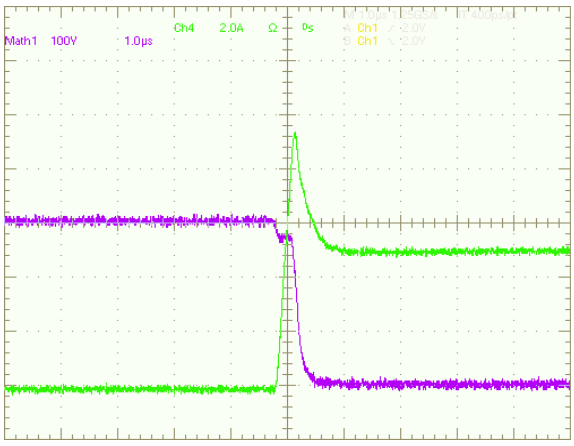


Figure 9. Turn−on Waveform Tj = 100°C, V_{CC} = 300 V

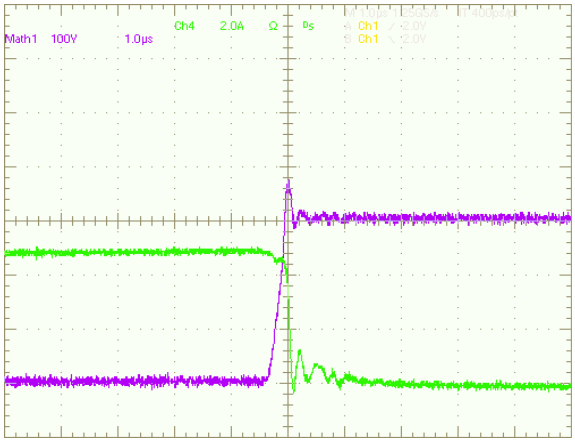


Figure 10. Turn−off Waveform Tj = 100°C, V_{CC} = 300 V

APPLICATIONS INFORMATION

Input/Output Timing Chart

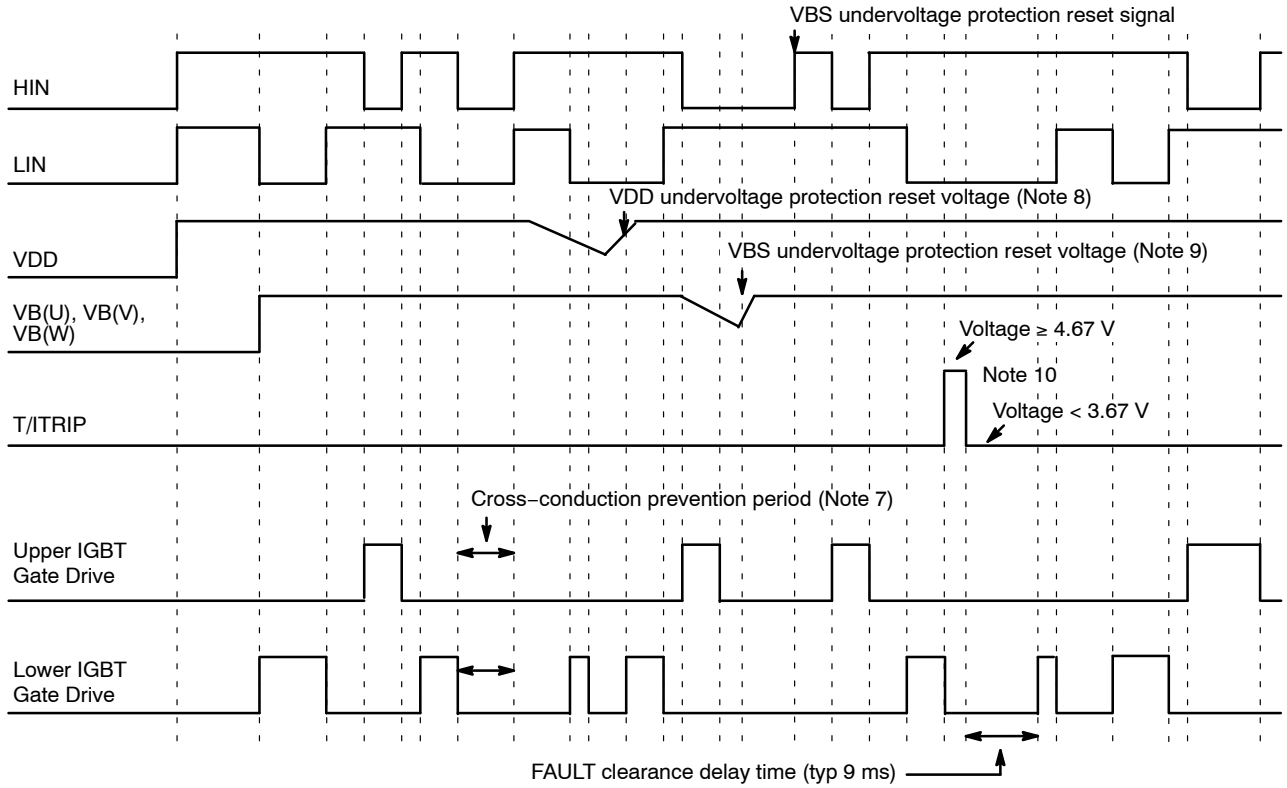


Figure 11. Input/Output Timing Chart

NOTES:

7. This section of the timing diagram shows the effect of cross−conduction prevention.
8. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
9. This section shows that when the bootstrap voltage on VB(U) (VB(V), VB(W)) drops, the corresponding high side output U (V, W) is switched off. When the voltage on VB(U) (VB(V), VB(W)) rises sufficiently, normal operation will resume.
10. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over−current condition is removed.

Input/Output Logic Table

Table 1. INPUT/OUTPUT LOGIC TABLE

INPUT			OUTPUT		
HIN	**LIN**	**T/ITRIP**	**High Side IGBT**	**Low Side IGBT**	**U, V, W**
L	H	L	ON	OFF	P
H	L	L	OFF	ON	NU, NV, NW
H	H	L	OFF	OFF	High Impedance
L	L	L	OFF	OFF	High Impedance
X	X	H	OFF	OFF	High Impedance

Thermistor Characteristics

Table 2. THERMISTOR CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{25}	Resistance	Tth = 25°C	99	100	101	kΩ
R_{125}		Tth = 125°C	2.40	2.52	2.65	kΩ
B	B−Constant (25 to 50°C)		−4207	4250	4293	K
	Temperature Range		−40	−	+125	°C

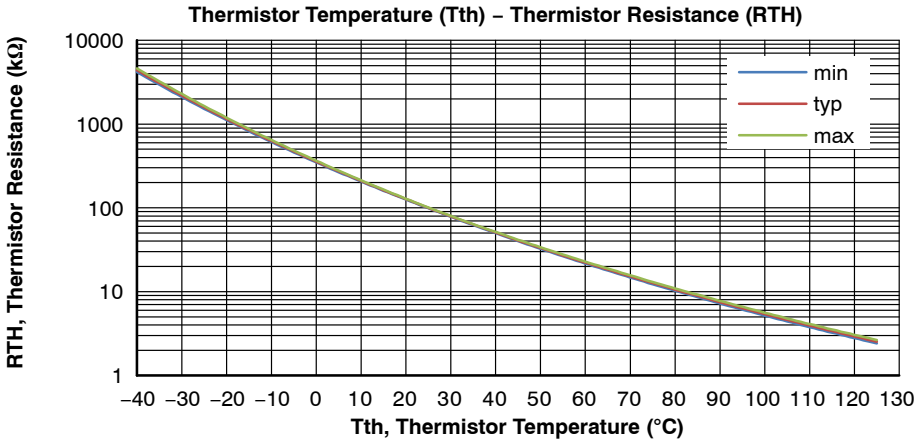


Figure 12. Thermistor Resistance versus Thermistor Temperature

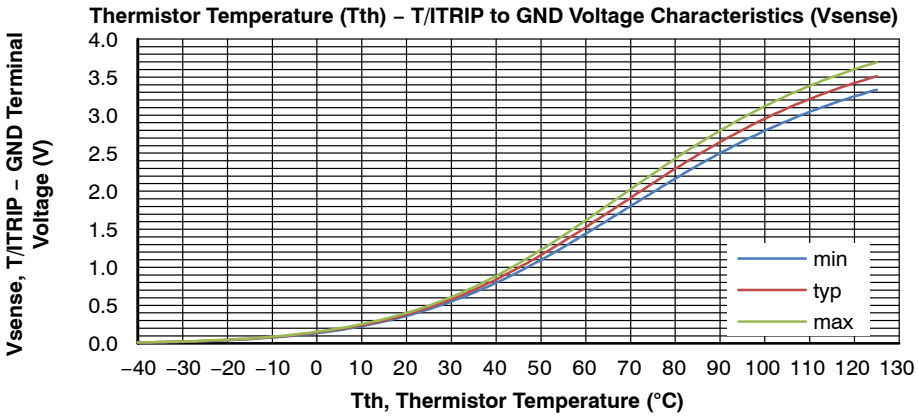


Figure 13. Thermistor Voltage versus Thermistor Temperature
Conditions: RP = 4.3 kΩ 1% Pull−down and VDD = 15.0 V (See below)

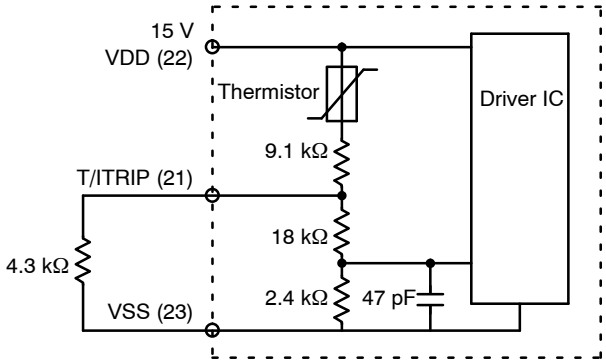


Figure 14. Sample Application Circuit for Temperature Monitoring

TEST CIRCUITS

- $I_{CE, IR(DB)}$

	U+	V+	W+	U−	V−	W−
A	10	10	10	8	5	2
B	8	5	2	12	13	14

U+,V+,W+: High side phase
U−,V−,W−: Low side phase

	U(DB)	V(DB)	W(DB)
A	7	4	1
B	23	23	23

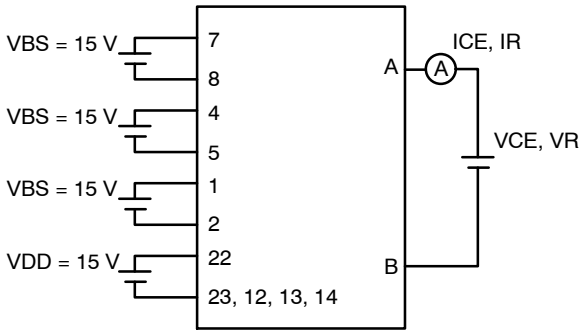


Figure 15. Test Circuit for I_{CE}

- V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U−	V−	W−
A	10	10	10	8	5	2
B	8	5	2	12	13	14
C	15	16	17	18	19	20

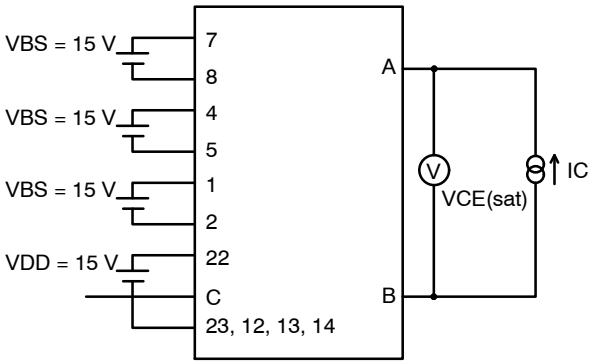


Figure 16. Test Circuit for $V_{CE(SAT)}$

- VF (Test by pulse)

	U+	V+	W+	U−	V−	W−
A	10	10	10	8	5	2
B	8	5	2	12	13	14

	U(DB)	V(DB)	W(DB)
A	7	4	1
B	22	22	22

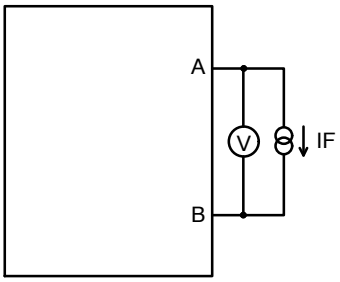


Figure 17. Test Circuit for V_F

- ID

	VBS U+	VBS V+	VBS W+	V_{DD}
A	7	4	1	22
B	8	5	2	23

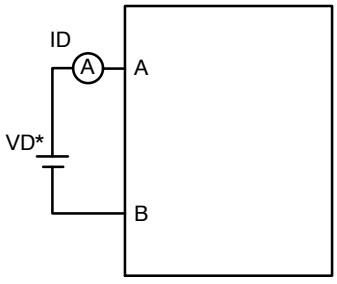
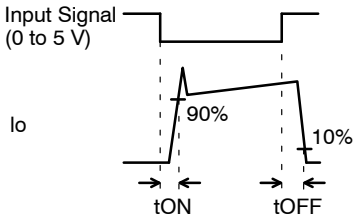


Figure 18. Test Circuit for I_D

- Switching time (The circuit is a representative example of the lower side U phase.)

	U+	V+	W+	U−	V−	W−
A	10	10	10	10	10	10
B	12	13	14	12	13	14
C	8	5	2	10	10	10
D	12	13	14	8	5	2
E	15	16	17	18	19	20



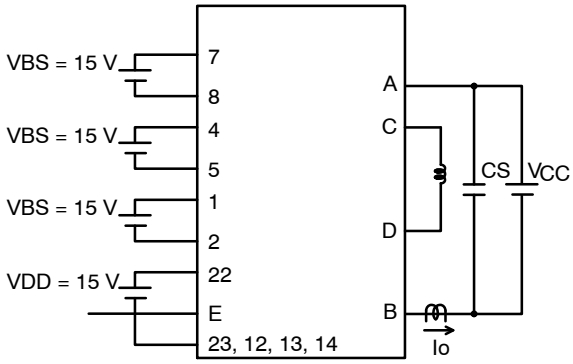


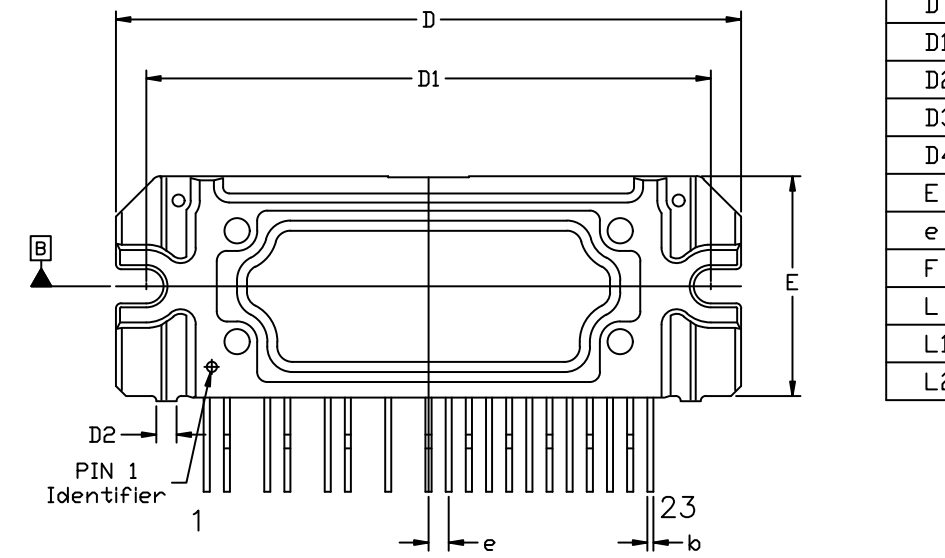
Figure 19. Test Circuit for Switching Time

SIP23, 62x21.8 FP−4
CASE 127FC
ISSUE O

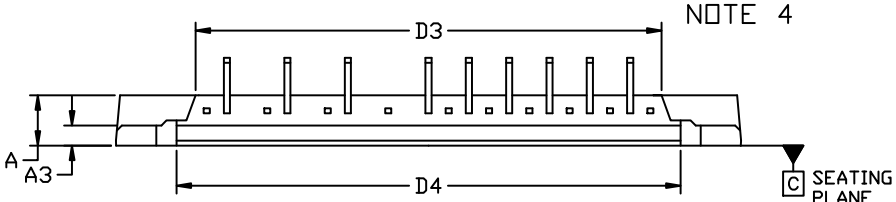
DATE 07 JAN 2019

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. PIN 1 IDENTIFICATION IS A MIRRORED SURFACE INDENT.
6. MISSING PINS ARE 3,6,9 and 11.

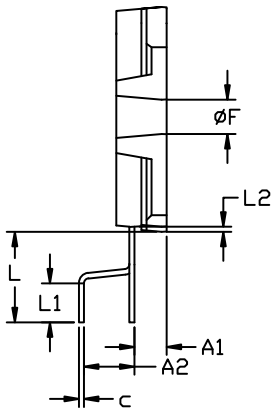
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.5	5.0	5.5
A1	2.7	3.2	3.7
A2	4.5	5.0	5.5
A3	1.5	2.0	2.5
b	0.55	0.6	0.8
c	0.45	0.5	0.7
D	61.5	62.0	62.5
D1	55.5	56.0	56.5
D2	1.5	2.0	2.5
D3	45.7	46.2	46.7
D4	49.5	50.0	50.5
E	21.3	21.8	22.3
e	2.0 REF		
F	2.9	3.4	3.9
L	8.5	9.0	9.5
L1	3.8	4.3	4.8
L2	0.0	0.5	1.0



TOP VIEW



SIDE VIEW



END VIEW

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SIP23, 62x21.8 FP−4**	**PAGE 1 OF 1**

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