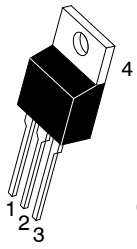
Complementary Silicon Plastic Power Transistors

TIP29, A, B, C (NPN), TIP30, A, B, C (PNP)

Designed for use in general purpose amplifier and switching applications. Compact TO−220 package.



TO−220
CASE 221A
STYLE 1

Features

- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CEO}	Collector − Emitter Voltage TIP29G, TIP30G TIP29AG, TIP30AG TIP29BG, TIP30BG TIP29CG, TIP30CG	 40 60 80 100	Vdc
V_{CB}	Collector − Base Voltage TIP29G, TIP30G TIP29AG, TIP30AG TIP29BG, TIP30BG TIP29CG, TIP30CG	 40 60 80 100	Vdc
V_{EB}	Emitter − Base Voltage	5.0	Vdc
I_C	Collector Current − Continuous	1.0	Adc
I_{CM}	Collector Current − Peak	3.0	Adc
I_B	Base Current	0.4	Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	 30 0.24	 W W/°C
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C	 2.0 0.016	 W W/°C
E	Unclamped Inductive Load Energy (Note 1)	32	mJ
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

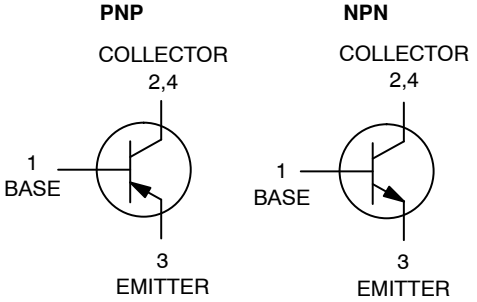
1. This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F = 10 Hz

THERMAL CHARACTERISTICS

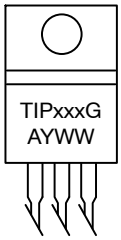
Symbol	Characteristic	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	62.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	4.167	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

1 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 40, 60, 80, 100 VOLTS, 80 WATTS



MARKING DIAGRAM



TIPxxx	=	Device Code: 29, 29A, 29B, 29C 30, 30A, 30B, 30C
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
OFF CHARACTERISTICS				
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0) (Note 2) TIP29G, TIP30G TIP29AG, TIP30AG TIP29BG, TIP30BG TIP29CG, TIP30CG	 40 60 80 100	 – – – –	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) TIP29G, TIP29AG, TIP30G, TIP30AG (V_{CE} = 60 Vdc, I_B = 0) TIP29BG, TIP29CG, TIP30BG, TIP30CG	 – –	 0.3 0.3	mAdc
I_{CES}	Collector Cutoff Current (V_{CE} = 40 Vdc, V_{EB} = 0) TIP29G, TIP30G (V_{CE} = 60 Vdc, V_{EB} = 0) TIP29AG, TIP30AG (V_{CE} = 80 Vdc, V_{EB} = 0) TIP29BG, TIP30BG (V_{CE} = 100 Vdc, V_{EB} = 0) TIP29CG, TIP30CG	 – – – –	 200 200 200 200	μAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	 –	 1.0	mAdc
ON CHARACTERISTICS (Note 2)				
h_{FE}	DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	 40 15	 – 75	–
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)	 –	 0.7	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	 –	 1.3	Vdc
DYNAMIC CHARACTERISTICS				
f_T	Current−Gain − Bandwidth Product (Note 3) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	 3.0	 –	MHz
h_{fe}	Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	 20	 –	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
3. $f_T = |h_{fe}| \bullet f_{test}$

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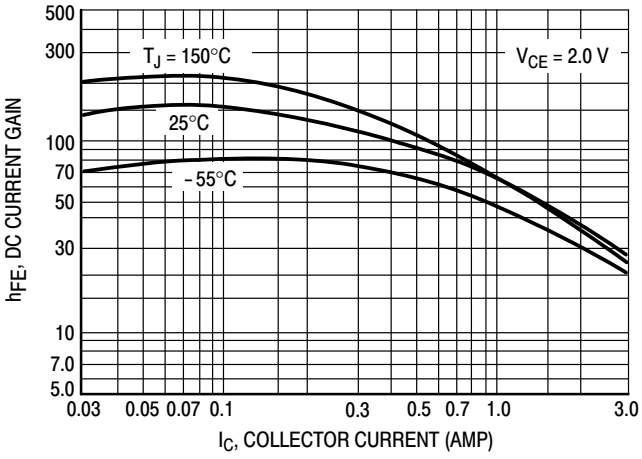

Figure 1. DC Current Gain

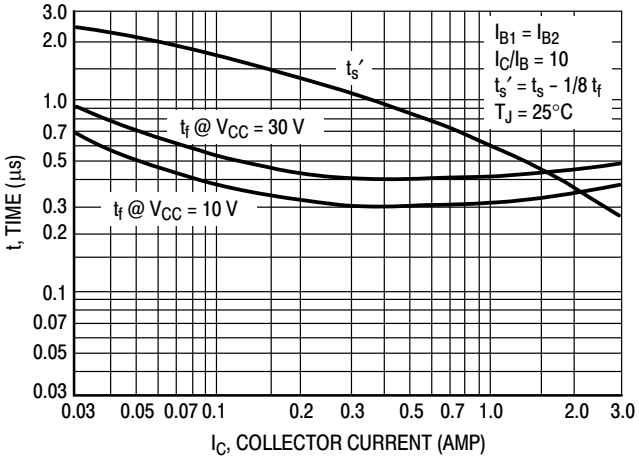

Figure 2. Turn−Off Time

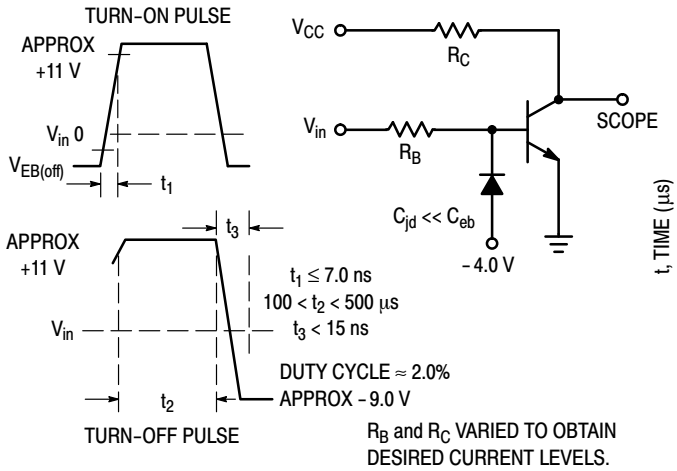

Figure 3. Switching Time Equivalent Circuit

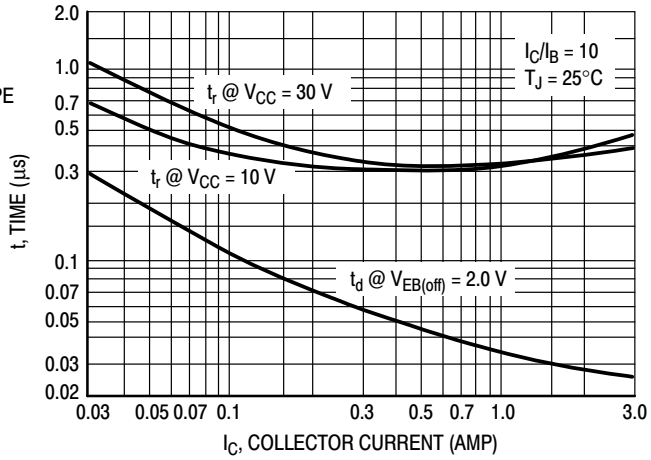

Figure 4. Turn−On Time

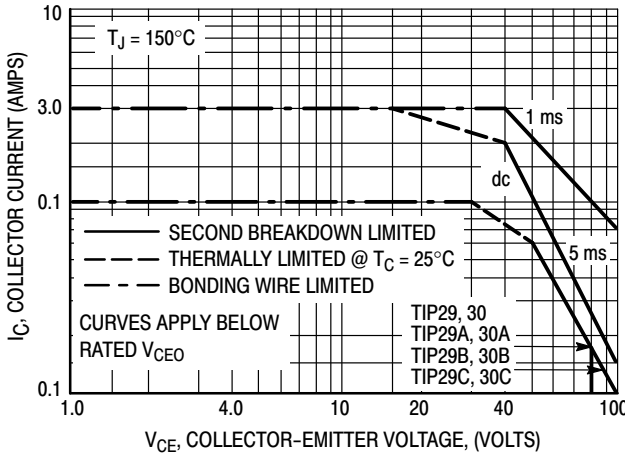

Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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ORDERING INFORMATION

Device	Package	Shipping
TIP29G	TO−220 (Pb−Free)	50 Units / Rail
TIP29AG	TO−220 (Pb−Free)	50 Units / Rail
TIP29BG	TO−220 (Pb−Free)	50 Units / Rail
TIP29CG	TO−220 (Pb−Free)	50 Units / Rail
TIP30G	TO−220 (Pb−Free)	50 Units / Rail
TIP30AG	TO−220 (Pb−Free)	50 Units / Rail
TIP30BG	TO−220 (Pb−Free)	50 Units / Rail
TIP30CG	TO−220 (Pb−Free)	50 Units / Rail

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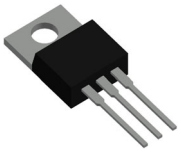
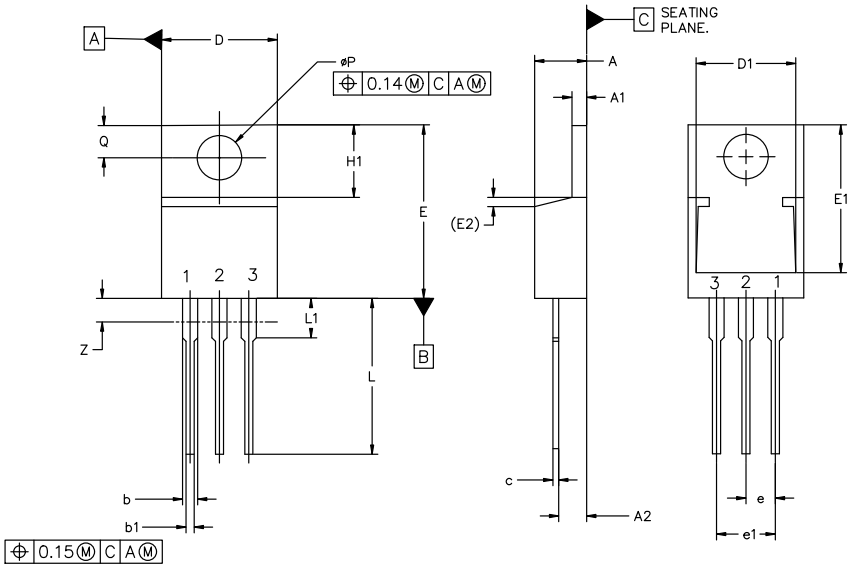


TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	−.−−	−.−−	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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