

# Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO247-3, 650 V, 42 mohm

## UF3C065040K3S

### Description

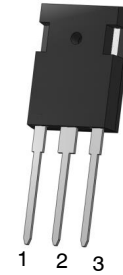
onsemi's cascode products co-package its high-performance G3 SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.

### Features

- Typical On-resistance  $R_{DS(on),typ}$  of 42 m $\Omega$
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected, HBM Class 2
- Very Low Switching Losses (required RC-snubber loss negligible under typical operating conditions)
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

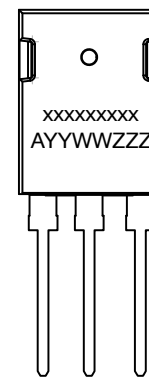
### Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



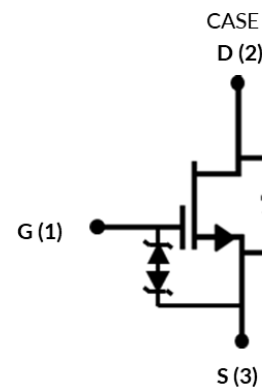
TO247-3  
CASE 340AK

### MARKING DIAGRAM



xxxxxxx = Specific Device Number  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

# UF3C065040K3S

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	$V_{DS}$		650	V
Gate-source Voltage	$V_{GS}$	DC	-25 to +25	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25\text{ }^{\circ}\text{C}$	54	A
		$T_C = 100\text{ }^{\circ}\text{C}$	40	A
Pulsed Drain Current (Note 2)	$I_{DM}$	$T_C = 25\text{ }^{\circ}\text{C}$	125	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	$L = 15\text{ mH}$ , $I_{AS} = 3.19\text{ A}$	76	mJ
Power Dissipation	$P_{tot}$	$T_C = 25\text{ }^{\circ}\text{C}$	326	W
Maximum Junction Temperature	$T_{J,max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	$T_J$ , $T_{STG}$		-55 to 175	$^{\circ}\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	$T_L$		250	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by  $T_{J,max}$
2. Pulse width  $t_p$  limited by  $T_{J,max}$
3. Starting  $T_J = 25\text{ }^{\circ}\text{C}$

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.35	0.46	$^{\circ}\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	$BV_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650	-	-	V
Total Drain Leakage Current	$I_{DSS}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	0.7	150	$\mu\text{A}$
		$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	10	-	
Total Gate Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$ , $V_{GS} = -20\text{ V}/+20\text{ V}$	-	6	$\pm 20$	$\mu\text{A}$
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12\text{ V}$ , $I_D = 40\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	42	52	$\text{m}\Omega$
		$T_J = 125\text{ }^{\circ}\text{C}$	-	59	-	
		$T_J = 175\text{ }^{\circ}\text{C}$	-	78	-	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$	4	5	6	V
Gate Resistance	$R_G$	$f = 1\text{ MHz}$ , open drain	-	4.5	-	$\Omega$

### TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 4)	$I_S$	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	54	A
Diode Pulse Current (Note 5)	$I_{S,pulse}$	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	125	A
Forward Voltage	$V_{FSD}$	$V_{GS} = 0\text{ V}$ , $I_F = 20\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	1.5	1.75	V
		$V_{GS} = 0\text{ V}$ , $I_S = 20\text{ A}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	1.8	-	
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 400\text{ V}$ , $I_F = 40\text{ A}$ , $V_{GS} = -5\text{ V}$ , $R_{G,EXT} = 20\text{ }\Omega$ , $di/dt = 1100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	138	-	nC
Reverse Recovery Time	$t_{rr}$		-	38	-	ns
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 400\text{ V}$ , $I_F = 40\text{ A}$ , $V_{GS} = -5\text{ V}$ , $R_{G,EXT} = 20\text{ }\Omega$ , $di/dt = 1100\text{ A}/\mu\text{s}$ , $T_J = 150\text{ }^{\circ}\text{C}$	-	137	-	nC
Reverse Recovery Time	$t_{rr}$		-	38	-	ns

# UF3C065040K3S

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>TYPICAL PERFORMANCE – DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 100 kHz	–	1500	–	pF
Output Capacitance	C <sub>oss</sub>		–	200	–	
Reverse Transfer Capacitance	C <sub>rss</sub>		–	2.2	–	
Effective Output Capacitance, Energy Related	C <sub>oss(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	146	–	pF
Effective Output Capacitance, Time Related	C <sub>oss(tr)</sub>		–	325	–	pF
C <sub>oss</sub> Stored Energy	E <sub>oss</sub>	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V	–	11.7	–	μJ
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 40 A, V <sub>GS</sub> = –5 V to 15 V	–	51	–	nC
Gate-drain Charge	Q <sub>GD</sub>		–	11	–	
Gate-source Charge	Q <sub>GS</sub>		–	19	–	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 40 A, Gate Driver = –5 V to +15 V, Turn-on R <sub>G,EXT</sub> = 1.8 Ω, Turn-off R <sub>G,EXT</sub> = 22 Ω, Inductive Load, FWD: Same Device With V <sub>GS</sub> = –5 V, R <sub>G</sub> = 22 Ω, RC Snubber: R <sub>S</sub> = 5 Ω, C <sub>S</sub> = 150 pF, T <sub>J</sub> = 25 °C	–	35	–	ns
Rise Time	t <sub>r</sub>		–	24	–	
Turn-off Delay Time	t <sub>d(off)</sub>		–	57	–	
Fall Time	t <sub>f</sub>		–	14	–	
Turn-on Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>ON</sub>		–	500	–	μJ
Turn-off Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>OFF</sub>		–	118	–	
Total Switching Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>TOTAL</sub>		–	618	–	
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>		–	1.7	–	
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>		–	4.5	–	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 40 A, Gate Driver = –5 V to +15 V, Turn-on R <sub>G,EXT</sub> = 1.8 Ω, Turn-off R <sub>G,EXT</sub> = 22 Ω, Inductive Load, FWD: Same Device With V <sub>GS</sub> = –5 V, R <sub>G</sub> = 22 Ω, RC Snubber: R <sub>S</sub> = 5 Ω, C <sub>S</sub> = 150 pF, T <sub>J</sub> = 150 °C	–	35	–	ns
Rise Time	t <sub>r</sub>		–	22	–	
Turn-off Delay Time	t <sub>d(off)</sub>		–	60	–	
Fall Time	t <sub>f</sub>		–	13	–	
Turn-on Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>ON</sub>		–	479	–	μJ
Turn-off Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>OFF</sub>		–	124	–	
Total Switching Energy Including R <sub>S</sub> Energy (Note 6)	E <sub>TOTAL</sub>		–	603	–	
Snubber R <sub>S</sub> Energy During Turn-on	E <sub>RS_ON</sub>		–	1.8	–	
Snubber R <sub>S</sub> Energy During Turn-off	E <sub>RS_OFF</sub>		–	5.3	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Limited by T<sub>J,max</sub>

5. Pulse width t<sub>p</sub> limited by T<sub>J,max</sub>

6. The switching performance are evaluated with a RC snubber circuit as shown in Figure 29.

TYPICAL PERFORMANCE DIAGRAMS

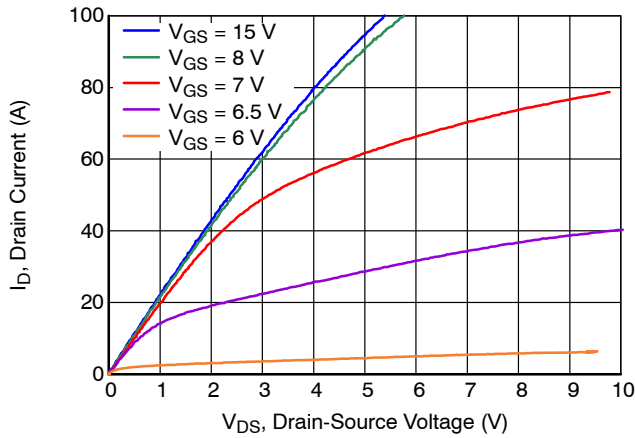


Figure 1. Typical Output Characteristics at  $T_J = -55^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

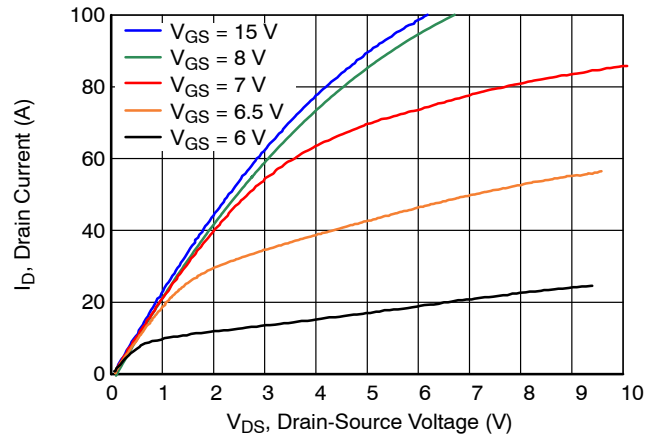


Figure 2. Typical Output Characteristics at  $T_J = 25^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

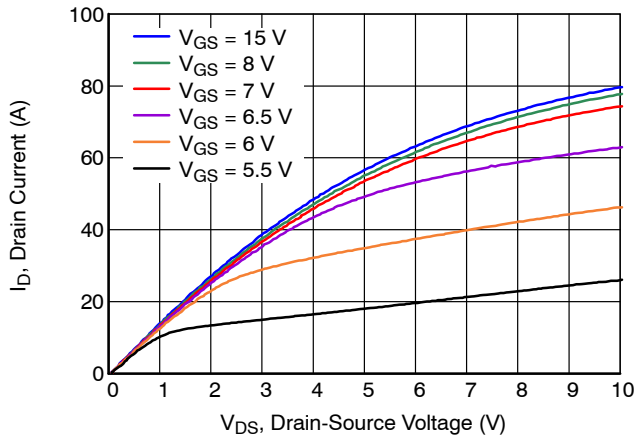


Figure 3. Typical Output Characteristics at  $T_J = 175^\circ\text{C}$ ,  $t_p < 250\ \mu\text{s}$

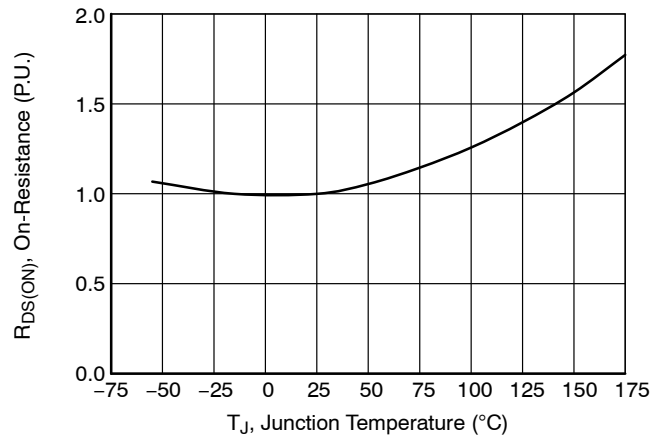


Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\ \text{V}$  and  $I_D = 40\ \text{A}$

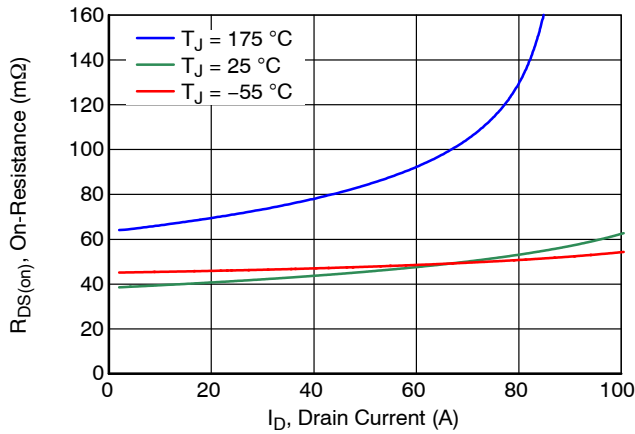


Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\ \text{V}$

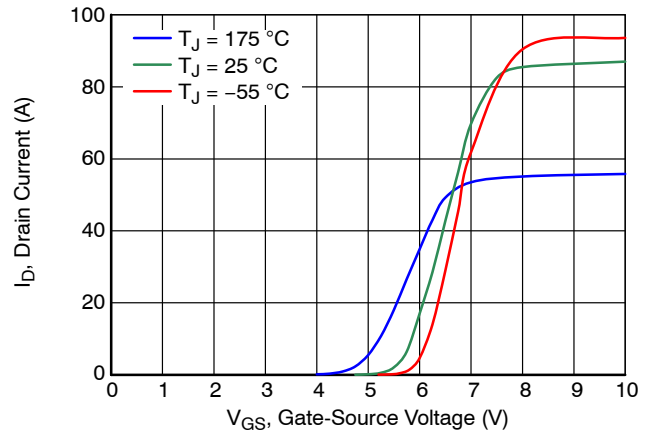
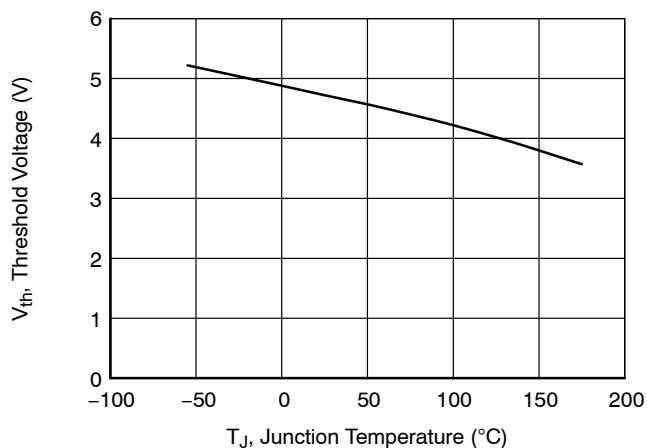
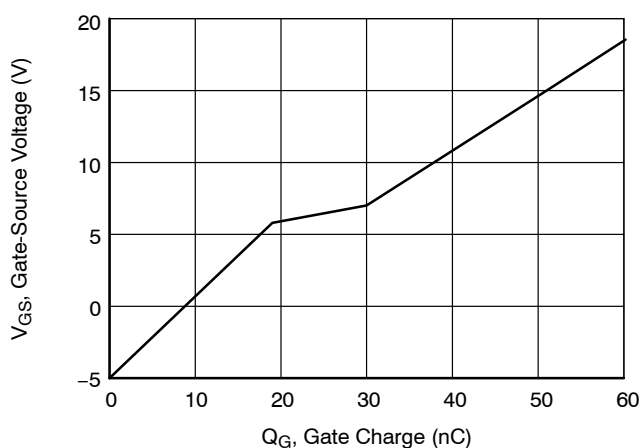


Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\ \text{V}$

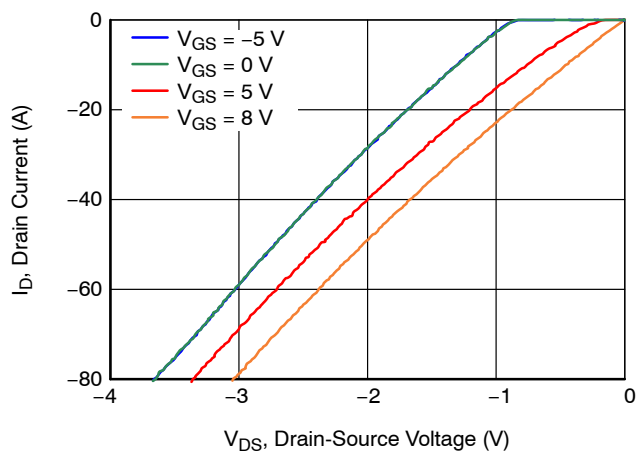
TYPICAL PERFORMANCE DIAGRAMS (continued)



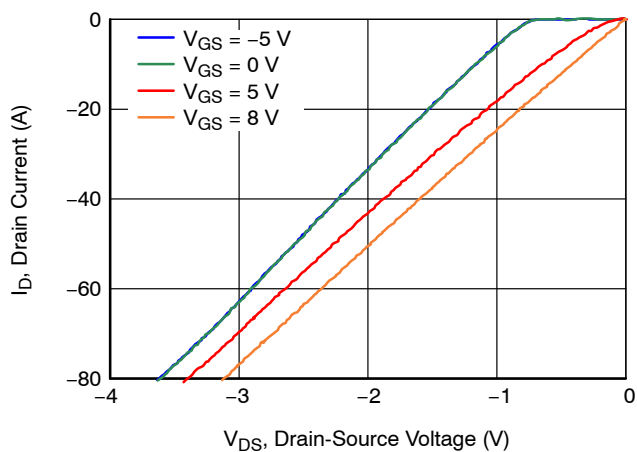
**Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 10\text{ mA}$**



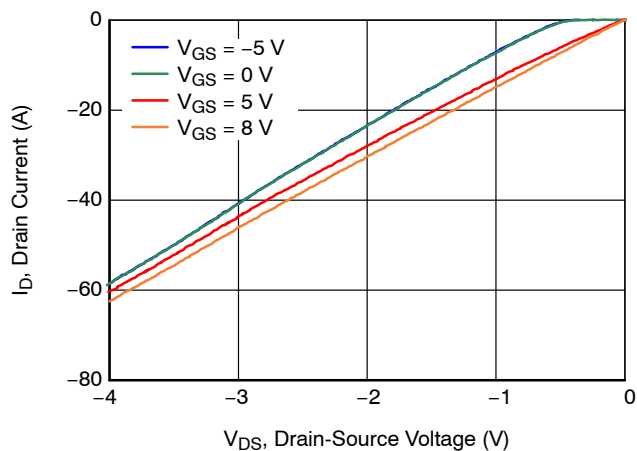
**Figure 8. Typical Gate Charge at  $V_{DS} = 400\text{ V}$  and  $I_D = 40\text{ A}$**



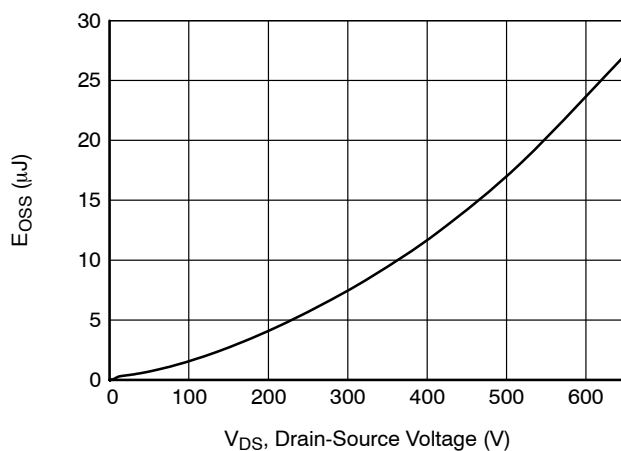
**Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55\text{ °C}$**



**Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25\text{ °C}$**



**Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175\text{ °C}$**



**Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0\text{ V}$**

TYPICAL PERFORMANCE DIAGRAMS (continued)

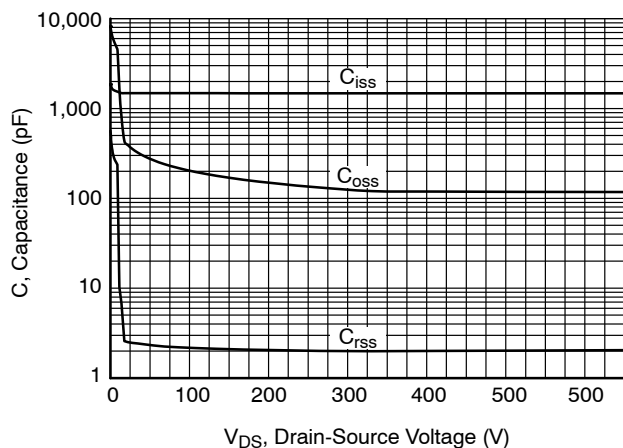


Figure 13. Typical Capacitances at  $f = 100 \text{ kHz}$  and  $V_{GS} = 0 \text{ V}$

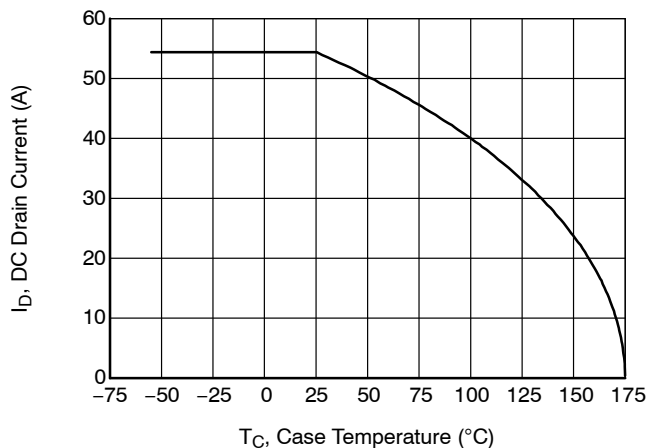


Figure 14. DC Drain Current Derating

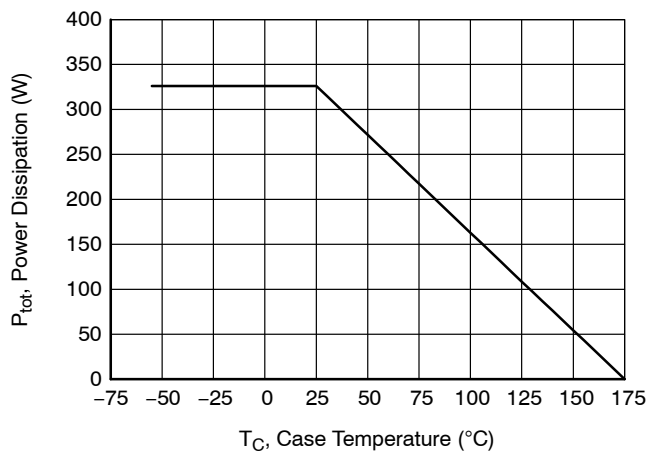


Figure 15. Total Power Dissipation

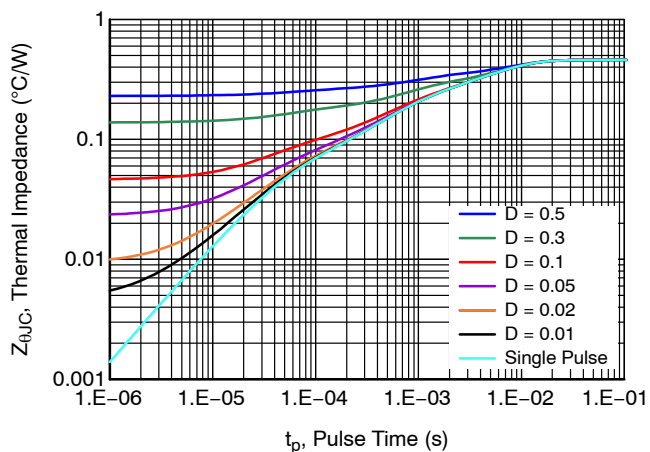


Figure 16. Maximum Transient Thermal Impedance

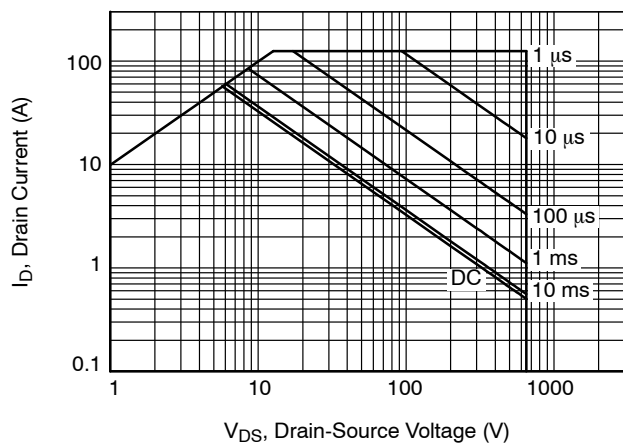


Figure 17. Safe Operation Area at  $T_C = 25 \text{ °C}$ ,  $D = 0$ , Parameter  $t_p$

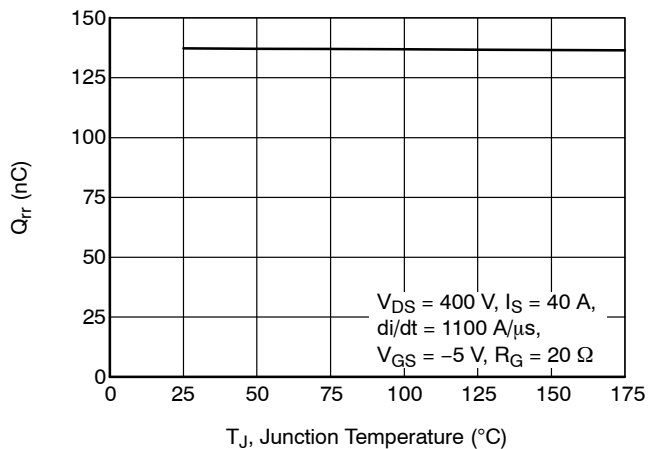
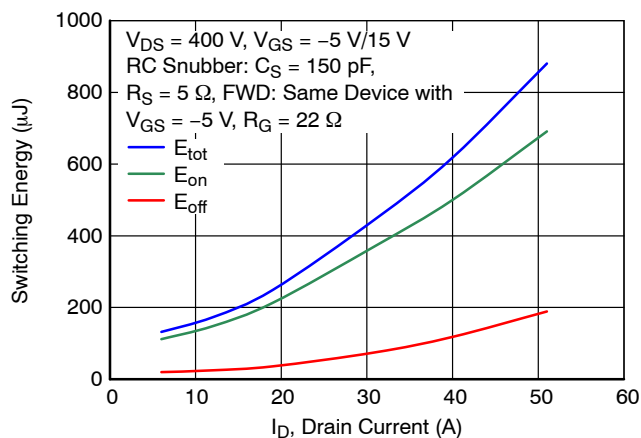
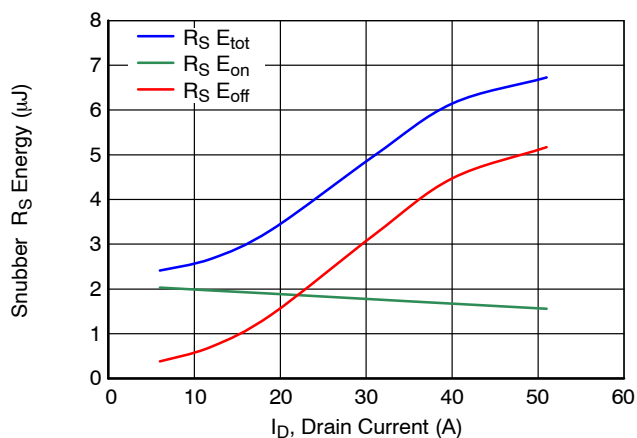


Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature

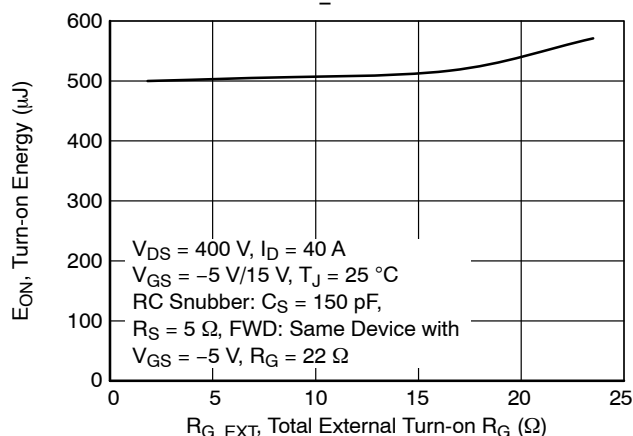
## TYPICAL PERFORMANCE DIAGRAMS (continued)



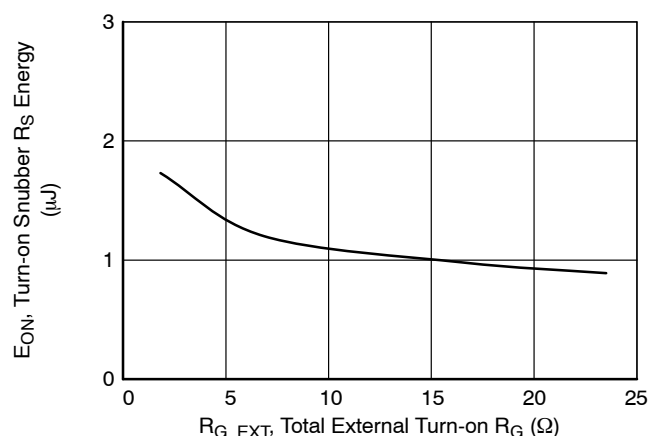
**Figure 19. Clamped Inductive Switching Energy vs. Drain Current at  $T_J = 25\text{ }^{\circ}\text{C}$ , Turn-on  $R_{G\_EXT} = 1.8\text{ }\Omega$ , and Turn-off  $R_{G\_EXT} = 22\text{ }\Omega$**



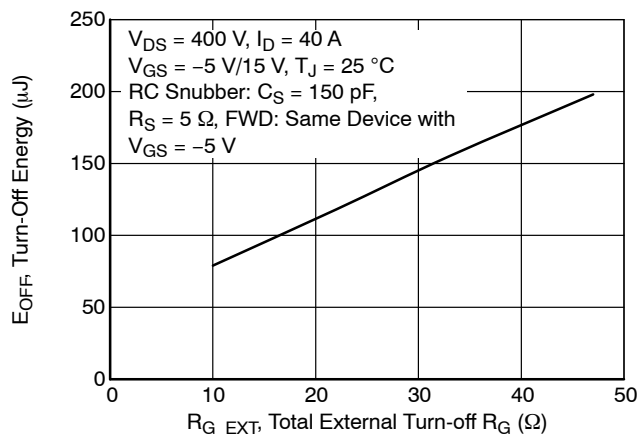
**Figure 20. RC Snubber Energy Loss vs. Drain Current at the Test Conditions Shown in Figure 19**



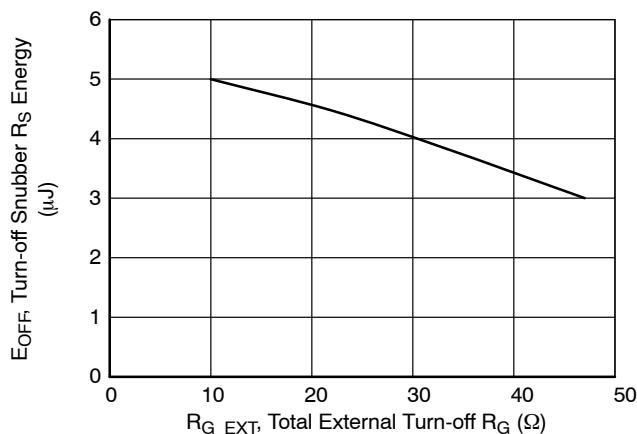
**Figure 21. Clamped Inductive Switching Turn-on Energy Including RC Snubber Energy Loss as a Function of Total External Turn-on Gate Resistor  $R_{G\_EXT}$**



**Figure 22. RC Snubber Energy Loss as a Function of Total External Turn-on Gate Resistor  $R_{G\_EXT}$  at the Test Conditions Shown in Figure 21**

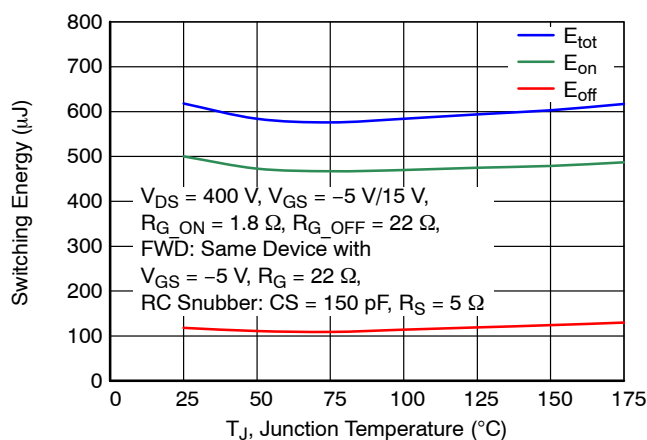


**Figure 23. Clamped Inductive Switching Turn-off Energy Including RC Snubber Energy Loss as a Function of Total External Turn-off Gate Resistor  $R_{G\_EXT}$**

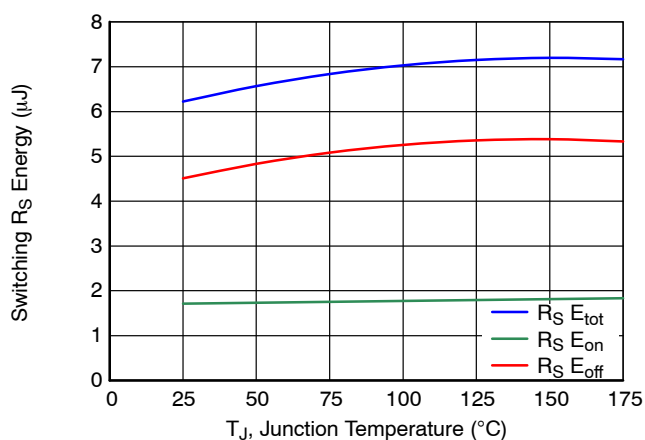


**Figure 24. RC Snubber Energy Loss as a Function of Total External Turn-off Gate Resistor  $R_{G\_EXT}$  at the Test Conditions Shown in Figure 23**

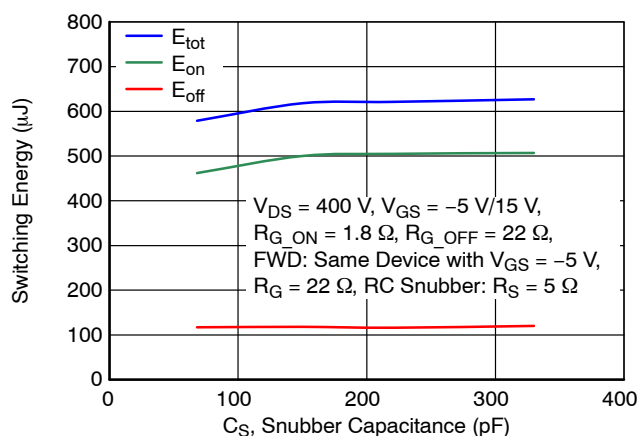
## TYPICAL PERFORMANCE DIAGRAMS (continued)



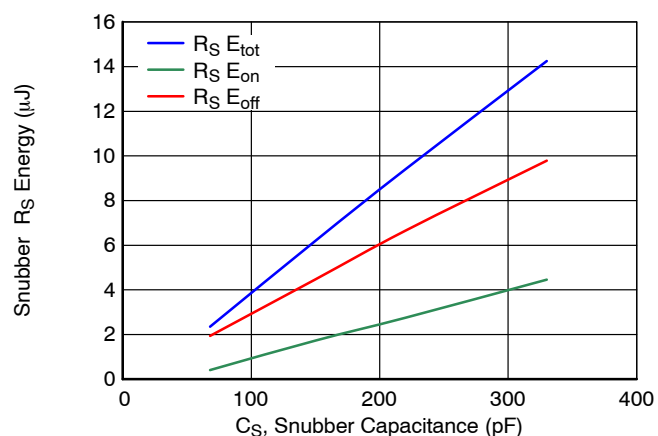
**Figure 25. Clamped Inductive Switching Energy Including RC Snubber Energy Loss as a Function of Junction Temperature at  $I_D = 40$  A**



**Figure 26. RC Snubber Energy Loss as a Function of Junction Temperature at the Test Conditions Shown in Figure 25**

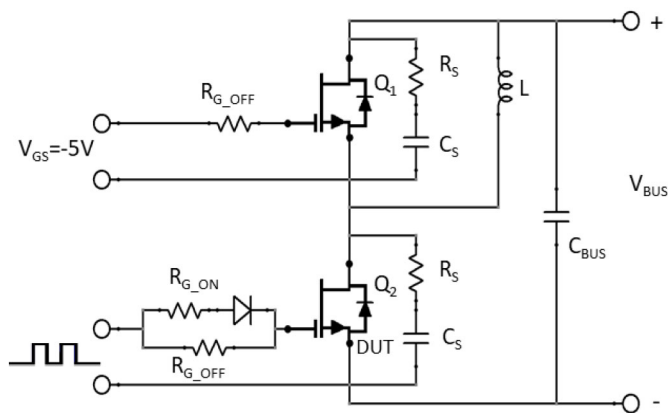


**Figure 27. Clamped Inductive Switching Energy Including RC Snubber Energy Loss as a Function of Snubber Capacitance at  $I_D = 40$  A and  $T_J = 25$  °C**



**Figure 28. RC Snubber Energy Loss as a Function of Snubber Capacitance at the Test Conditions Shown in Figure 27**

**UF3C065040K3S**



**Figure 29. Clamped Inductive Load Switching Test Circuit With An RC Snubber ( $R_S = 5\ \Omega$  and  $C_S = 150\ \text{pF}$ )**

## APPLICATIONS INFORMATION

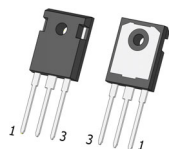
SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_g$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction

capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.onsemi.com](http://www.onsemi.com).

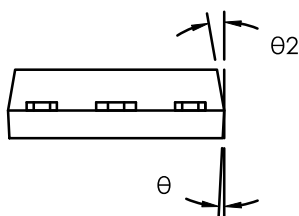
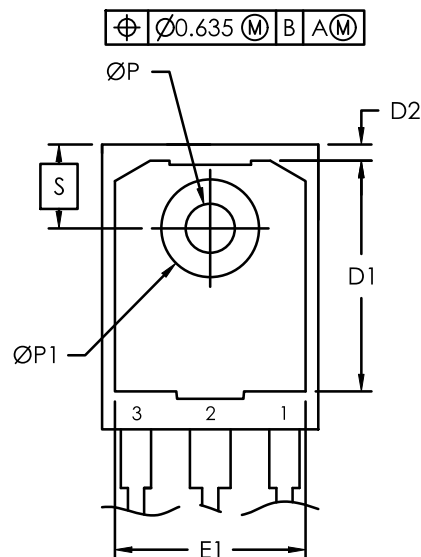
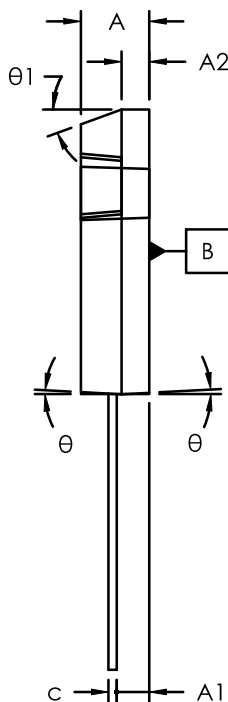
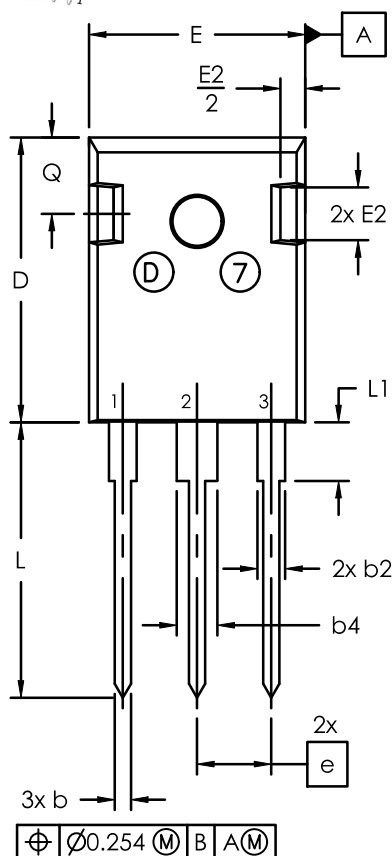
## ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UF3C065040K3S	UF3C065040K3S	TO247-3 (Pb-Free, Halogen Free)	600 / Tube



TO247-3 15.90x20.96x5.03, 5.44P  
CASE 340AK  
ISSUE B

DATE 14 APR 2025



NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
b4	2.59	3.00	3.43
c	0.38	0.60	0.89
D	20.70	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	5.44 BSC		
E1	13.00	13.30	13.60
E2	3.43	3.89	5.20
L	19.62	20.27	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.15 BSC		
θ	3°		
θ1	20°		
θ2	10°		

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DESCRIPTION: TO247-3 15.90x20.96x5.03, 5.44P

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