

# Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-263-7, 1200 V, 53 mohm

## UF4C120053B7S

### Description

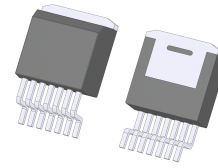
The UF4C120053B7S is a 1200 V, 53 mΩ G4 SiC FET. It is based on a unique “cascode” circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving TO-263-7 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

### Features

- On-resistance  $R_{DS(on)}$ : 53 mΩ (Typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery:  $Q_{rr}$  = 98 nC
- Low Body Diode  $V_{FSD}$ : 1.28 V
- Low Gate Charge:  $Q_G$  = 37.8 nC
- Threshold Voltage  $V_{G(th)}$ : 4.8 V (Typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- TO-263-7 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

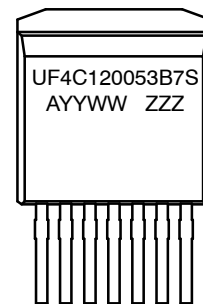
### Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Induction Heating



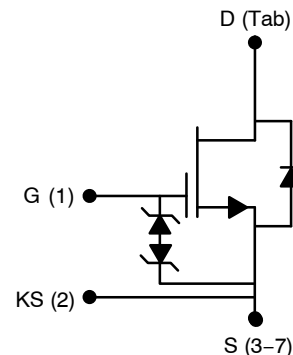
TO-263-7 10.18x9.08x4.43, 1.27P  
CASE 418BA

### MARKING DIAGRAM



UF4C120053B7S = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# UF4C120053B7S

## MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	$V_{DS}$		1200	V
Gate-source Voltage	$V_{GS}$	DC	-20 to +20	V
		AC ( $f > 1$ Hz)	-25 to +25	V
Continuous Drain Current (Note 1)	$I_D$	$T_C = 25\text{ }^{\circ}\text{C}$	34	A
		$T_C = 100\text{ }^{\circ}\text{C}$	24.6	A
Pulsed Drain Current (Note 2)	$I_{DM}$	$T_C = 25\text{ }^{\circ}\text{C}$	100	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	$L = 15\text{ mH}$ , $I_{AS} = 2.7\text{ A}$	54.6	mJ
SiC FET dv/dt Ruggedness	dv/dt	$V_{DS} \leq 800\text{ V}$	150	V/ns
Power Dissipation	$P_{tot}$	$T_C = 25\text{ }^{\circ}\text{C}$	250	W
Maximum Junction Temperature	$T_{J, max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	$T_J$ , $T_{STG}$		-55 to 175	$^{\circ}\text{C}$
Reflow Soldering Temperature	$T_{solder}$	Reflow MSL 1	245	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Limited by  $T_{J, max}$ .
- Pulse width  $t_p$  limited by  $T_{J, max}$ .
- Starting  $T_J = 25\text{ }^{\circ}\text{C}$ .

## THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.46	0.60	$^{\circ}\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

### TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	$BV_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1200	-	-	V
Total Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	0.2	50	$\mu\text{A}$
		$V_{DS} = 1200\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	15	-	
Total Gate Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $T_J = 25\text{ }^{\circ}\text{C}$ , $V_{GS} = -20\text{ V} / +20\text{ V}$	-	6	20	$\mu\text{A}$
Drain-source On-resistance	$R_{DS(on)}$	$V_{GS} = 12\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	53	67	$\text{m}\Omega$
		$V_{GS} = 12\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	112	-	
		$V_{GS} = 12\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	159	-	
Gate Threshold Voltage	$V_{G(th)}$	$V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$	4	4.8	6	V
Gate Resistance	$R_G$	$f = 1\text{ MHz}$ , open drain	-	4.5	-	$\Omega$

### TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 1)	$I_S$	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	34	A
Diode Pulse Current (Note 2)	$I_{S, pulse}$	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	100	A
Forward Voltage	$V_{FSD}$	$V_{GS} = 0\text{ V}$ , $I_S = 10\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	1.28	1.65	V
		$V_{GS} = 0\text{ V}$ , $I_S = 10\text{ A}$ , $T_J = 175\text{ }^{\circ}\text{C}$	-	1.96	-	
Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800\text{ V}$ , $I_S = 25\text{ A}$ , $V_{GS} = -5\text{ V}$ , $R_G = 20\text{ }\Omega$ , $di/dt = 1600\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^{\circ}\text{C}$	-	98	-	nC
Reverse Recovery Time	$t_{rr}$		-	15.2	-	ns

# UF4C120053B7S

## ELECTRICAL CHARACTERISTICS ( $T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----------------	-----	-----	-----	------

### TYPICAL PERFORMANCE – REVERSE DIODE

Reverse Recovery Charge	$Q_{rr}$	$V_{DS} = 800\text{ V}$ , $I_S = 25\text{ A}$ , $V_{GS} = -5\text{ V}$ , $R_G = 20\text{ }\Omega$ , $di/dt = 1600\text{ A}/\mu\text{s}$ , $T_J = 150\text{ }^{\circ}\text{C}$	–	105	–	nC
Reverse Recovery Time	$t_{rr}$		–	19.6	–	ns

### TYPICAL PERFORMANCE – DYNAMIC

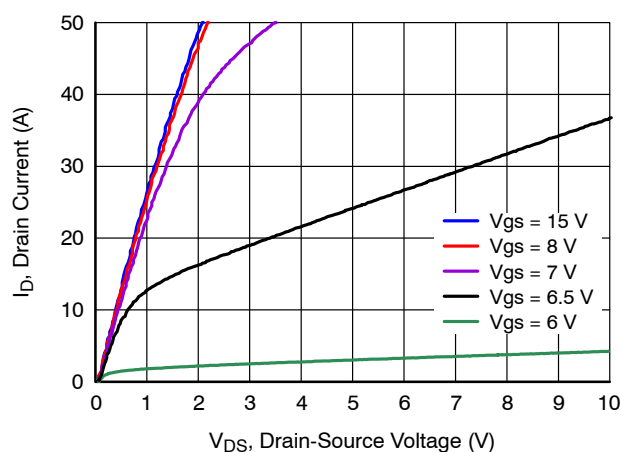
Input Capacitance	$C_{iss}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 100\text{ kHz}$	–	1370	–	pF
Output Capacitance	$C_{oss}$		–	43.5	–	
Reverse Transfer Capacitance	$C_{rss}$		–	2.2	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}$ , $V_{GS} = 0\text{ V}$	–	54	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	100	–	
$C_{oss}$ Stored Energy	$E_{oss}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$	–	17.3	–	$\mu\text{J}$
Total Gate Charge	$Q_G$	$V_{DS} = 800\text{ V}$ , $I_D = 25\text{ A}$ , $V_{GS} = 0\text{ V to } 15\text{ V}$	–	37.8	–	nC
Gate-drain Charge	$Q_{GD}$		–	9.5	–	
Gate-source Charge	$Q_{GS}$		–	10	–	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 800\text{ V}$ , $I_D = 25\text{ A}$ , Gate Driver = $-5\text{ V to } +15\text{ V}$ , $R_{G\_ON} = 1\text{ }\Omega$ , $R_{G\_OFF} = 20\text{ }\Omega$ , Inductive Load, FWD: Same Device with $V_{GS} = -5\text{ V}$ and $R_G = 20\text{ }\Omega$ , Snubber: $R_S = 20\text{ }\Omega$ , $C_S = 100\text{ pF}$ , $T_J = 25\text{ }^{\circ}\text{C}$ (Note 4), (Note 5)	–	20	–	ns
Rise Time	$t_r$		–	32	–	
Turn-off Delay Time	$t_{d(off)}$		–	57	–	
Fall Time	$t_f$		–	12	–	
Turn-on Energy Including $R_S$ Energy	$E_{ON}$		–	570	–	$\mu\text{J}$
Turn-off Energy Including $R_S$ Energy	$E_{OFF}$		–	57	–	
Total Switching Energy	$E_{TOTAL}$		–	627	–	
Snubber $R_S$ Energy During Turn-on	$E_{RS\_ON}$		–	5	–	
Snubber $R_S$ Energy During Turn-off	$E_{RS\_OFF}$		–	11	–	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 800\text{ V}$ , $I_D = 25\text{ A}$ , Gate Driver = $-5\text{ V to } +15\text{ V}$ , $R_{G\_ON} = 1\text{ }\Omega$ , $R_{G\_OFF} = 20\text{ }\Omega$ , Inductive Load, FWD: Same Device with $V_{GS} = -5\text{ V}$ and $R_G = 20\text{ }\Omega$ , Snubber: $R_S = 20\text{ }\Omega$ , $C_S = 100\text{ pF}$ , $T_J = 150\text{ }^{\circ}\text{C}$ (Note 4), (Note 5)	–	24	–	ns
Rise Time	$t_r$		–	33	–	
Turn-off Delay Time	$t_{d(off)}$		–	63	–	
Fall Time	$t_f$		–	13	–	
Turn-on Energy Including $R_S$ Energy	$E_{ON}$		–	660	–	$\mu\text{J}$
Turn-off Energy Including $R_S$ Energy	$E_{OFF}$		–	75	–	
Total Switching Energy	$E_{TOTAL}$		–	735	–	
Snubber $R_S$ Energy During Turn-on	$E_{RS\_ON}$		–	5	–	
Snubber $R_S$ Energy During Turn-off	$E_{RS\_OFF}$		–	12	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

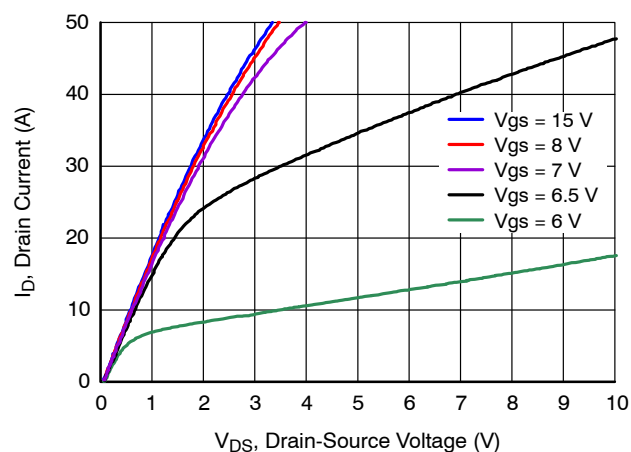
4. Measured with the switching test circuit in Figure 26.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

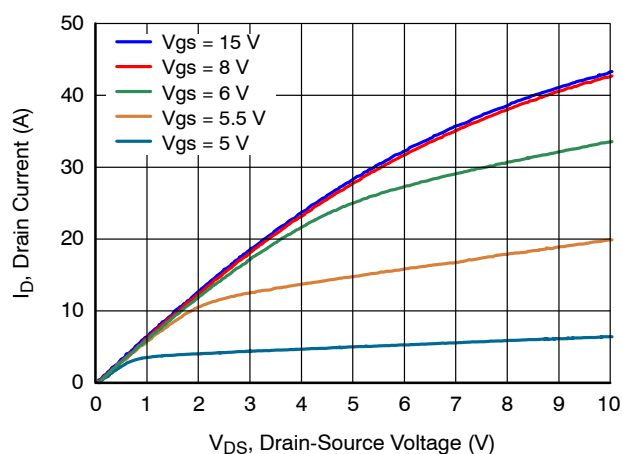
# TYPICAL PERFORMANCE DIAGRAMS



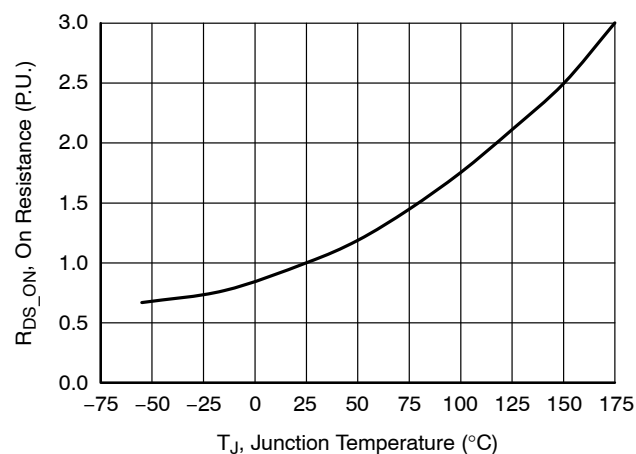
**Figure 1. Typical Output Characteristics at  $T_J = -55\text{ }^{\circ}\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$**



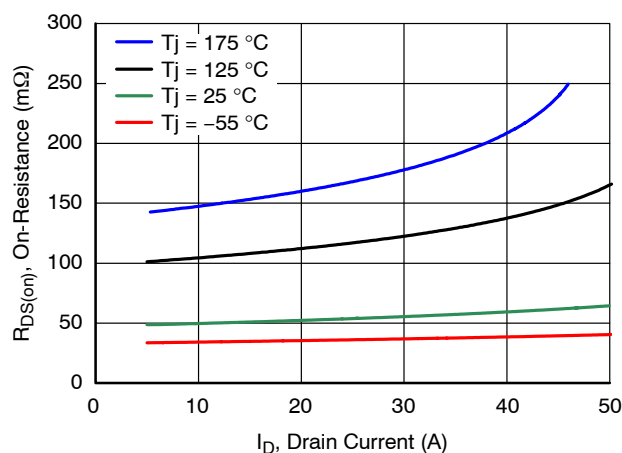
**Figure 2. Typical Output Characteristics at  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$**



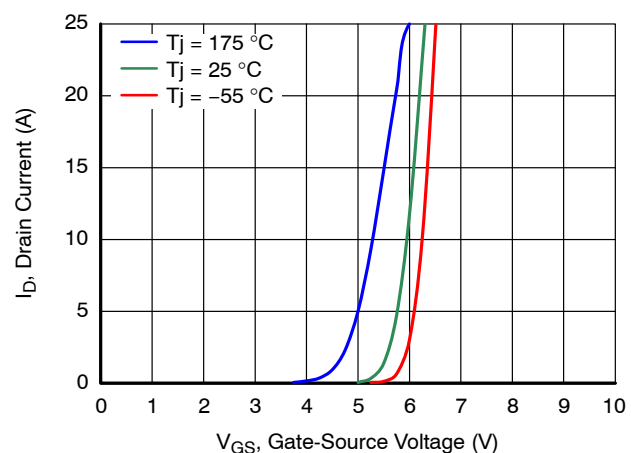
**Figure 3. Typical Output Characteristics at  $T_J = 175\text{ }^{\circ}\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$**



**Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\text{ V}$  and  $I_D = 25\text{ A}$**



**Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\text{ V}$**



**Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\text{ V}$**

TYPICAL PERFORMANCE DIAGRAMS (continued)

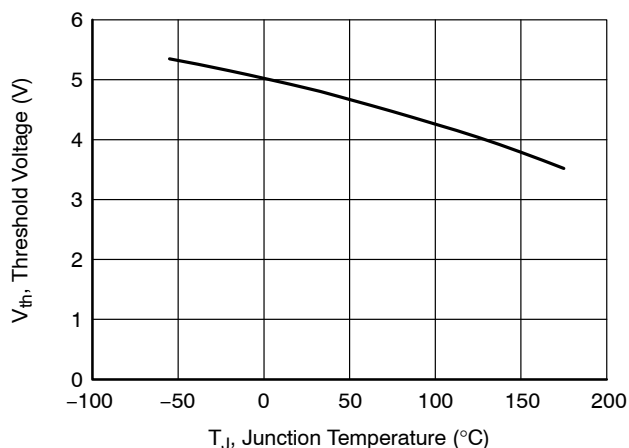


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5 \text{ V}$  and  $I_D = 10 \text{ mA}$

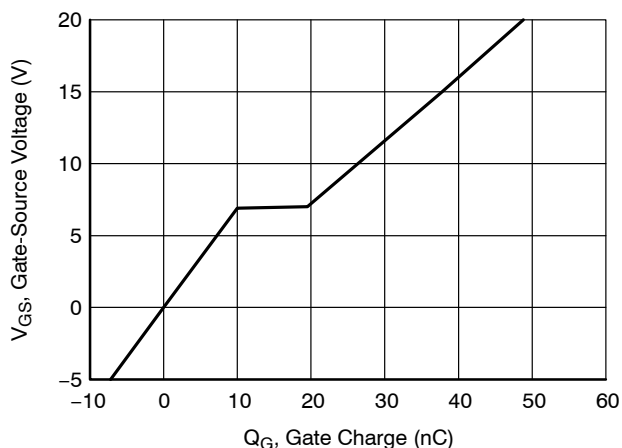


Figure 8. Typical Gate Charge at  $V_{DS} = 800 \text{ V}$  and  $I_D = 25 \text{ A}$

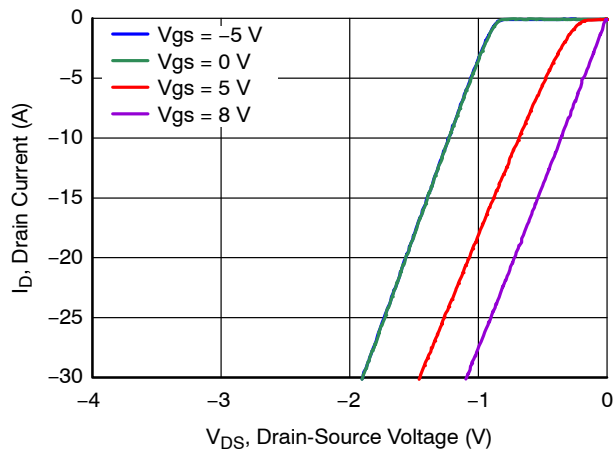


Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55 \text{ }^{\circ}\text{C}$

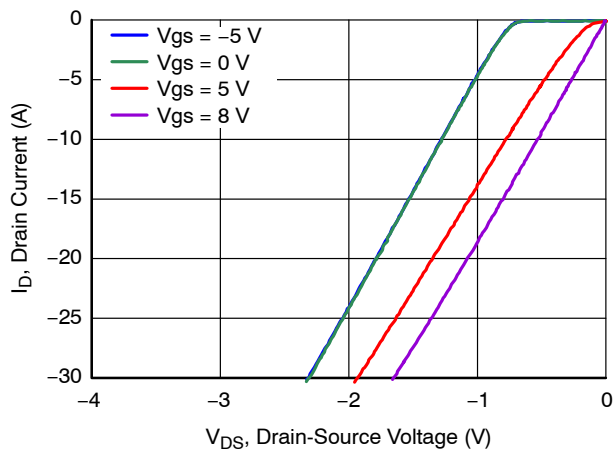


Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25 \text{ }^{\circ}\text{C}$

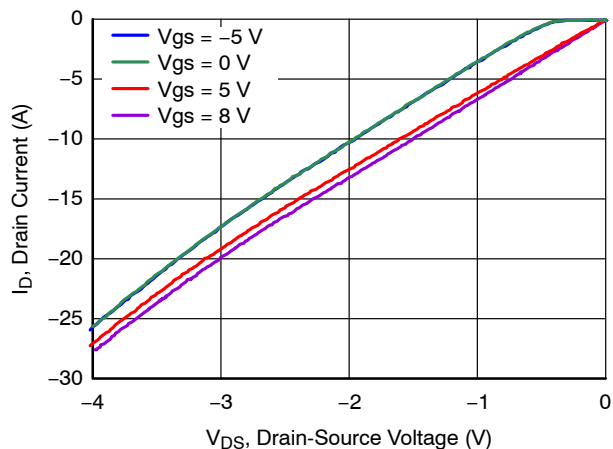


Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175 \text{ }^{\circ}\text{C}$

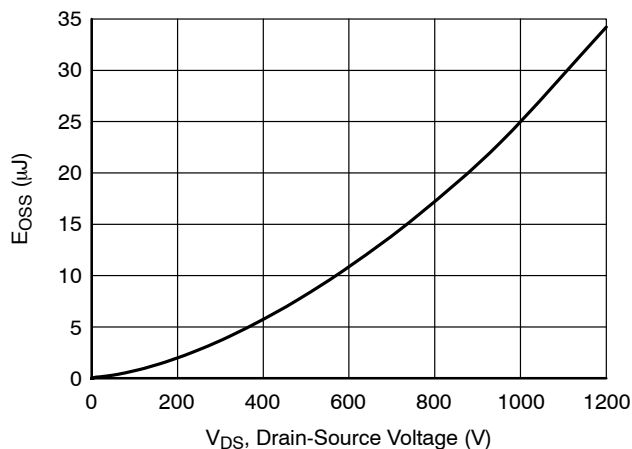


Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0 \text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

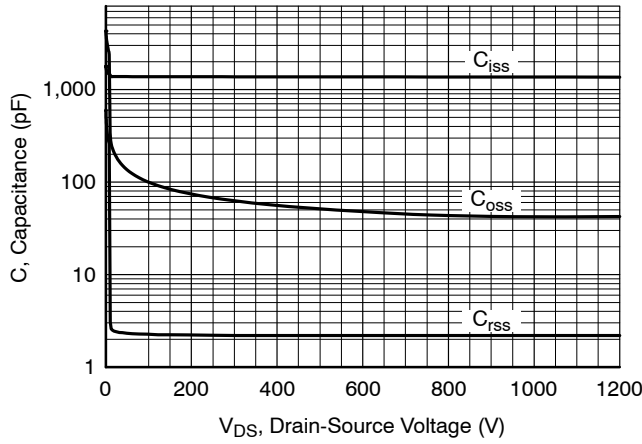


Figure 13. Typical Capacitances at  $f = 100$  kHz and  $V_{GS} = 0$  V

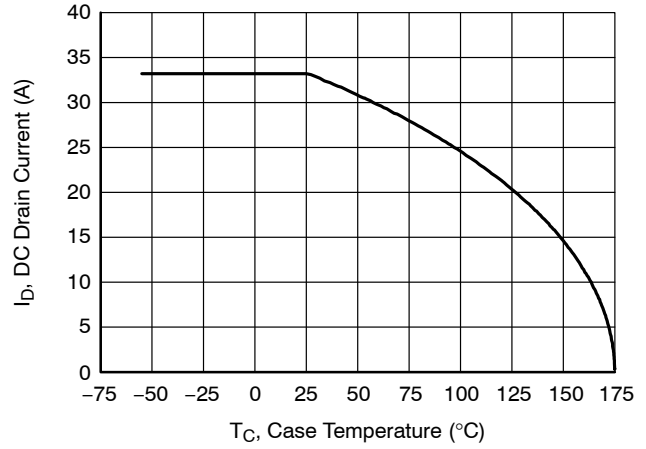


Figure 14. DC Drain Current Derating

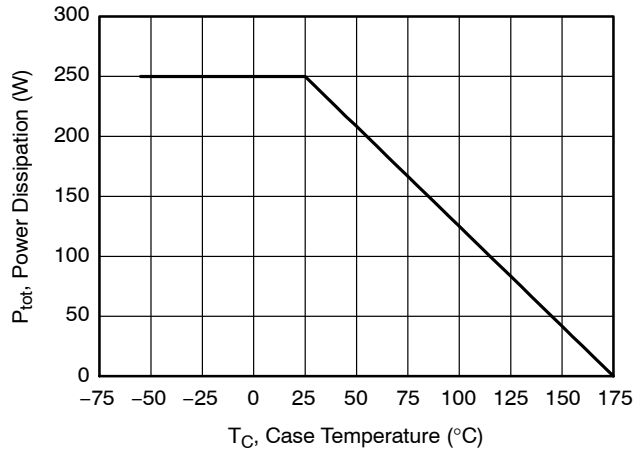


Figure 15. Total Power Dissipation

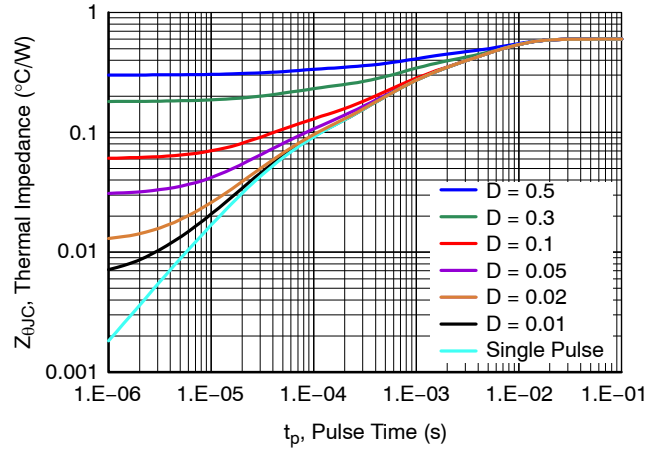


Figure 16. Maximum Transient Thermal Impedance

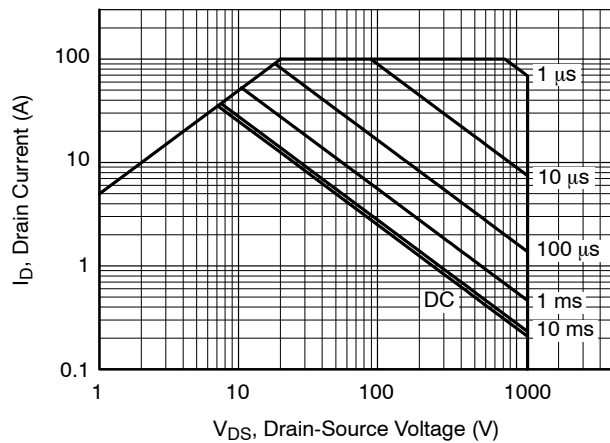


Figure 17. Safe Operation Area at  $T_C = 25$  °C,  $D = 0$ , Parameter  $t_p$

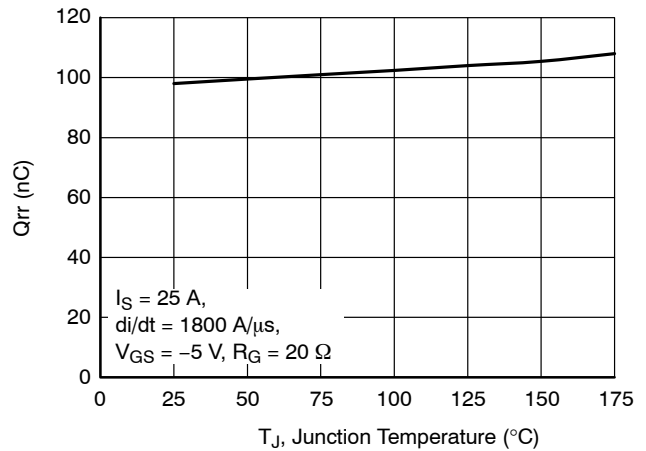
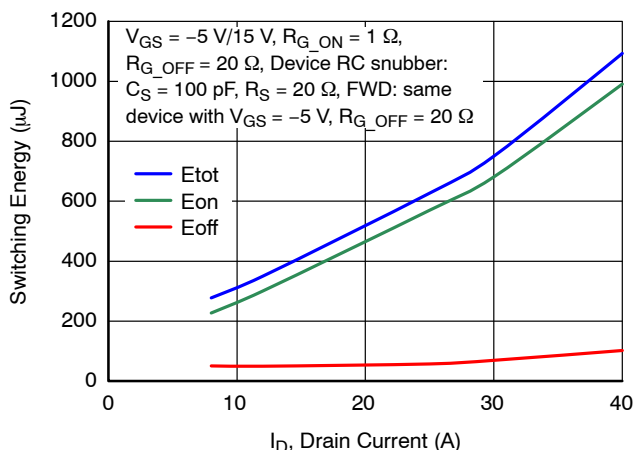
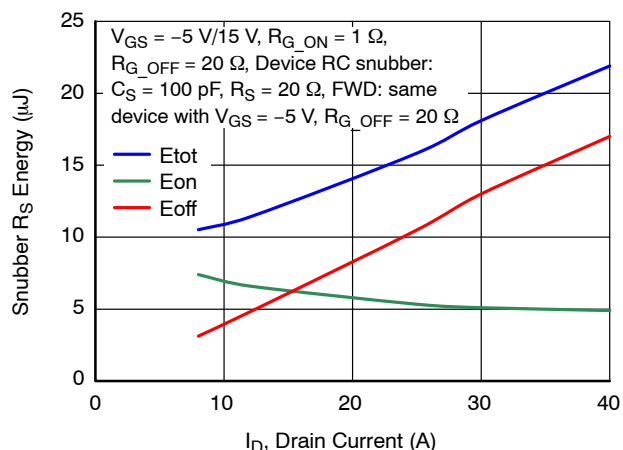


Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature at  $V_{DS} = 800$  V

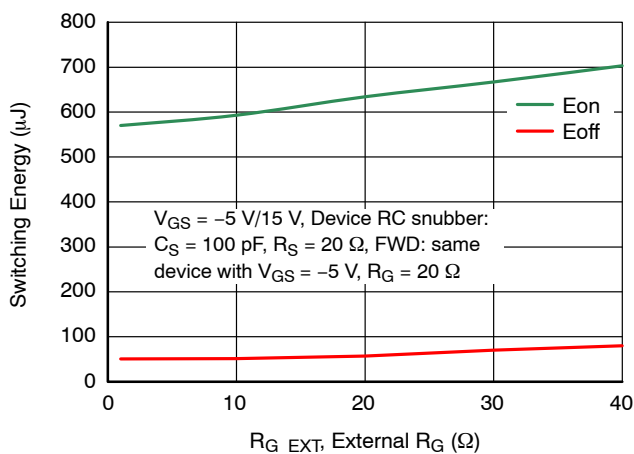
## TYPICAL PERFORMANCE DIAGRAMS (continued)



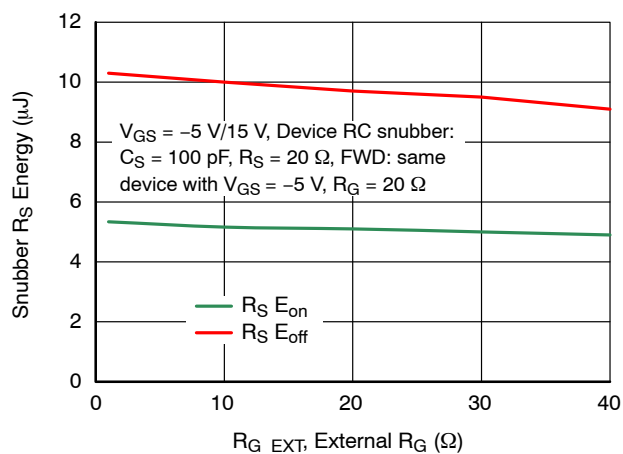
**Figure 19. Clamped Inductive Switching Energy vs. Drain Current at  $V_{DS} = 800$  V and  $T_J = 25$  °C**



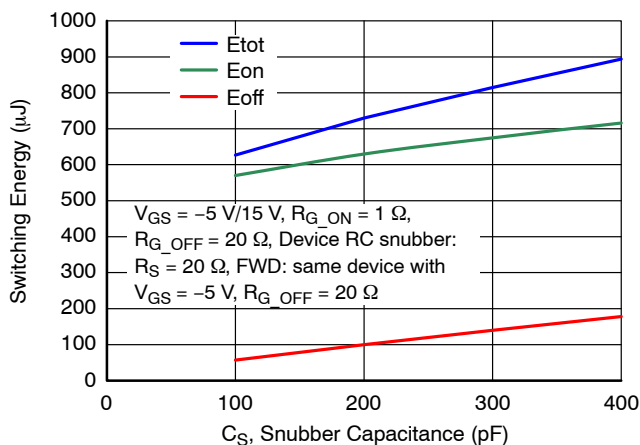
**Figure 20. RC Snubber Energy Loss vs.  $R_{G,EXT}$  at  $V_{DS} = 800$  V,  $I_D = 25$  A, and  $T_J = 25$  °C**



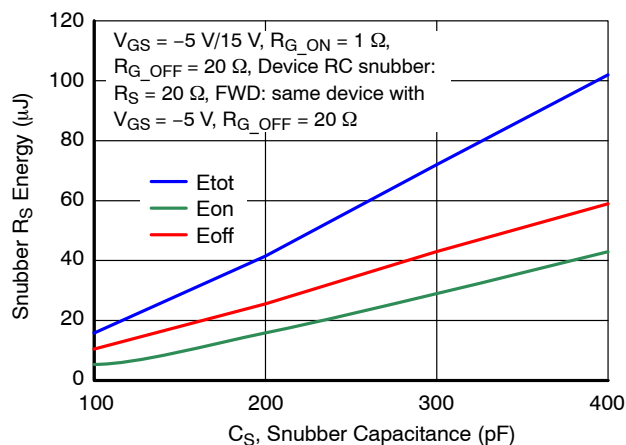
**Figure 21. Clamped Inductive Switching Energies vs.  $R_{G,EXT}$  at  $V_{DS} = 800$  V,  $I_D = 25$  A, and  $T_J = 25$  °C**



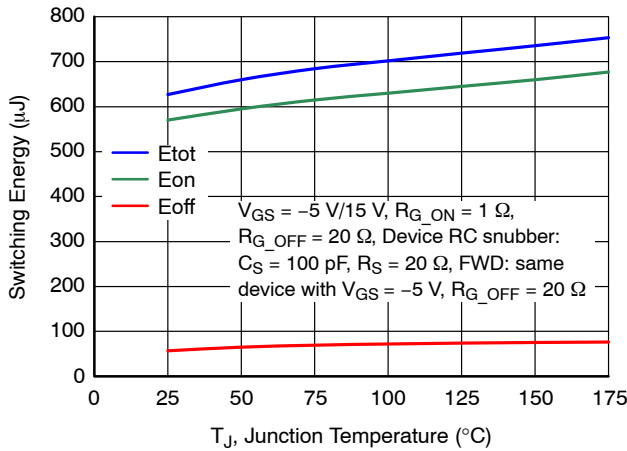
**Figure 22. RC Snubber Energy Loss vs.  $R_{G,EXT}$  at  $V_{DS} = 800$  V,  $I_D = 25$  A, and  $T_J = 25$  °C**



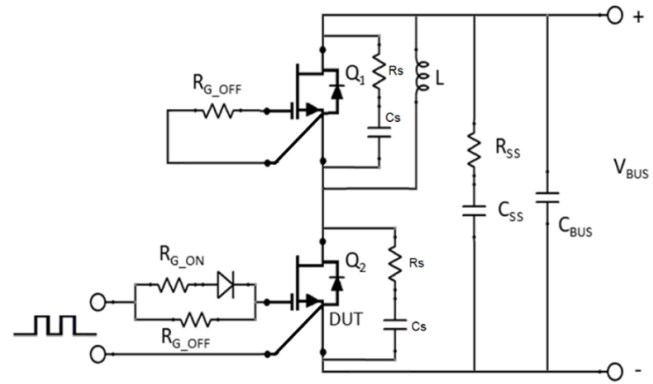
**Figure 23. Clamped Inductive Switching Energies vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 800$  V,  $I_D = 25$  A, and  $T_J = 25$  °C**



**Figure 24. RC Snubber Energy Losses vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 800$  V,  $I_D = 25$  A, and  $T_J = 25$  °C**



**Figure 25. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 800$  V and  $I_D = 25$  A**



**Figure 26. Schematic of the Half-bridge Mode Switching Test Circuit with Device RC Snubbers ( $R_S = 20$  Ω,  $C_S = 100$  pF) and a Bus RC Snubber ( $R_{SS} = 2.5$  Ω,  $C_{SS} = 100$  nF)**

## APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.onsemi.com](http://www.onsemi.com).

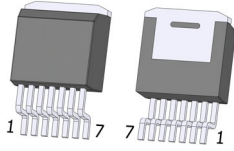
A snubber circuit with a small  $R_G$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_G$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_G$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_G$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_G$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at [www.onsemi.com](http://www.onsemi.com)

## ORDERING INFORMATION

Part Number	Marking	Package	Shipping <sup>†</sup>
UF4C120053B7S	UF4C120053B7S	TO-263-7	800 / Tape & Reel

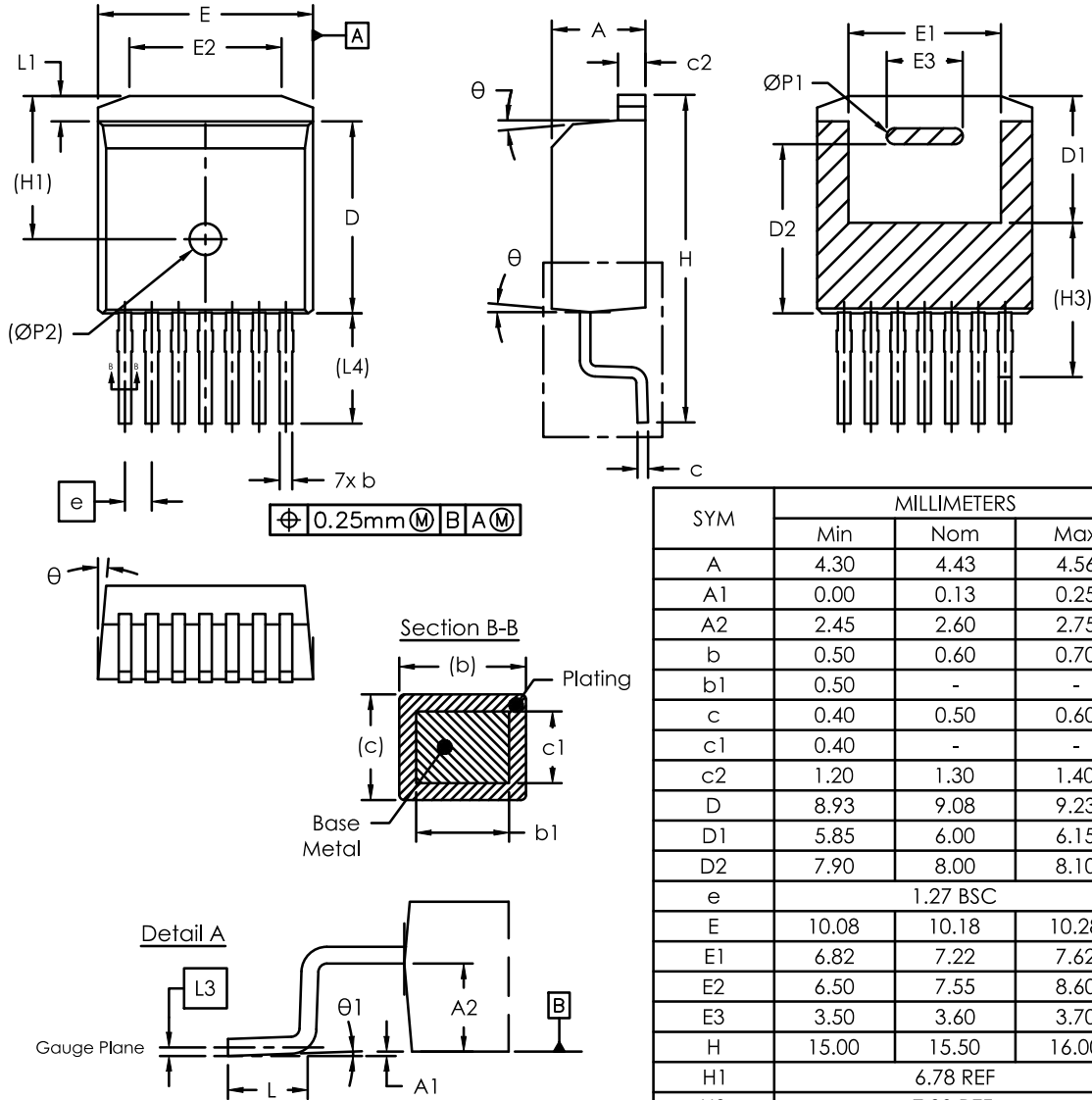
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://www.onsemi.com).





**TO-263-7 10.18x9.08x4.43, 1.27P**  
**CASE 418BA**  
**ISSUE B**

DATE 17 APR 2025



SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
$\theta$	5°		
$\theta_1$	3°		

**Notes:**

1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

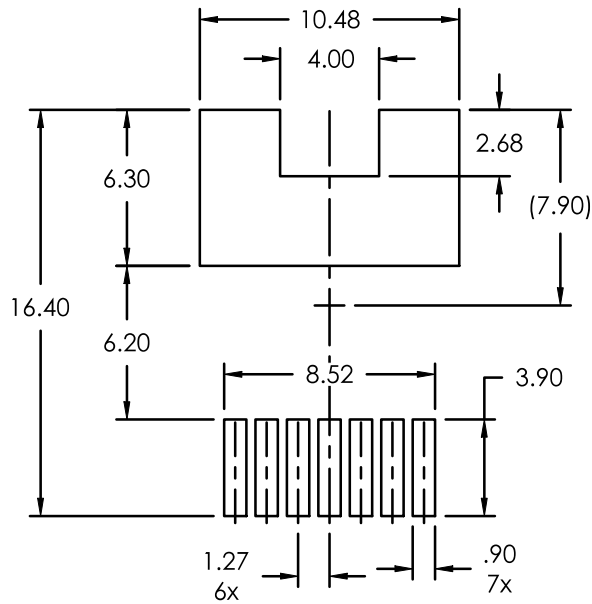
<b>DOCUMENT NUMBER:</b>	<b>98AON13800G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-263-7 10.18x9.08x4.43, 1.27P</b>	<b>PAGE 1 OF 2</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

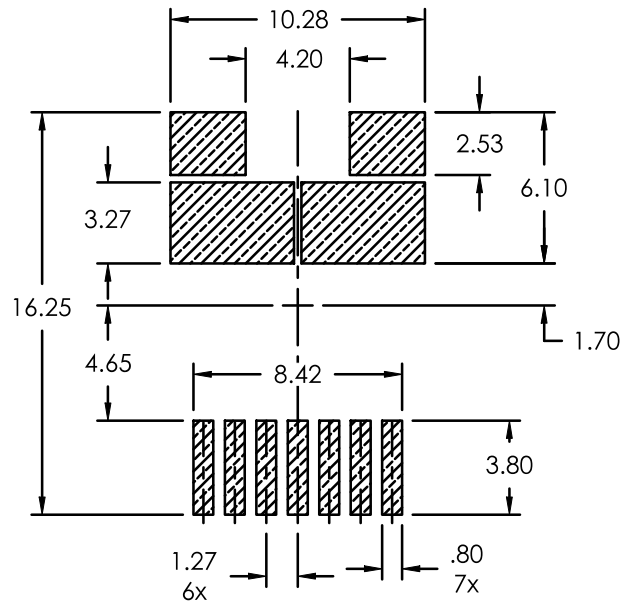
TO-263-7 10.18x9.08x4.43, 1.27P  
CASE 418BA  
ISSUE B

DATE 17 APR 2025

RECOMMENDED PCB FOOTPRINT

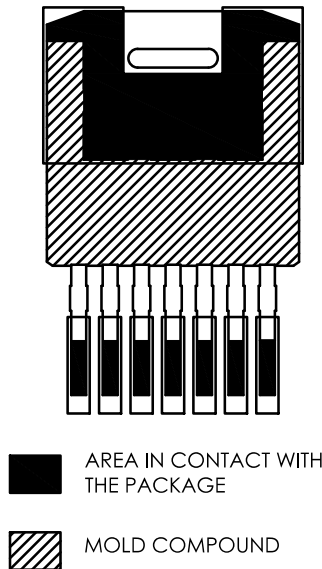


RECOMMENDED STENCIL APERTURE



NOTE: LAND PATTERN AND STENCIL APERTURE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE. END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

PCB FOOTPRINT with PACKAGE OVERLAY



DOCUMENT NUMBER:	98AON13800G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-263-7 10.18x9.08x4.43, 1.27P	PAGE 2 OF 2

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)