Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO247-4, 750 V, 33 mohm

UJ4C075033K4S

Description

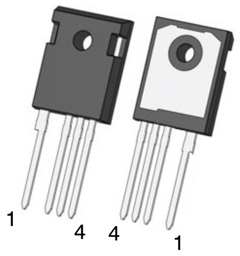
The UJ4C075033K4S is a 750 V, 33 mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO247-4 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 33 mΩ (Typ)
- Operating Temperature of 175 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 88 nC
- Low Body Diode V_{FSD}: 1.26 V
- Low Gate Charge: Q_G = 37.8 nC
- Threshold Voltage $V_{G(th)}$: 4.8 V (Typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- TO247-4 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

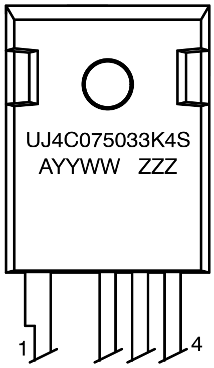
Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



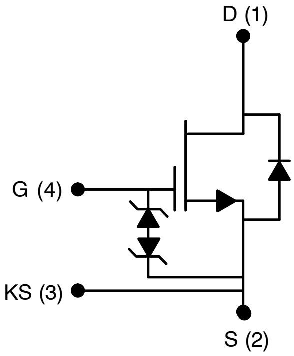
TO247-4
CASE 340AN

MARKING DIAGRAM



UJ4C075033K4S	= Specific Device Code
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		750	V
Gate-source Voltage	V_{GS}	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	T_C = 25 °C	47	A
		T_C = 100 °C	35	A
Pulsed Drain Current (Note 2)	I_{DM}	T_C = 25 °C	140	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L = 15 mH, I_{AS} = 2.4 A	43	mJ
SiC FET dv/dt Ruggedness	dv/dt	$V_{DS} \leq 500$ V	200	V/ns
Power Dissipation	P_{tot}	T_C = 25 °C	242	W
Maximum Junction Temperature	$T_{J,\,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Max. Lead Temperature for Soldering, 1/8” from Case for 5 Seconds	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,\,max}$.
2. Pulse width t_p limited by $T_{J,\,max}$.
3. Starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.48	0.62	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1 mA	750	–	–	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 750 V, V_{GS} = 0 V, T_J = 25 °C	–	2	20	μA
		V_{DS} = 750 V, V_{GS} = 0 V, T_J = 175°C	–	20	–	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, T_J = 25 °C, V_{GS} = −20 V / +20 V	–	6	±20	μA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 30 A, T_J = 25°C	–	33	41	mΩ
		V_{GS} = 12 V, I_D = 30 A, T_J = 125°C	–	57	–	
		V_{GS} = 12 V, I_D = 30 A, T_J = 175°C	–	75	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 10 mA	4	4.8	6	V
Gate Resistance	R_G	f = 1 MHz, open drain	–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE						
Diode Continuous Forward Current (Note 1)	I_S	T_C = 25 °C	–	–	47	A
Diode Pulse Current (Note 2)	$I_{S,\ pulse}$	T_C = 25 °C	–	–	140	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 15 A, T_J = 25 °C	–	1.26	1.42	V
		V_{GS} = 0 V, I_S = 15 A, T_J = 175 °C	–	1.59	–	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 30 A, V_{GS} = 0 V, R_{G_EXT} = 5 Ω, di/dt = 3100 A/μs, T_J = 25 °C	–	88	–	nC
Reverse Recovery Time	t_{rr}		–	11.5	–	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 30 A, V_{GS} = 0 V, R_{G_EXT} = 5 Ω, di/dt = 3100 A/μs, T_J = 150 °C	–	95	–	nC
Reverse Recovery Time	t_{rr}		–	12	–	ns
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 kHz	–	1400	–	pF
Output Capacitance	C_{oss}		–	68	–	
Reverse Transfer Capacitance	C_{rss}		–	2.5	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	83	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	162	–	
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 400 V, V_{GS} = 0 V	–	6.6	–	μJ
Total Gate Charge	Q_G	V_{DS} = 400 V, I_D = 30 A, V_{GS} = 0 V to 15 V	–	37.8	–	nC
Gate-drain Charge	Q_{GD}		–	8	–	
Gate-source Charge	Q_{GS}		–	11.8	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,\ EXT}$ = 1 Ω, Turn-off $R_{G,\ EXT}$ = 5 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V, and R_G = 5 Ω, RC Snubber: R_S = 15 Ω and C_S = 100 pF, T_J = 25 °C (Notes 4 and 5)	–	12	–	ns
Rise Time	t_r		–	19	–	
Turn-off Delay Time	$t_{d(off)}$		–	18	–	
Fall Time	t_f		–	7	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	131	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	24	–	
Total Switching Energy	E_{TOTAL}		–	155	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	3.2	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	10	–	

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,\ EXT}$ = 1 Ω, Turn-off $R_{G,\ EXT}$ = 5 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V, and R_G = 5 Ω, RC Snubber: R_S = 15 Ω and C_S = 100 pF, T_J = 150 °C (Notes 4 and 5)	–	13	–	ns
Rise Time	t_r		–	21	–	
Turn-off Delay Time	$t_{d(off)}$		–	20	–	
Fall Time	t_f		–	9	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	160	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	41	–	
Total Switching Energy	E_{TOTAL}		–	201	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	3	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	9.6	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,\ EXT}$ = 1 Ω, Turn-off $R_{G,\ EXT}$ = 5 Ω, Inductive Load, FWD: UJ3D06520TS RC Snubber: R_S = 15 Ω and C_S = 100 pF, T_J = 25 °C (Note 6)	–	11.5	–	ns
Rise Time	t_r		–	19	–	
Turn-off Delay Time	$t_{d(off)}$		–	17.5	–	
Fall Time	t_f		–	6	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	114	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	22	–	
Total Switching Energy	E_{TOTAL}		–	136	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	4.1	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	14	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,\ EXT}$ = 1 Ω, Turn-off $R_{G,\ EXT}$ = 5 Ω, Inductive Load, FWD: UJ3D06520TS RC Snubber: R_S = 15 Ω and C_S = 100 pF, T_J = 150 °C (Note 6)	–	13	–	ns
Rise Time	t_r		–	16	–	
Turn-off Delay Time	$t_{d(off)}$		–	23	–	
Fall Time	t_f		–	7	–	
Turn-on Energy Including R_S Energy	E_{ON}		–	137	–	μJ
Turn-off Energy Including R_S Energy	E_{OFF}		–	39	–	
Total Switching Energy	E_{TOTAL}		–	176	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	4	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	14	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 35.
5. In this datasheet, all the switching energies (turn−on energy, turn−off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.
6. Measured with the switching test circuit in Figure 36.

TYPICAL PERFORMANCE DIAGRAMS

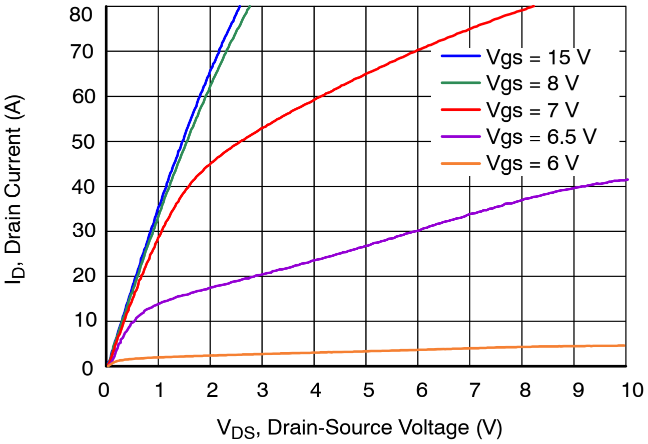


Figure 1. Typical Output Characteristics at $T_J = -55$ °C, $t_p < 250$ µs

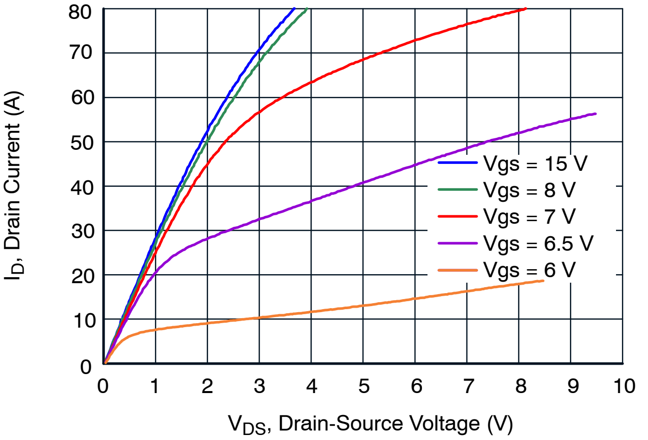


Figure 2. Typical Output Characteristics at $T_J = 25$ °C, $t_p < 250$ µs

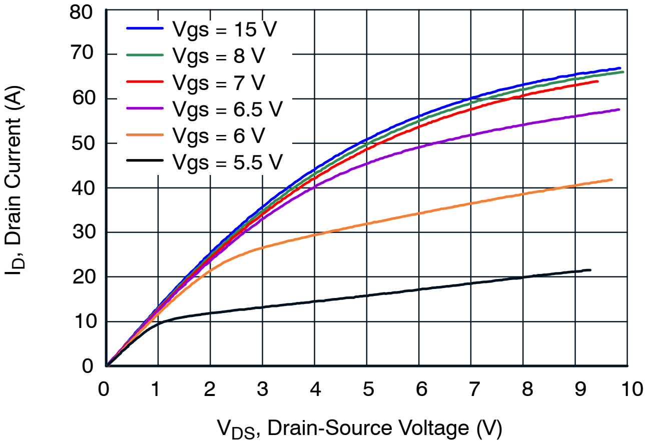


Figure 3. Typical Output Characteristics at $T_J = 175$ °C, $t_p < 250$ µs

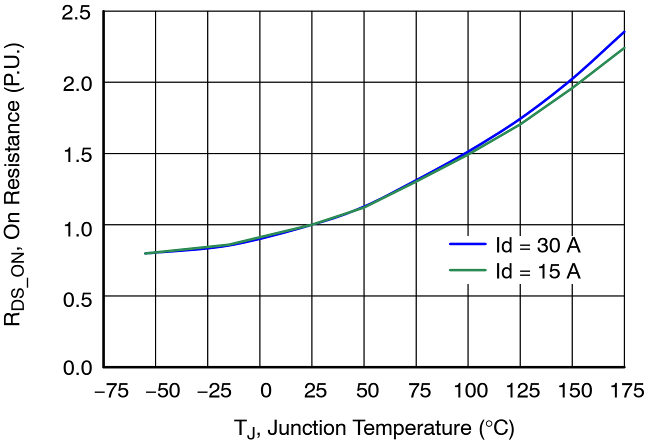


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12$ V

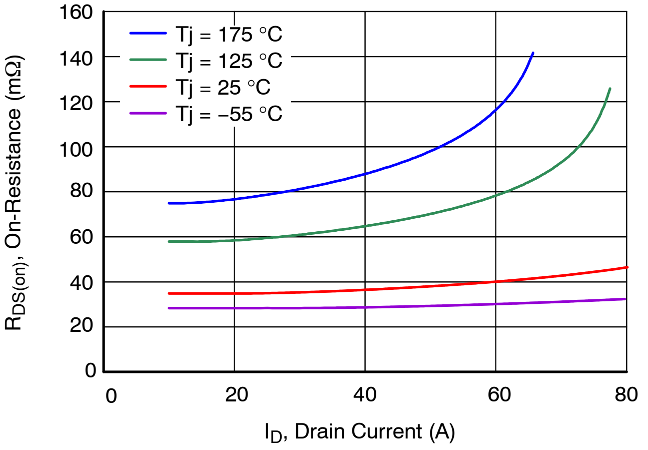


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12$ V

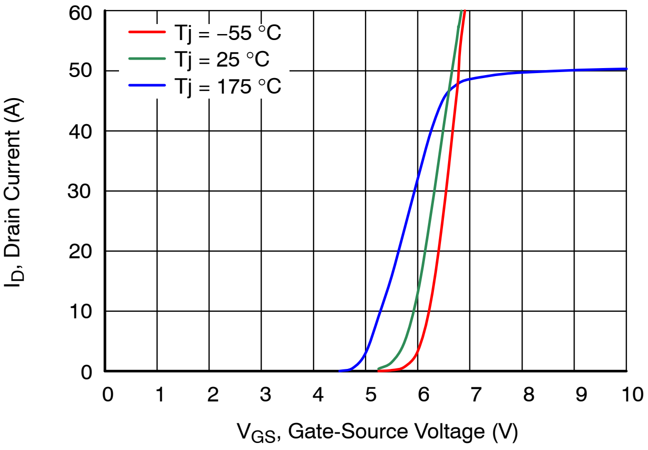


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5$ V

TYPICAL PERFORMANCE DIAGRAMS (continued)

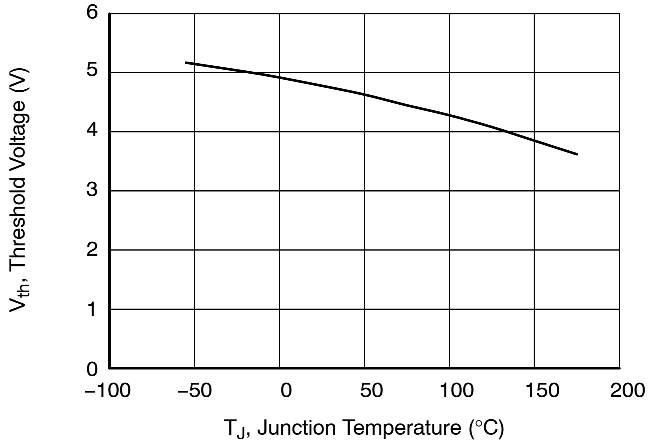


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

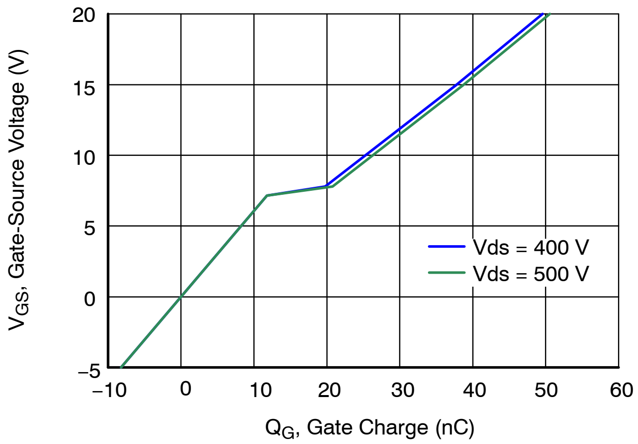


Figure 8. Typical Gate Charge at I_D = 30 A

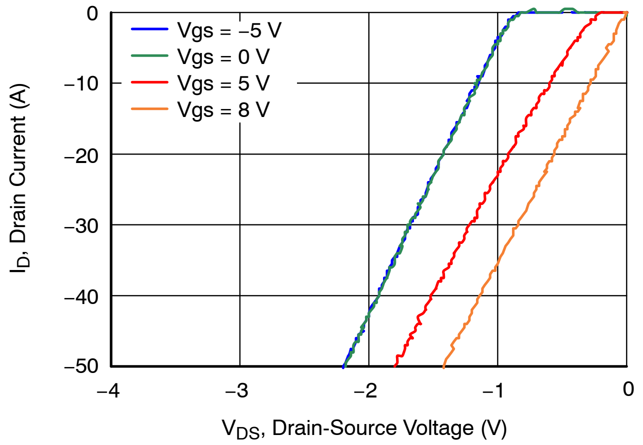


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

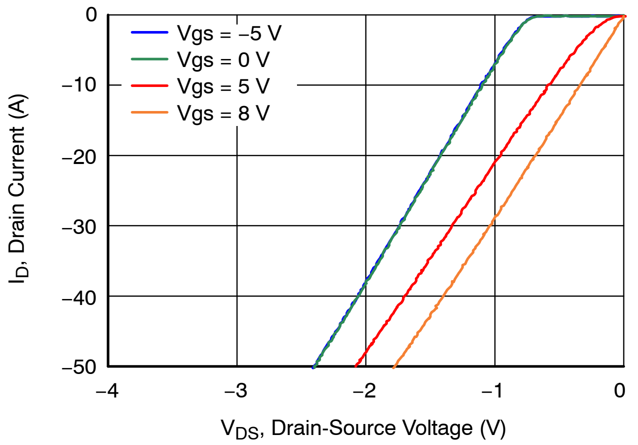


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

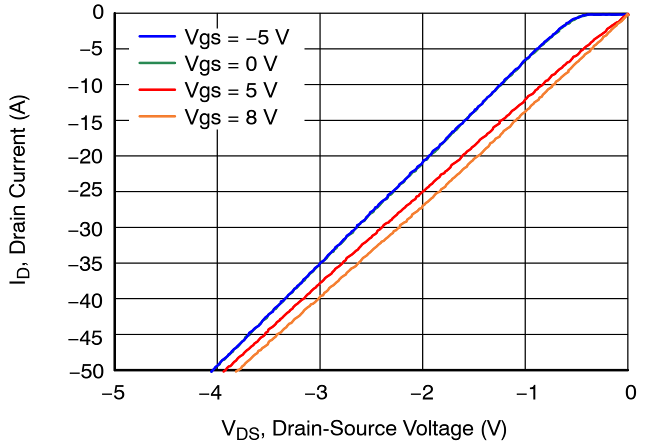


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

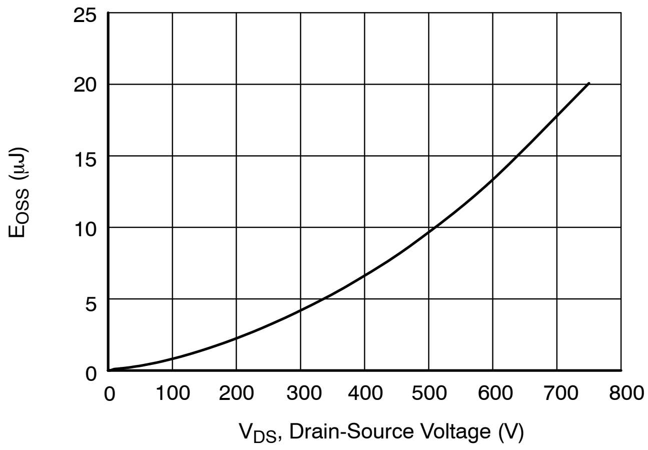


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

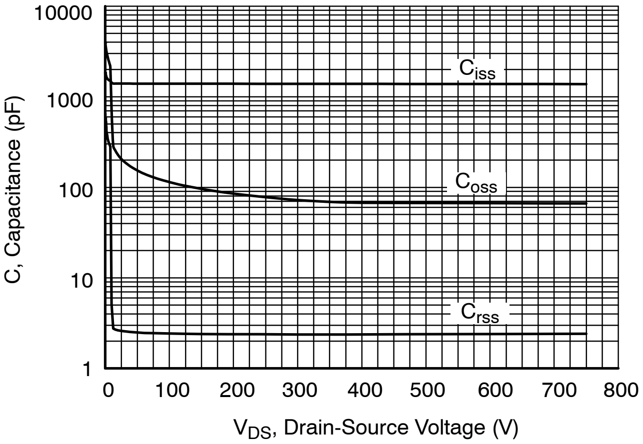


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

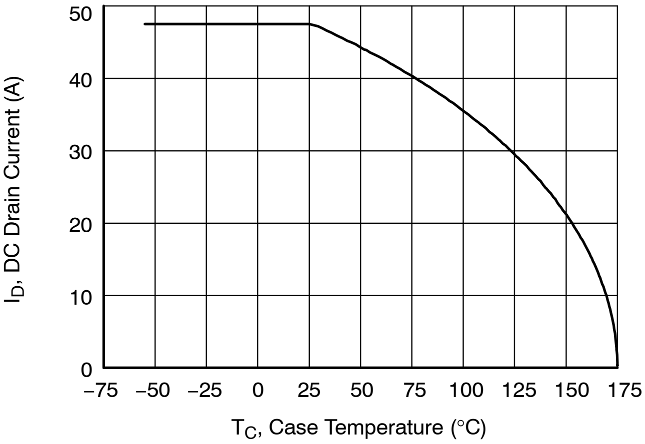


Figure 14. DC Drain Current Derating

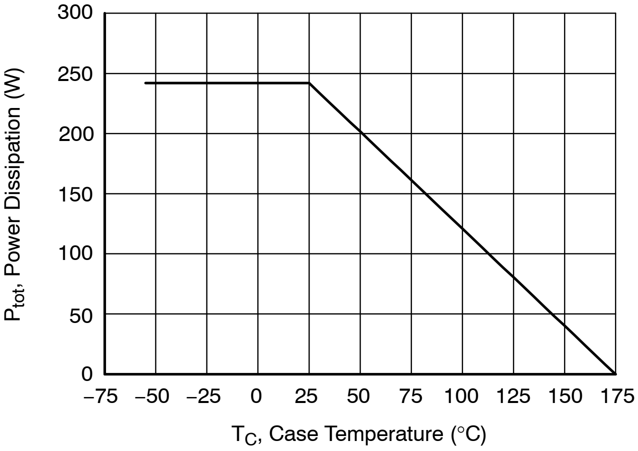


Figure 15. Total Power Dissipation

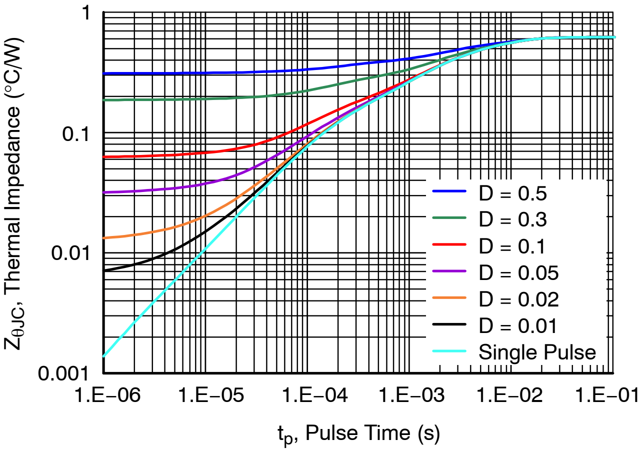


Figure 16. Maximum Transient Thermal Impedance

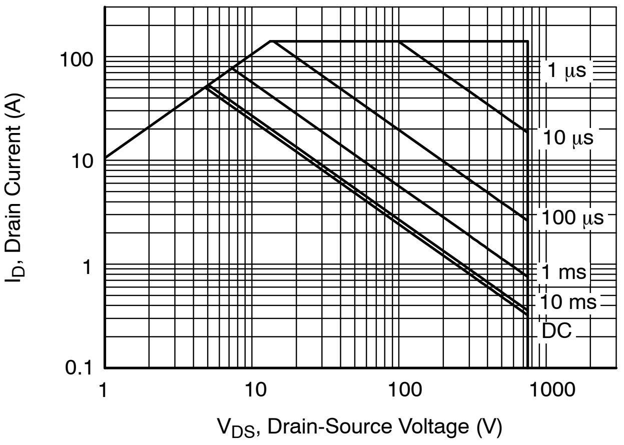


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

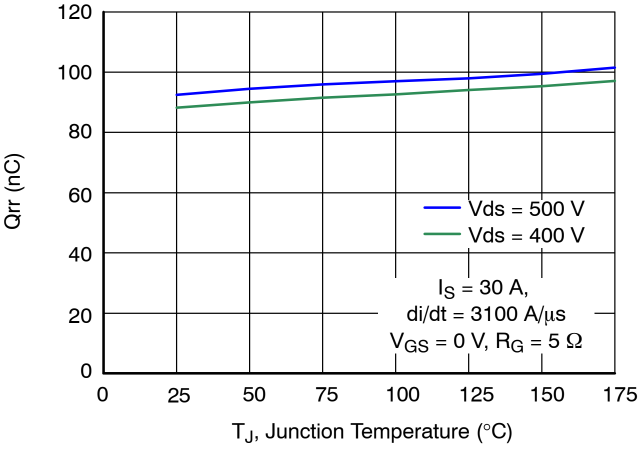


Figure 18. Reverse Recovery Charge Qrr vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS (continued)

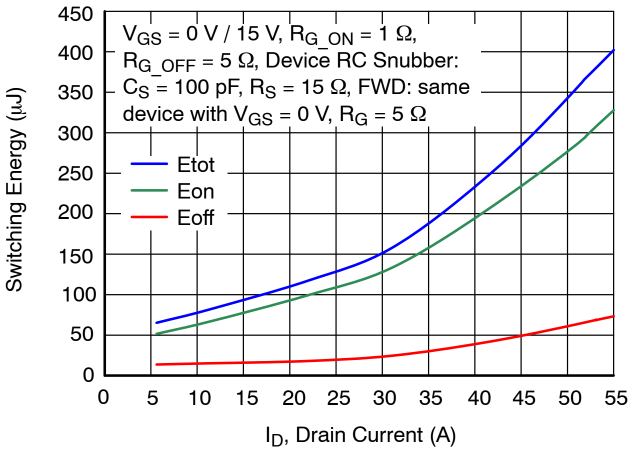


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

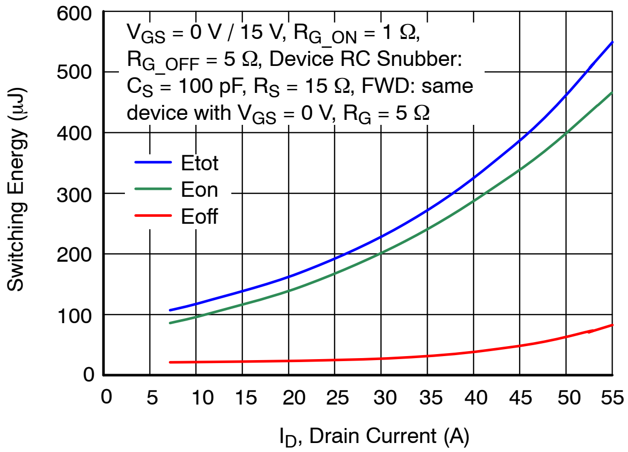


Figure 20. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 500 V and T_J = 25 °C

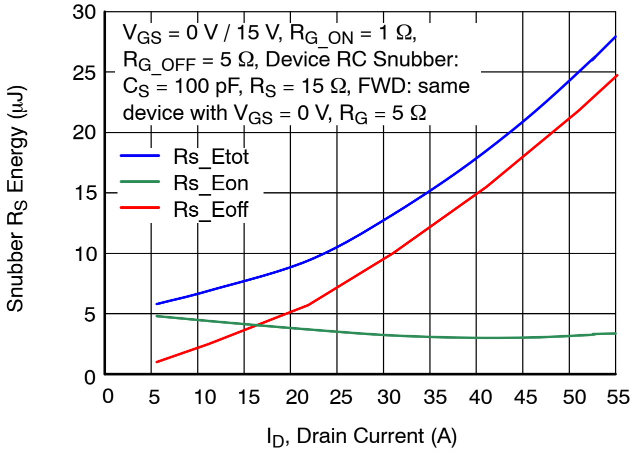


Figure 21. RC Snubber Energy Loss vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

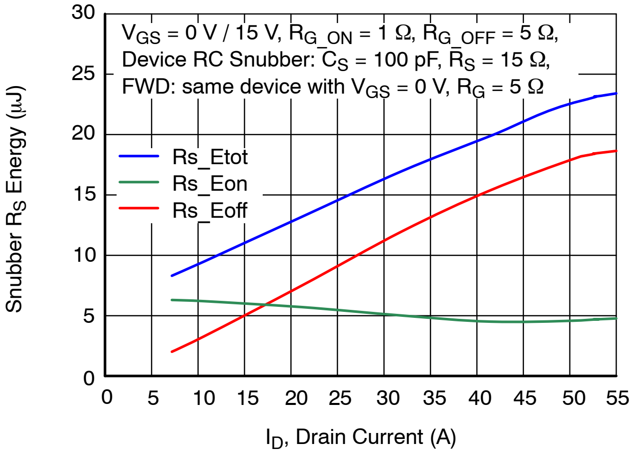


Figure 22. RC Snubber Energy Losses vs. Drain Current at V_{DS} = 500 V and T_J = 25 °C

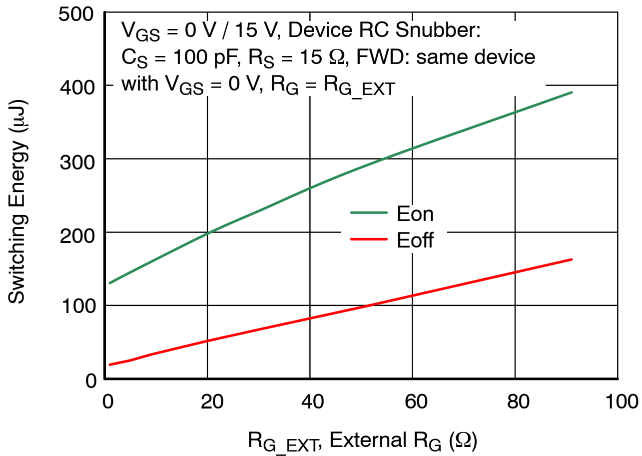


Figure 23. Clamped Inductive Switching Energies vs. $R_{G, EXT}$ at V_{DS} = 400 V, I_D = 30 A, and T_J = 25 °C

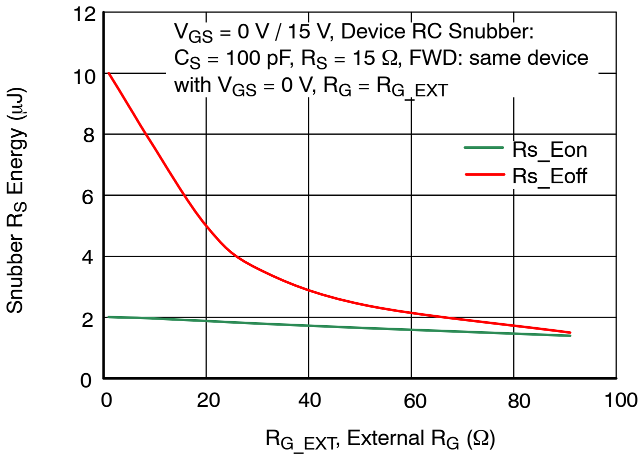


Figure 24. RC Snubber Energy Losses vs. $R_{G, EXT}$ at V_{DS} = 400 V, I_D = 30 A, and T_J = 25 °C

TYPICAL PERFORMANCE DIAGRAMS (continued)

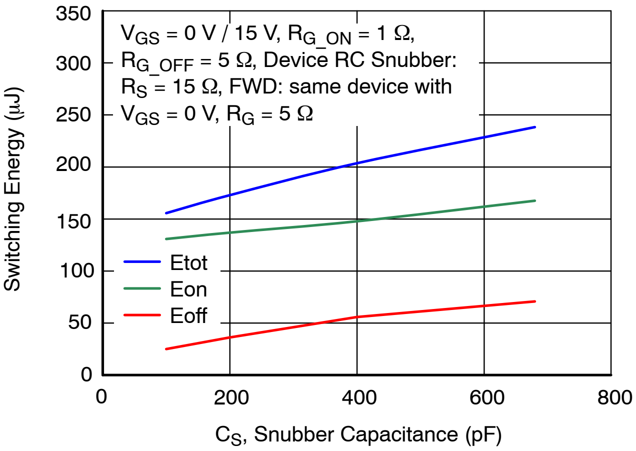


Figure 25. Clamped Inductive Switching Energies vs. Snubber Capacitance C_S at V_{DS} = 400 V, I_D = 30 A, and T_J = 25 °C

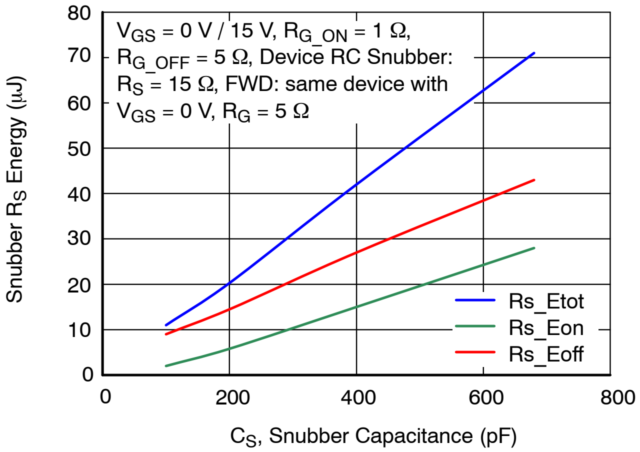


Figure 26. RC Snubber Energy Losses vs. Snubber Capacitance C_S at V_{DS} = 400 V, I_D = 30 A, and T_J = 25 °C

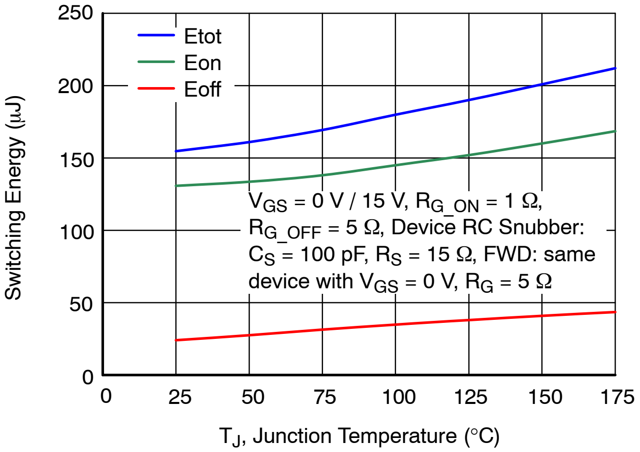


Figure 27. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 30 A

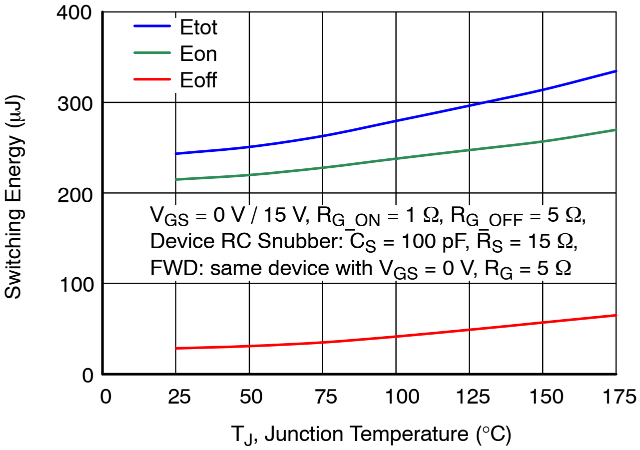


Figure 28. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 500 V and I_D = 30 A

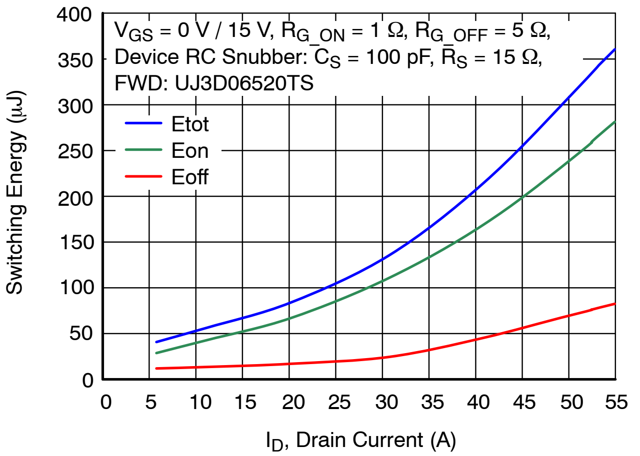


Figure 29. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

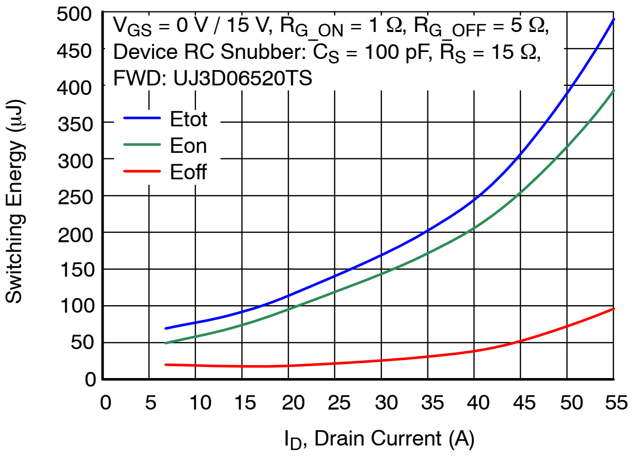


Figure 30. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 500 V and T_J = 25 °C

TYPICAL PERFORMANCE DIAGRAMS (continued)

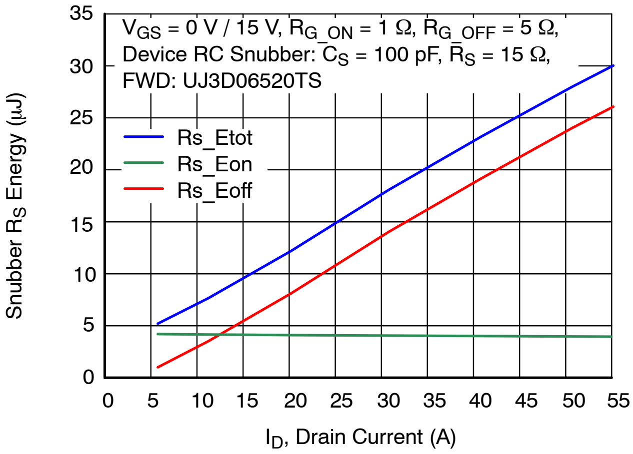


Figure 31. RC Snubber Energy Losses vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

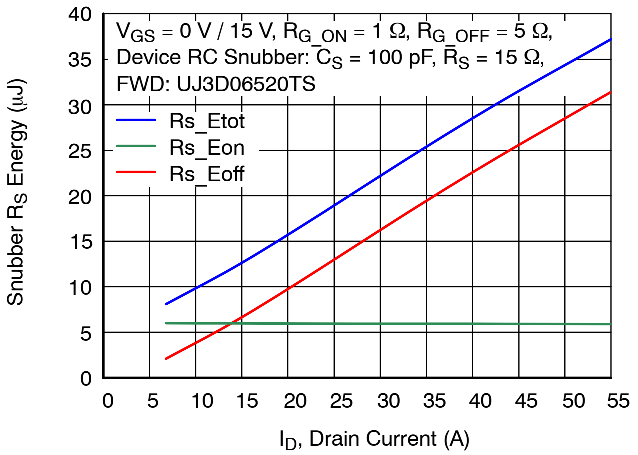


Figure 32. RC Snubber Energy Losses vs. Drain Current at V_{DS} = 500 V and T_J = 25 °C

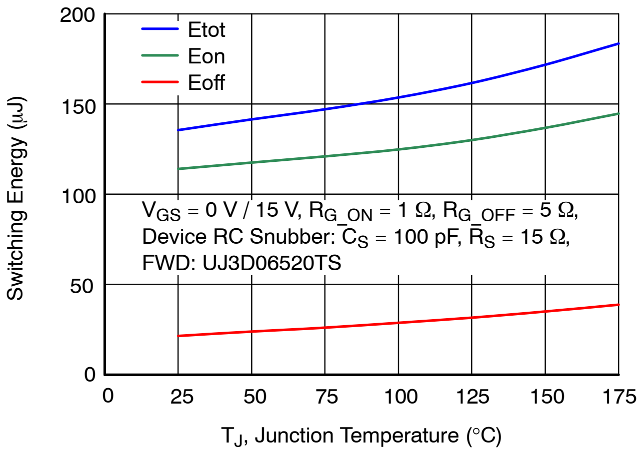


Figure 33. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 30 A

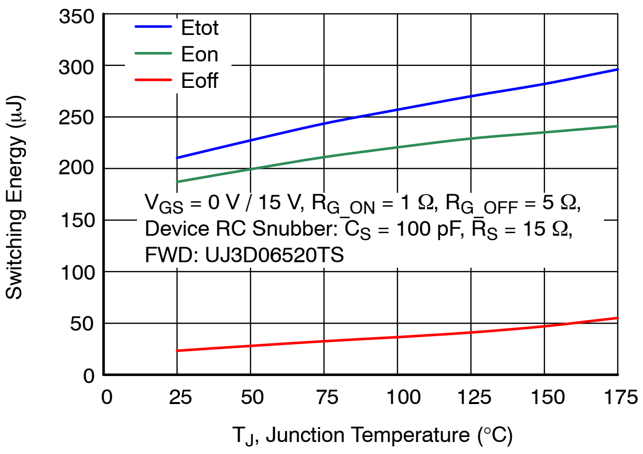


Figure 34. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 500 V and I_D = 30 A

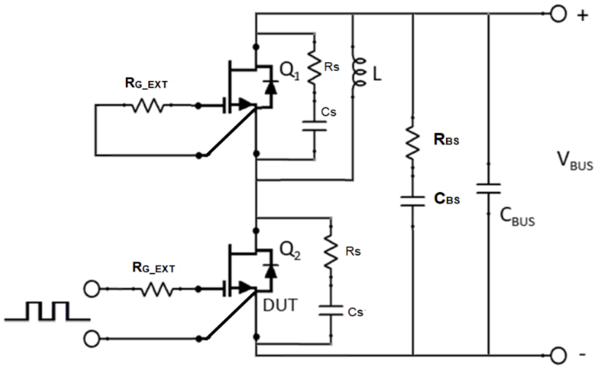


Figure 35. Schematic of the Half−bridge Mode Switching Test Circuit. Note, a Bus RC Snubber (R_{BS} = 2.5 Ω, C_{BS} = 100nF) is Used to Reduce the Power Loop High Frequency Oscillations

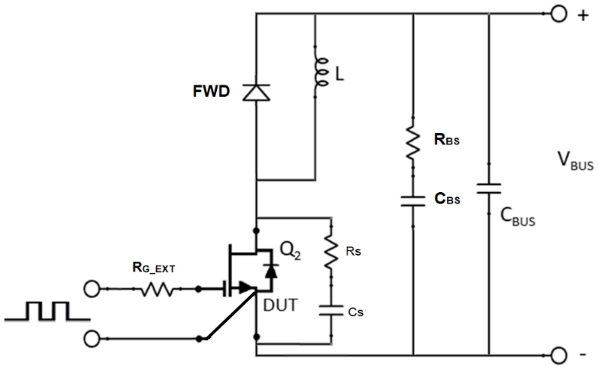


Figure 36. Schematic of the Chopper Mode Switching Test Circuit. Note, a Bus RC Snubber (R_{BS} = 2.5 Ω, C_{BS} = 100 nF) is Used to Reduce the Power Loop High Frequency Oscillations

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

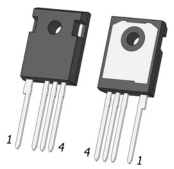
A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com

ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ4C075033K4S	UJ4C075033K4S	TO247-4	600 Units / Tube

REVISION HISTORY

Revision	Description of Changes	Date
C	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products.	3/21/2025
3	Converted the Data Sheet to **onsemi** format.	6/26/2025



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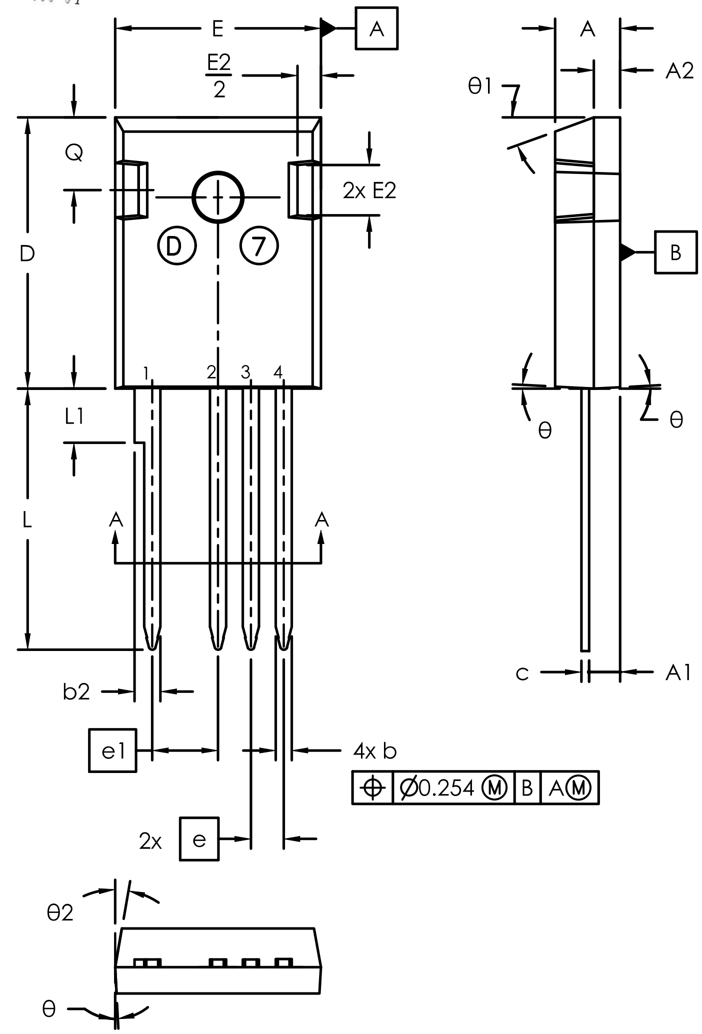

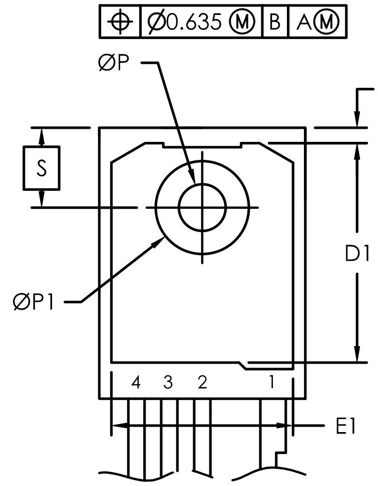

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	–	–
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	–	–
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	–	–	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

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ISSUE E

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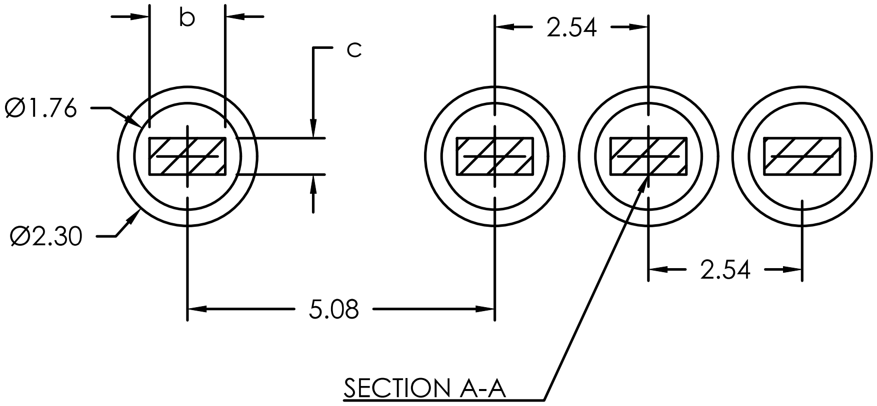
RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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