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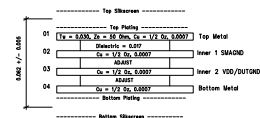
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07/09/2010

NOTES: (Unless Otherwise Specified)

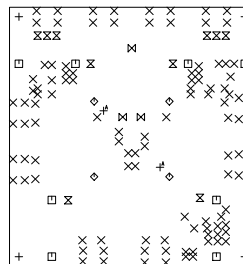
1. Latest revisions shall apply to all specifications.
2. Fabricate PCB in accordance with IPC-A-600; using supplied CAD Data. Board data viewed from primary side (layer 1). Board shall meet the requirements of UL796 with a flammability rating of 94V-0. Vendors UL logo or designation, date code, and UL rating shall be located in etch on the secondary side of the board. If space is limited, it is permissible to locate markings on secondary legend.
3. Materials: 170 TG FR4 or better, RoHS compliant.
Refer to layer stack-up for copper weight and dielectric thickness.
4. Impedance: Refer to layer stack-up.
5. Finish - .00005" of Hard Gold over .0002" Nickel
6. Soldermask: NONE
7. Legend (silkscreen): No legend allowed on exposed lands.
Color - White, permanent, organic, non-conductive epoxy ink.
8. Electrical Test - 100% electrical test required and verified to IPC-356 netlist provided. Not applicable for double sided boards.
9. Warp and twist shall not exceed 10X (.010" per linear inch).
10. Tolerances:
Finished Plated through hole tolerance is +/- .003".
Non-plated through hole tolerance is +/- .001".
Board profile +/- .010".
11. Conductor widths shall be within +/- .001 of supplied artwork (except for impedance signals).
12. Remove all burrs and sharp edges > .015".
13. CAM to remove ODD Aperatures

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



Special Instructions:

Impedance Tolerance: +/- 5X. (When defined in above stacking.)
EBTech designs impedance line widths with approximately .0015" etch tolerance included. Fabrication shop to modify line width to meet impedance specification. Fabrication shop shall not modify dielectric thickness defined on the layer stack-up without EBTech approval.
Fabrication shop to use areas noted on the layer stack-up as "Adjust" at shop option, to meet overall thickness specification.



SIZE	QTY	SYM	PLATED	TOL
12	108	X	YES	Per_default_and_notes
35	10	X	YES	Per_default_and_notes
35.43	3	X	YES	Per_default_and_notes
71	8	X	YES	Per_default_and_notes
62	2	X	NO	Per_default_and_notes
89	4	X	NO	Per_default_and_notes
125	4	X	NO	Per_default_and_notes

EBTech		BOARD NAME		DESIGNER	ENGINEER
EVALUATION BOARD TECHNOLOGIES, INC.		N03N03005 EVAL BOARD		T.J.K.	V.R.
3220 N. Central Ex. Hwy 250		PART NUMBER		REV	DATE
DANMOR, AZ 85025 USA		EBT1763-01		A	07/09/2010
CITY DESCRIPTION		GENERAL			
FABRICATION DRAWING		E1763JAFAB.PHO			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE INCHES. TOLERANCES ARE: FRACTIONS DECIMALS +/- .X +/- 0.1 +/- .XX +/- 0.01 DO NOT SCALE DRAWING		APPROVALS		DATE	EBTech	
TREATMENT		CHECKED			TITLE FABRICATION DRAWING	
FINISH		APPROVED			SIZE C	
SIMILAR TO		MARKING SYMBOL		ISSUED	DWG NO. EBT1763-01	
					REV A	
					SHEET 1 of 1	