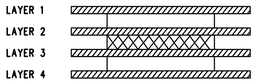
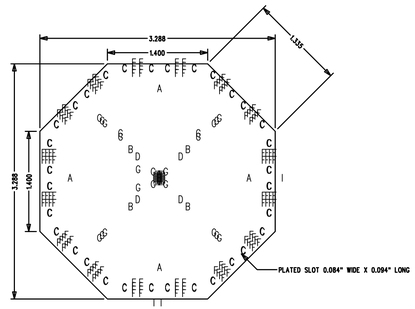
REV: E

NOTES:

1) FINISHED TRACE WIDTHS ARE SPECIFIED ON STACKING.
   TRACES MUST BE THIS TRACE WIDTH +/-0.000
2) BOARD OUTLINE ROUTING MUST BE TOLERANCE +/-0.005
3) SILKSCREEN ON TOP (ROGERS SIDE OF THE BOARD) MUST BE BLACK
4) SILKSCREEN ON BOTTOM (FR4 SIDE OF THE BOARD) MUST BE WHITE
5) NO SOLDERMASK REQUIRED ON TOP METAL

LAMINATION SPECIFICATIONS





EVERETT CHARLES TECHNOLOGIES SEMICONDUCTOR TEST GROUP 2909 SOUTH FAIRE DRIVE TEMPE, AZ 85282 U.S.A. INTAT 602-438-1112	PART NUMBER 1M00AB2C21835	REV E
	LAYER DESCRIPTION	SIZE B 21835
DESIGNER L.TRUEMAN	ENGINEER S.TRUEMAN	
VIEWED FROM TOP (LAYER 1) COPYRIGHT ECT 09/04	FABRICATION DRAWING	

Ver 1

	TOLERANCE	DRILLED	NOTES