MT9M114EBLSTCZH3-GEVB

MT9M114 Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
  - Default – 24 MHz Crystal Oscillator
  - Optional Demo3 Controlled MClk
- Two-wire Serial Interface
- Parallel Interface
- HiSPi (High Speed Serial Pixel) Interface
- ROHS Compliant

Figure 1. MT9M114 Evaluation Board

Block Diagram

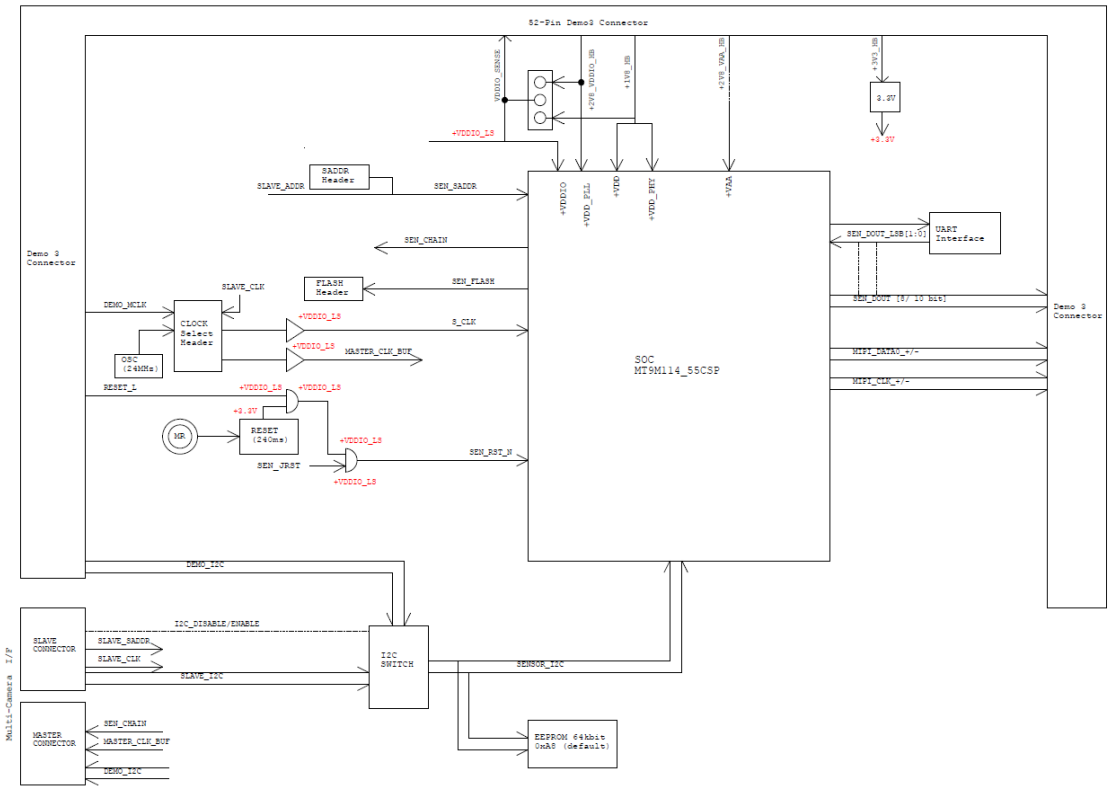

Figure 2. Block Diagram of MT9M114 Evaluation Board

Top View

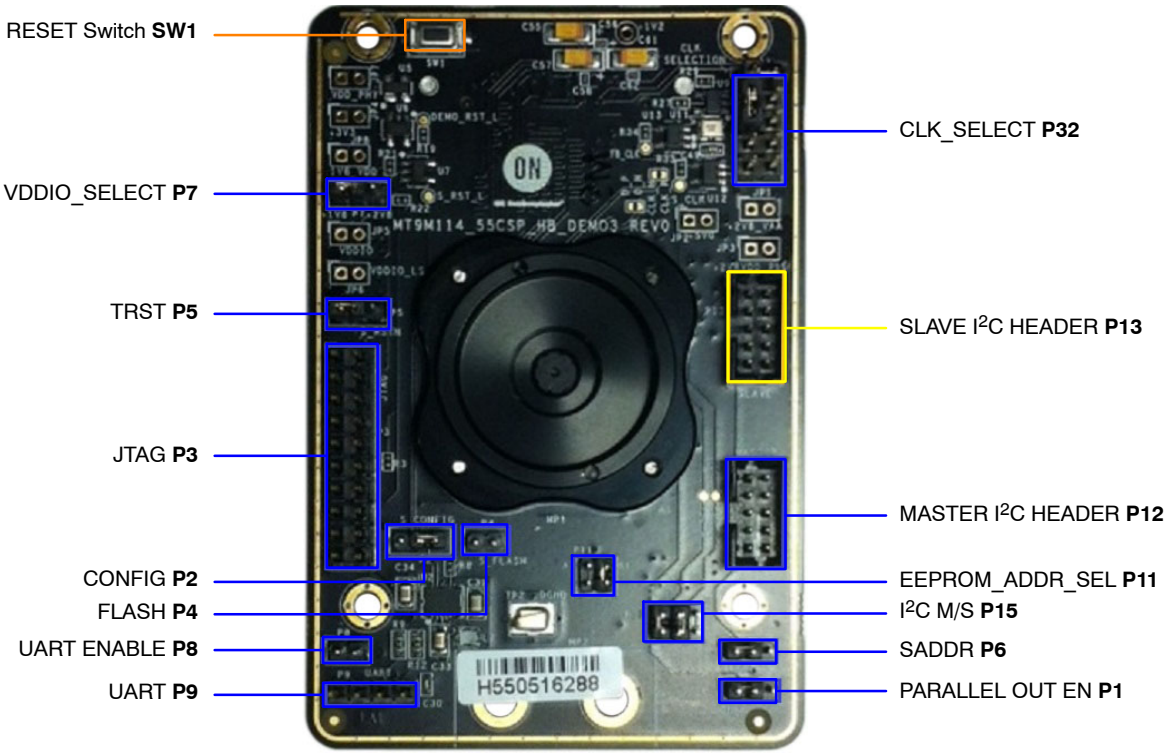

Figure 3. Top View of the Board − Default Jumpers

Bottom View

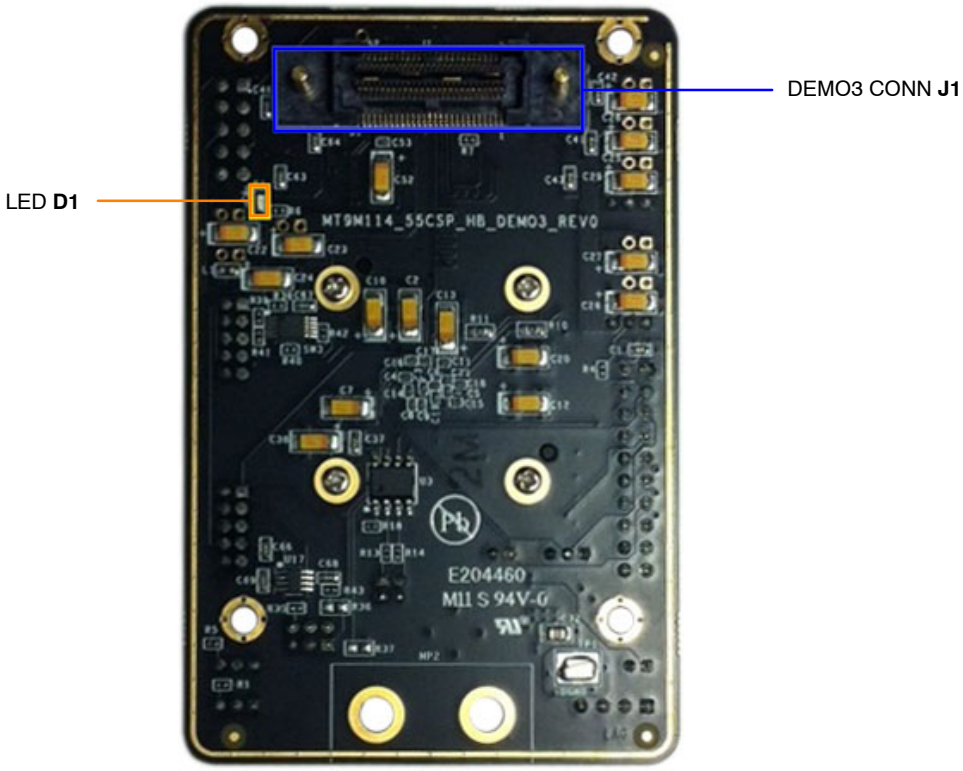

Figure 4. Bottom View of the Board − Connector

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added. The ‘L’ shape denotes pin 1.

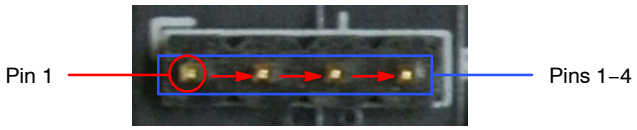

Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right (Except for P11)

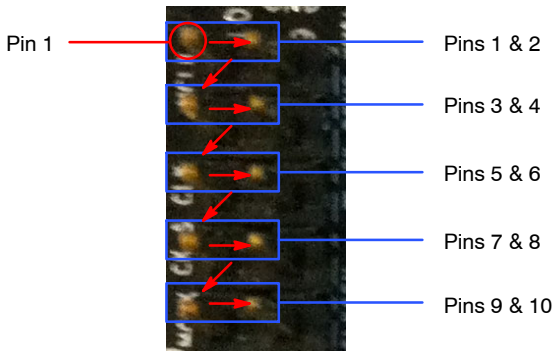

Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture (P11 and P15 has different orientation

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P1	OE_L	1−2 (Default)	Enable Parallel Interface
		2−3	Enable MIPI Interface
P2	CONFIG	2−3 (Default)	Set to Normal Mode
		1−2	Suspend State
P3	JTAG Probe	3 (SEN_TRSTN)	JTAG_TRSTN
		5 (SEN_CONFIG)	JTAG_TDI
		7 (SEN_CHAIN)	JTAG_SMS
		9 (SEN_TCK)	JTAG_TCK
		13 (SEN_FLASH)	JTAG_TDO
		15 (SEN_JRST)	JTAG_RST
P4	FLASH	1−2	For Connection to External Flash
P5	TRST	1−2 (Default)	Set to Normal Mode
		2−3	Set to Test Mode
P6	SADDR	1−2 (Default)	Slave Address: 0x90
		2−3	Slave Address: 0xBA
		Open	Multi-camera Slave Mode
P7	+VDDIO	1−2 (Default)	1.8 V Operation of Sensor
		2−3	2.8 V Operation of Sensor

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P8	UART	Open (Default)	UART Shutdown (Tristate)
		Close	UART Active
P9	UART Connector	1	GND
		2	UART_TX
		3	UART_RX
		4	VCC
P11	EEPROM	1−2 (Default)	Active Low (A1)
		3−4 (Default)	Active High (A2)
P12	Master connector (Multi−camera)	1	SEN_CHAIN
		3	MASTER_SCK
		5	MASTER _SDAT
		9	CLK_MCLK_BUF
P13	Slave connector (Multi−camera)	1	SEN_SADDR
		3	SLAVE_SCL
		5	SLAVE_SDA
		7	M_I2C_DISABLE
		9	CK_S_CLK
P15	I^2C connector	1−2 & 3−4 (Default)	Master and Sensor I^2C Connected
P32	CLOCK SELECTION	3−5 & 1−2 (Default)	Multi-camera, Master Mode; On-board Oscillator
		7−5 & 9−10	Multi-camera, Master Mode; DEMO3 Clock
		6−5 & 4−2	Multi-camera, Slave Mode; Clock from Master Sensor Unit
		3−5	Single Camera; On-board Oscillator
		5−7	Single Camera; External Clock from Demo3
		5−6	Single Camera; External Clock from Demo3

Interfacing to ON Semiconductor Demo3 Baseboard

The ON Semiconductor Demo3 headboard has a similar 52-pin connector which mates P5 of the Demo3 baseboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

Shorted Jumpers for Power Measurement

Different supplies to the evaluation board are provided by trace shorted jumper, for any voltage and power measurements. To conduct current measurement on a given power rail, cut the trace between the two pins of their respective JP, and insert an ammeter prior to powering up the system. The figure below shows where the trace to cut is located.

Table 2. SHORTENED JUMPERS FOR POWER MEASUREMENT

Jumper	Voltage
JP1 (VAA)	2.8 V
JP2 (From Demo3)	5.0 V
JP3 (VDD−PLL)	2.8 V
JP4 (Peripheral 3.3V)	3.3 V
JP5 (VDDIO)	1.8/2.8 V
JP6 (VDDIO_LS)	1.8/2.8 V
JP7 (VDD−PHY)	1.8 V
JP8 (VDD)	1.8 V

Figure 7. Top and Bottom View of Shorted Jumper. The Bottom View Shows the Trace Location to Cut for Current Measurement

ADDITIONAL INFORMATION

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