EVBUM2565/D

RSL10 SIP Evaluation and Development Board User's Manual

ON Semiconductor®

www.onsemi.com

EVAL BOARD USER'S MANUAL

INTRODUCTION

Purpose

This manual provides detailed information about the configuration and use of the RSL10 SIP Evaluation and Development Board (RSL10−SIP−001GEVB). The Evaluation and Development Board is designed to be used with the software development tools to evaluate the performance and capabilities of the RSL10 SIP radio.

Manual Organization

The *Evaluation and Development Board Manual* contains the following chapters and appendices:

- **Chapter 1: Introduction** describes the purpose of this manual, describes the target reader, explains how the book is organized, and provides a list of suggested reading for more information.
- **Chapter 2: Overview** provides an overview of the Evaluation and Development Board described in this manual.
- **Chapter 3: Evaluation and Development Board** provides the details of the Evaluation and Development Board. The chapter is divided into the following topics:
  - Development Board Setup
  - Development Board Design
  - Power Supply
  - Level Translators
  - LED Circuitry
  - RSL10 SIP
  - Measuring the Current Consumption
  - SWJ−DP Debug Port
  - Digital Input/Output (DIO)
  - Power Supply and Test Points
- **Appendix A: Connectors** provides a complete list of the connectors and jumpers on the Evaluation and Development Board.
- **Appendix B: Schematics** contains the schematics for the Evaluation and Development Board.
- **Appendix C: Bill of Materials** contains a list of the parts that are used to manufacture the Evaluation and Development Board.

Further Reading

For more information, refer to the following documents:

- *Getting Started with RSL10*
- *RSL10 Firmware Reference*
- *RSL10 Hardware Reference*
- RSL10 SIP Datasheet

OVERVIEW

Introduction

The RSL10 SIP Evaluation and Development Board is used for evaluating the RSL10 SIP and for application development. The board provides access to all input and output connections via 0.1″ standard headers. The on-board communication interface circuit provides communication to the board from a host PC. The communication interface translates RSL10 SIP SWJ−DP debug port signals to the USB of the host PC. There is also an on-board 4-bit level shifter for debugging; it translates the I/O signal level of the RSL10 SIP to the 3.3 V digital logic level. It is not enabled by default; you enable it when it is needed.

Evaluation and Development Board Features

The Evaluation and Development Board enables developers to evaluate the performance and capabilities of the RSL10 SIP in addition to developing, demonstrating and debugging applications.

Key features of the board include:

- J−Link onboard solution provides a SWJ−DP (serial-wire and/or JTAG) interface that enables you to debug the board via a USB connection with the PC
- Alternate onboard SWJ−DP (serial-wire and/or JTAG) interface for Arm® Cortex®−M3 processor debugging
- Access to all RSL10 SIP peripherals via standard 0.1″ headers
- Onboard 4-bit level translator to translate the LPDSP32 debug interface at low voltage to a 3.3 V JTAG debugger
- Integrated antenna (included as part of the RSL10 SIP)
- Compliance with the Arduino form factor

EVALUATION AND DEVELOPMENT BOARD

Evaluation and Development Board Setup

This section is an overview of how to configure the Evaluation and Development Board. Details of the development board configuration are discussed later in this manual.

Figure 1 represents an overview of the board setup.

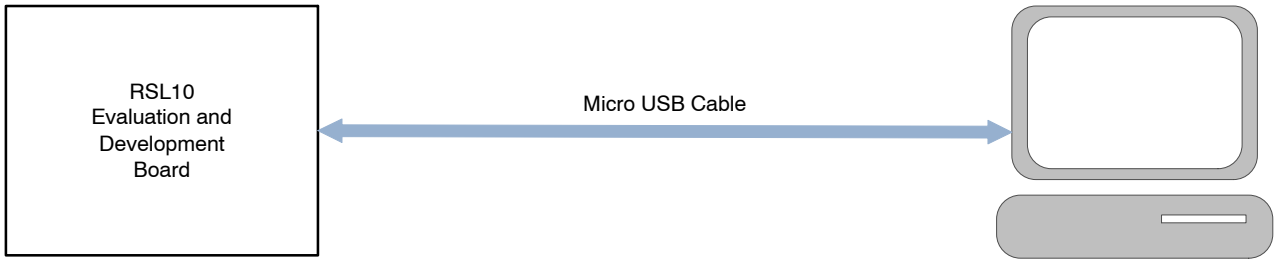

Figure 1. Evaluation and Development Board Setup

If you want to use an external J−Link debugger instead of the onboard one, connect the debugger to connector P2 on the SiP board, as shown in Figure 2. Notice that for this setup, you also need a power supply.

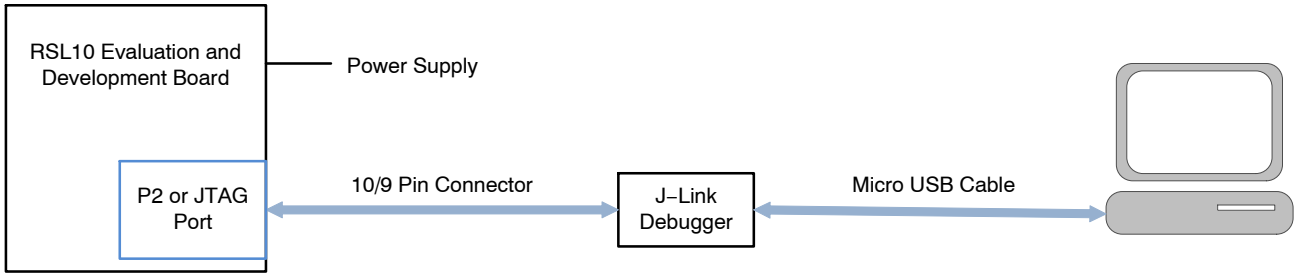

Figure 2. Evaluation and Development Board Setup with External J−Link Debugger

Evaluation and Development Board Design

The following sections detail the various sub-circuits of the RSL10 SIP Evaluation and Development Board. The block diagram in Figure 3 shows the locations of the various circuit sections. Figure 5 and Figure 6 provide 3-dimensional illustrations of the SiP board.

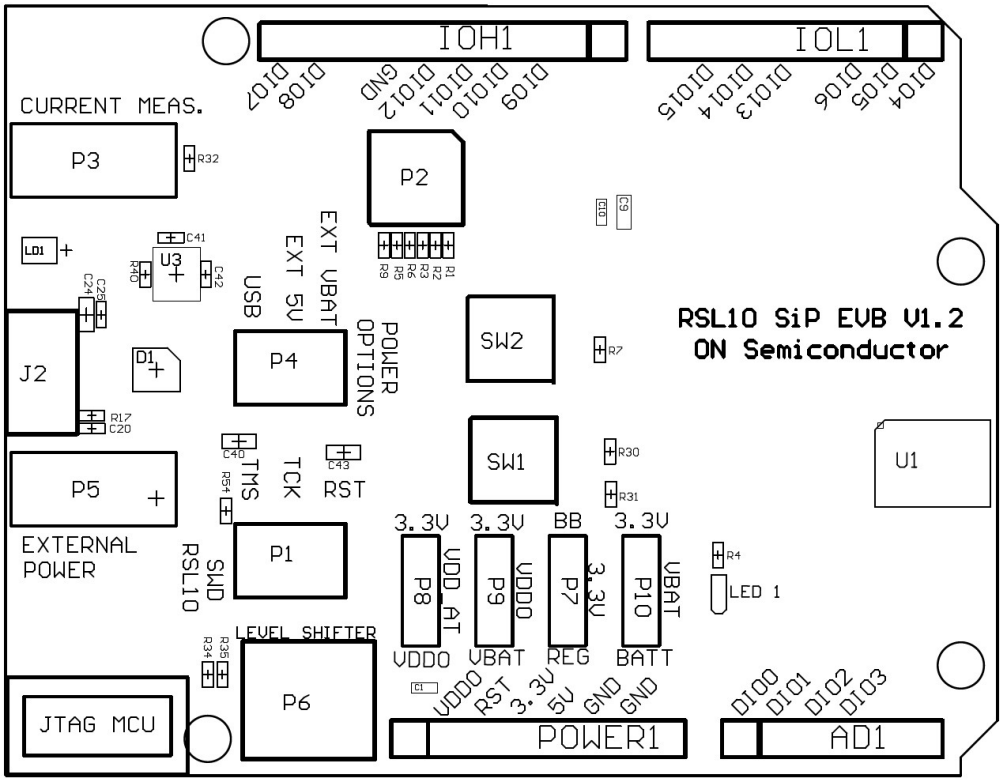

Figure 3. Circuit Location Block Diagram (Top View)

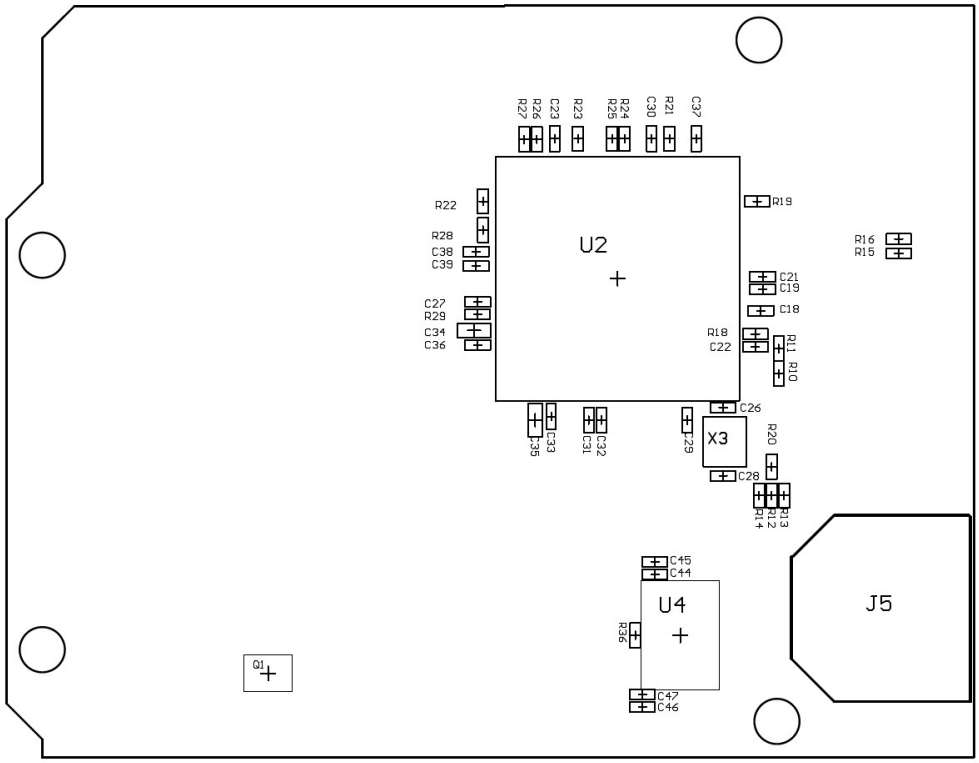

Figure 4. Circuit Location Block Diagram (Bottom View)

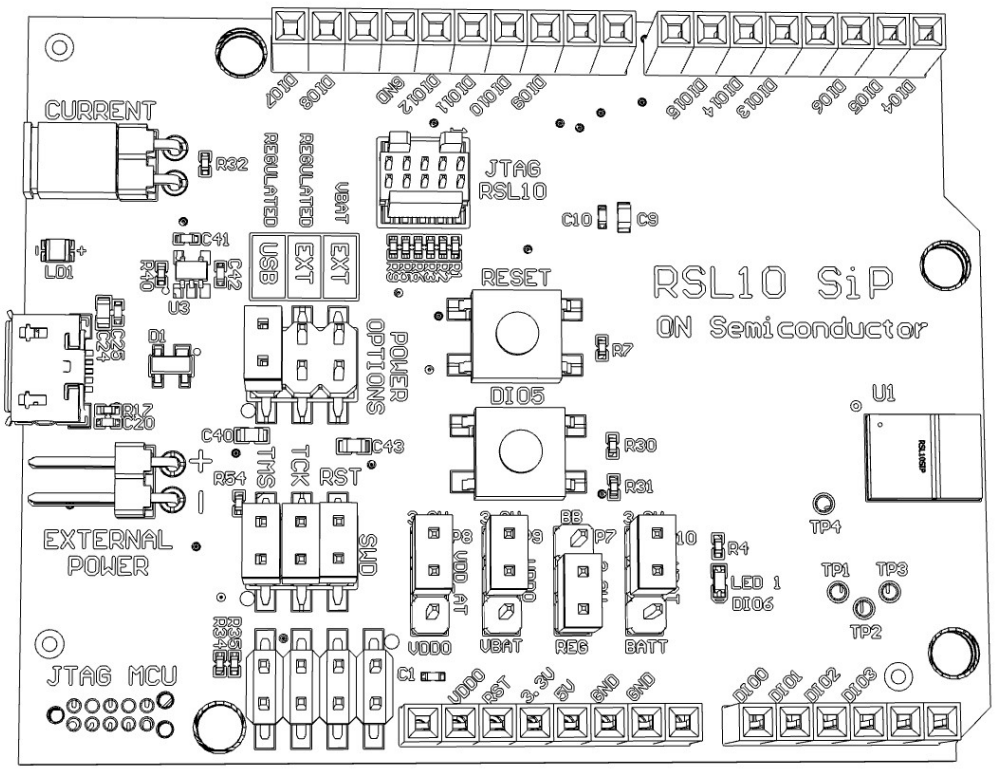

Figure 5. Three-Dimensional Line Drawing of the Board (Top View)

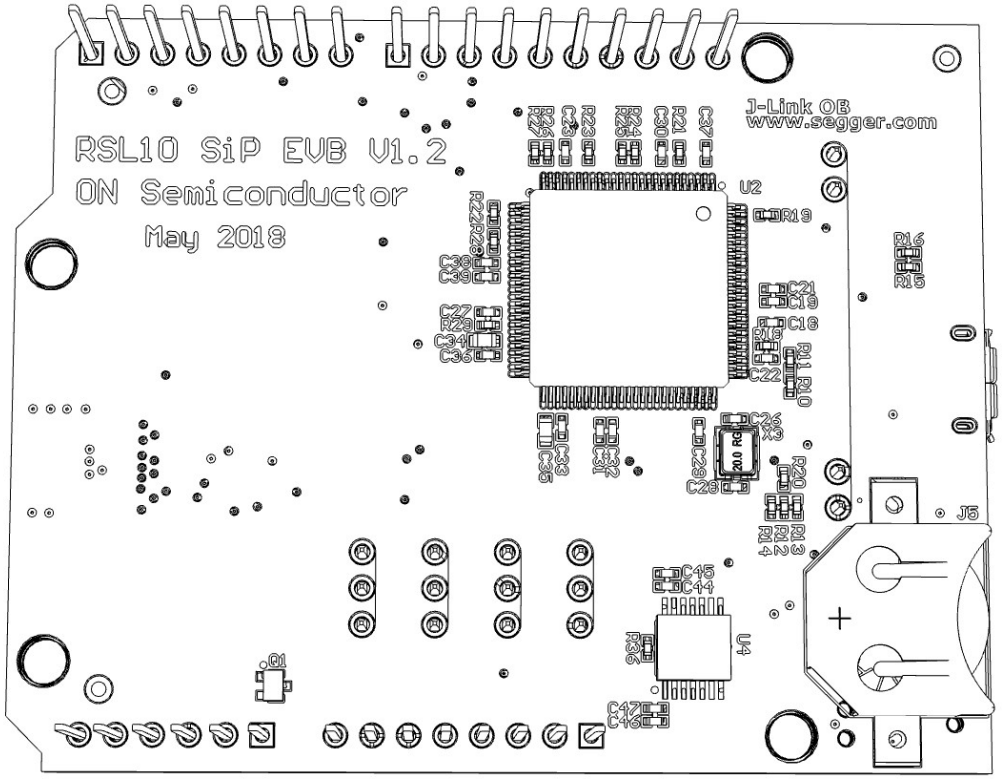

Figure 6. Three-Dimensional Line Drawing of the Board (Bottom View)

Power Supply

The Evaluation and Development Board can be powered by one of the following:

- Micro USB port with regulator
- External power supply connector (P5) with regulator
- External power supply connector (P5) without regulator

Use the jumpers on pin headers P4, P7 and P10 to select a power supply option as show in Table 1.

Table 1. POWER SUPPLY SELECTION

Power Source	Jumper Position on P4	Jumper Position on P7	Jumper Position on P10
Micro USB Port with Regulator	1&2	2&3	1&2
External Power Supply with Regulator	3&4	2&3	1&2
External Power Supply without Regulator	5&6	2&3	2&3

Table 2. MINIMUM/MAXIMUM EXTERNAL REGULATED VOLTAGES

Power Supply	Header	Input Voltage		
		Minimum	Typical	Maximum
RSL10 SIP and J−Link OB MCU	EXT−PSU Regulated	3.3 V	3.6 V	12.0 V
RSL10 SIP and J−Link OB MCU	USB	–	5.0 V	–
RSL10 SIP	EXT−PSU Unregulated	1.1 V	1.25 V	3.6 V

Level Translators

The board has level translators for the DIO signals of the RSL10 SIP, including the clock signal. The level translators facilitate interfacing to external devices that operate at a higher voltage than the RSL10 SIP.

VDDO and 3.3 V are two different power rails. The translator allows a logic signal on the VDDO side to be translated to either a higher or a lower logic signal voltage on the 3.3 V side, and vice-versa.

The level translation circuitry consists of components U4 and the 2x4 header. Signals are translated from the VDDO voltage reference to 3.3 V (default) voltage provided by the regulator output or by an external supply. The VDDO voltage is configured by the pin on header P11 (located on the board edge) to either VBAT_DUT, 3.3 V or other level within the VDDO voltage range, which is 1.1 to 3.3 V.

The NLSX5014 level translators are bi-directional. They have the following features:

- Wide voltage operating range: 0.9 V to 4.5 V
- VDDO and 3.3 V are independent
- VDDO can be equal to, or less than, 3.3 V when connected to the power rail

To enable the level translators, populate positions R34 and R35 with 0 ohms. By default, the level translators are disabled. NOTE: Enabling the level translator affects power consumption.

LED Circuitry

There are two LEDs on the board. One is a dual color LED, called LD1, connected to the J−Link emulator microcontroller unit (MCU). The other is the green LED, connected to DIO 6 of RSL10 SIP. You can use this LED within your applications as an indication LED by programming DIO 6. If DIO 6 is high, this LED is on.

Measuring the Current Consumption

This section deals with measuring current consumption for the Evaluation and Development Board.

Headers are provided for each of the regulated voltages for additional capacitance and/or for measurements. RSL10 SIP has 16 digital I/Os. The VDDO pin in header P9 configures the I/O voltages for power domains to VBAT. The VBAT pin in header P10 configures the VBAT source. The power select pin in header P4 configures the power source of the RSL10 SIP. In addition the measurements should be done by connecting an ammeter to current measure header P3 to measure the device power consumption in isolation.

To measure the current consumption of RSL10 SIP only, you need to source the chip using the external power supply without the regulator as shown in Table 2. To remove leakage currents during current measurement, remove the jumpers on header SWD. Removing the jumpers between the MCU and the RSL10 SIP that connect nRESET, SWDIO and SWCLK prevents current leakage from the JTAG interface, avoiding inaccurate current measurements. In addition, DIOs 4, 5 and 6 must be configured to High−Z (disabled) with no pull up in software. DIOs 4 and 5 are directly connected to the Atmel chip and will leak power into it. DIO 6 is directly connected to the transistor driving the LED and can leak power into it.

SWJ−DP DEBUG Port

The J−Link adapters are typically used to communicate with RSL10 SIP using the standard Coresight SWJ−DP debug port in a JTAG/SW communication protocol. The 9-pin 0.05 in Samtec FTSH header (P1), defined by the Arm Cortex−M3 core on the board, connects RSL10 SIP to external adapters compatible with the Arm Cortex−M3 processor's SWJ−DP interface. Alternatively, you can connect the micro USB port on the board to a PC.

DIGITAL Input/Output (DIO)

The RSL10 SIP contains 16 digital I/O (DIO) signals. The DIO voltage domain is VDDO, while the input voltage can be VBAT or external voltage as outlined in Section "Measuring the Current Consumption" on page 5.

The DIO signals on the RSL10 SIP are multiplexed with several interfaces, including:

- One I^2C interface (DIO [7:8])
- Four external inputs to the low-speed analog to digital converters (DIO [0:3])
- One PCM interface
- Two PWM drivers
- Two SPI interfaces (DIO [13:15])
- One UART interface (DIO [4:5])
- Support interfaces that can be used to monitor control of the RF front-end and Bluetooth® baseband controller

For more information about the DIO multiplexed signals, refer to the *RSL10 Hardware Reference*.

The board provides access to any of the DIOs or their multiplexed signals via the Arduino Headers (Power1, AD1, IOL1, and IOH1).

The LED circuit provides visual monitoring of the DIOs; refer to Section "LED Circuitry" on page 5 for further information.

Power Supplies

There are several external power supplies available on your Evaluation and Development Board.

The user can also access signals on various headers on boards, as described throughout this document.

The external power supplies available for QFN boards are:

- VBUS, 5 V from USB connection − available only when USB is plugged in
- V3.3, 3.3 V from LDO − available when regulated supply is selected
- VEXT, (P5 header) unregulated external supply − available when unregulated supply is selected
- Battery (J5 Battery Holder, 12 mm coin cell battery)

APPENDIX A – CONNECTORS

Overview

This appendix lists all connectors on the Evaluation and Development Board. The sections that follow provide descriptions for:

- Jumpers and their possible configurations
- Headers
- Switches and their possible configurations
- Connectors

Configuration Header Jumpers

Table 3. JUMPER DESCRIPTIONS

Designator	Description
P4	Regulated or Unregulated power supply selection
P10	VBAT Power Source selection (3.3 V, Vext or Battery)
P9	VDDO selection (VBAT_DUT, 3.3 V)
P8	VDD_AT selection (3.3 V, VDDO)
P1	Onboard JTAG debugger connection

Headers

Table 4. HEADER DESCRIPTIONS

Designator	Description
POWER1	Arduino Power header 3.3 V, VDDO, nRESET, GND
AD1	Arduino Analog Inputs header A [0:3]
IOL1	Arduino IOL header UART, INT [0:1], SPI2
IOH1	Arduino IOH header I2C, SPI1
P2	External JTAG debug connection header
P3	Current measurement header
P5	External power supply header
P6	Input and output of level shifter

Switches

Table 5. SWITCH DESCRIPTIONS

Designator	Description
SW1	Pushbutton switch to reset RSL10 SIP
SW2	Pushbutton switch for DIO5

Connectors

Table 6. CONNECTOR DESCRIPTIONS

Designator	Description
J1	RF switch connector
J2	Micro USB port for power supply, JTAG and UART emulation
J3	MCU programming connector
J5	Battery Holder (12 mm coin cell)

APPENDIX B – SCHEMATICS

This appendix contains schematics for the Evaluation and Development Board, version 1.3:

- The Top-level (Arduino interface) schematic
- The RSL10 SIP schematic
- The Interface MCU schematic
- The Power Supply schematic

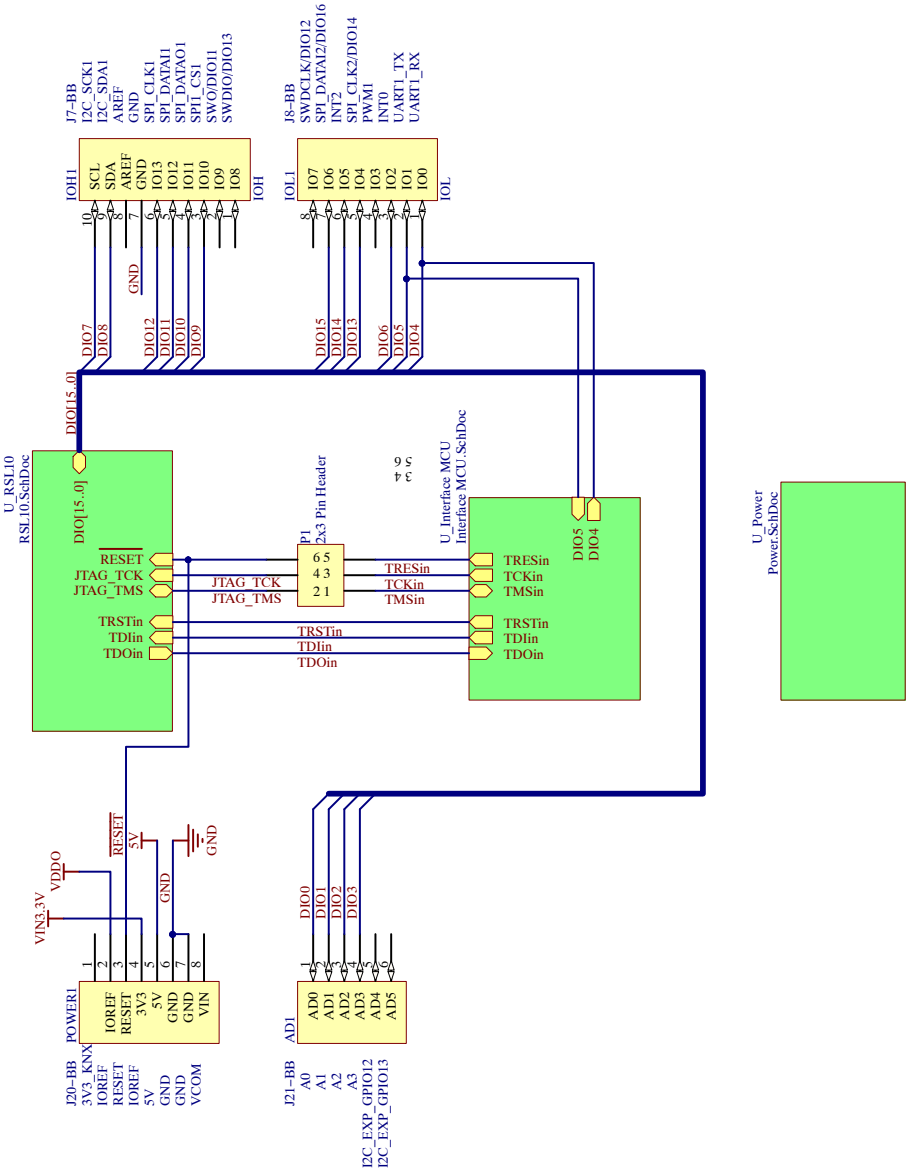

Figure 7. Top-Level (Arduino Interface) Schematic

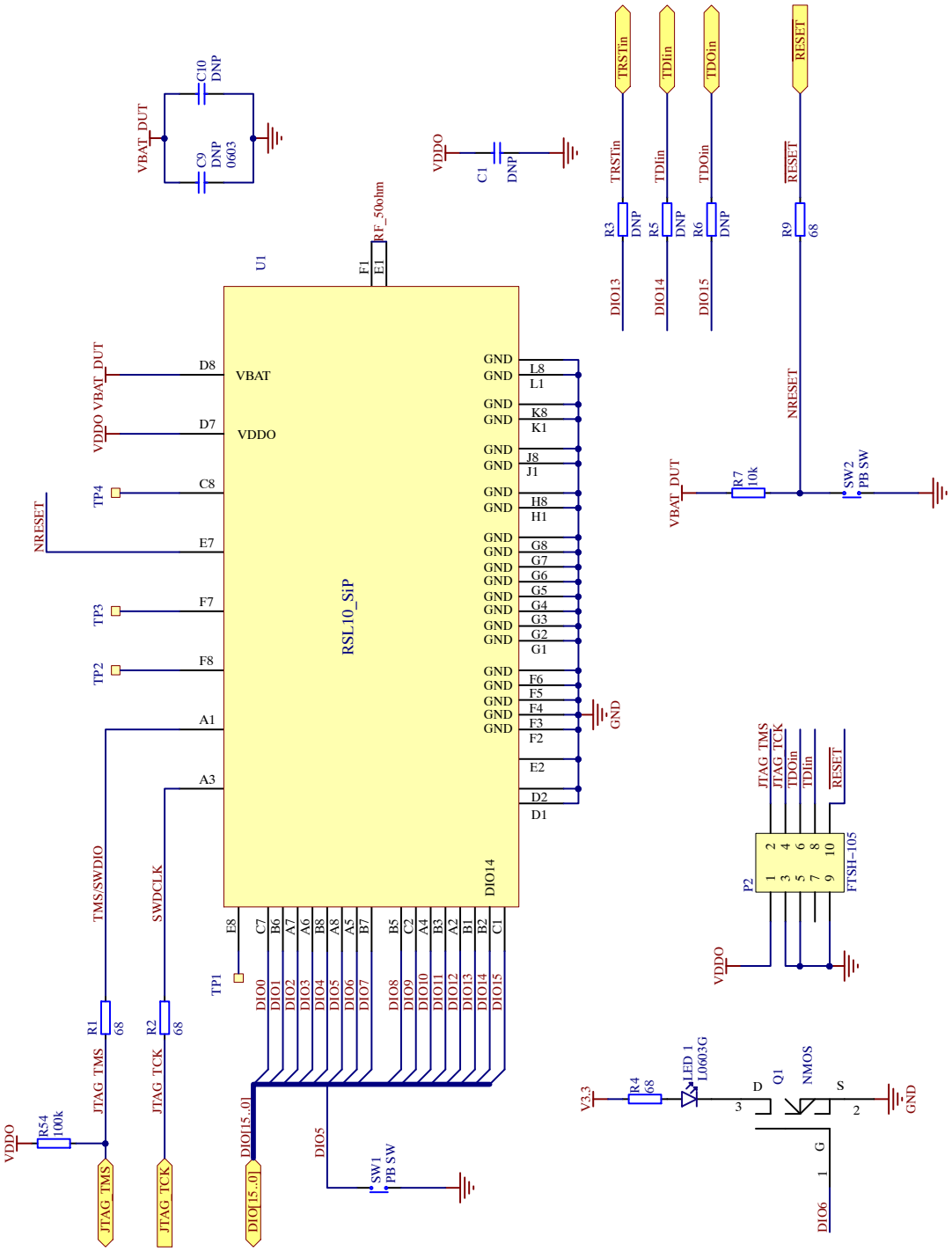

Figure 8. RSL10 SIP Schematic

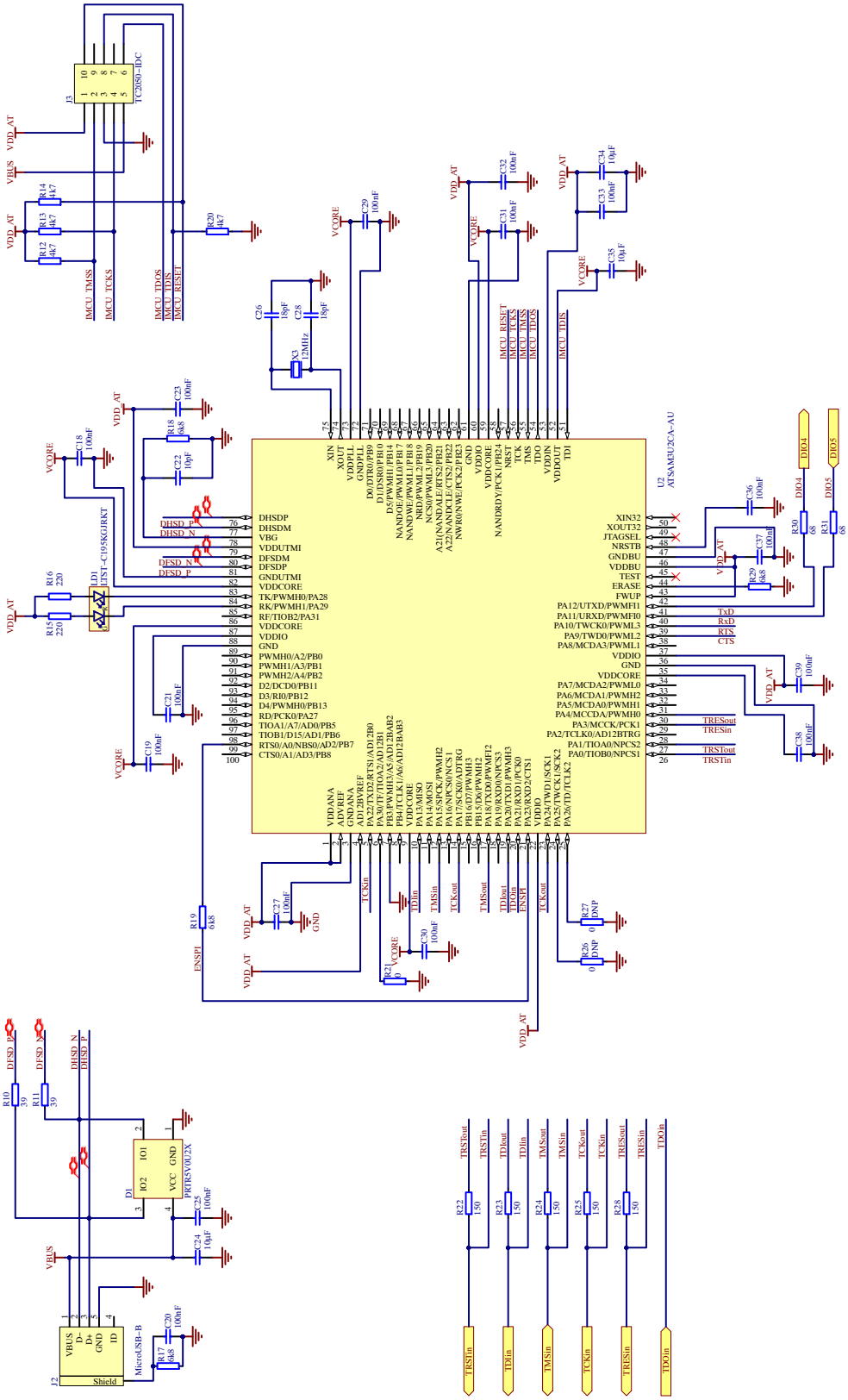

Figure 9. Interface MCU Schematic

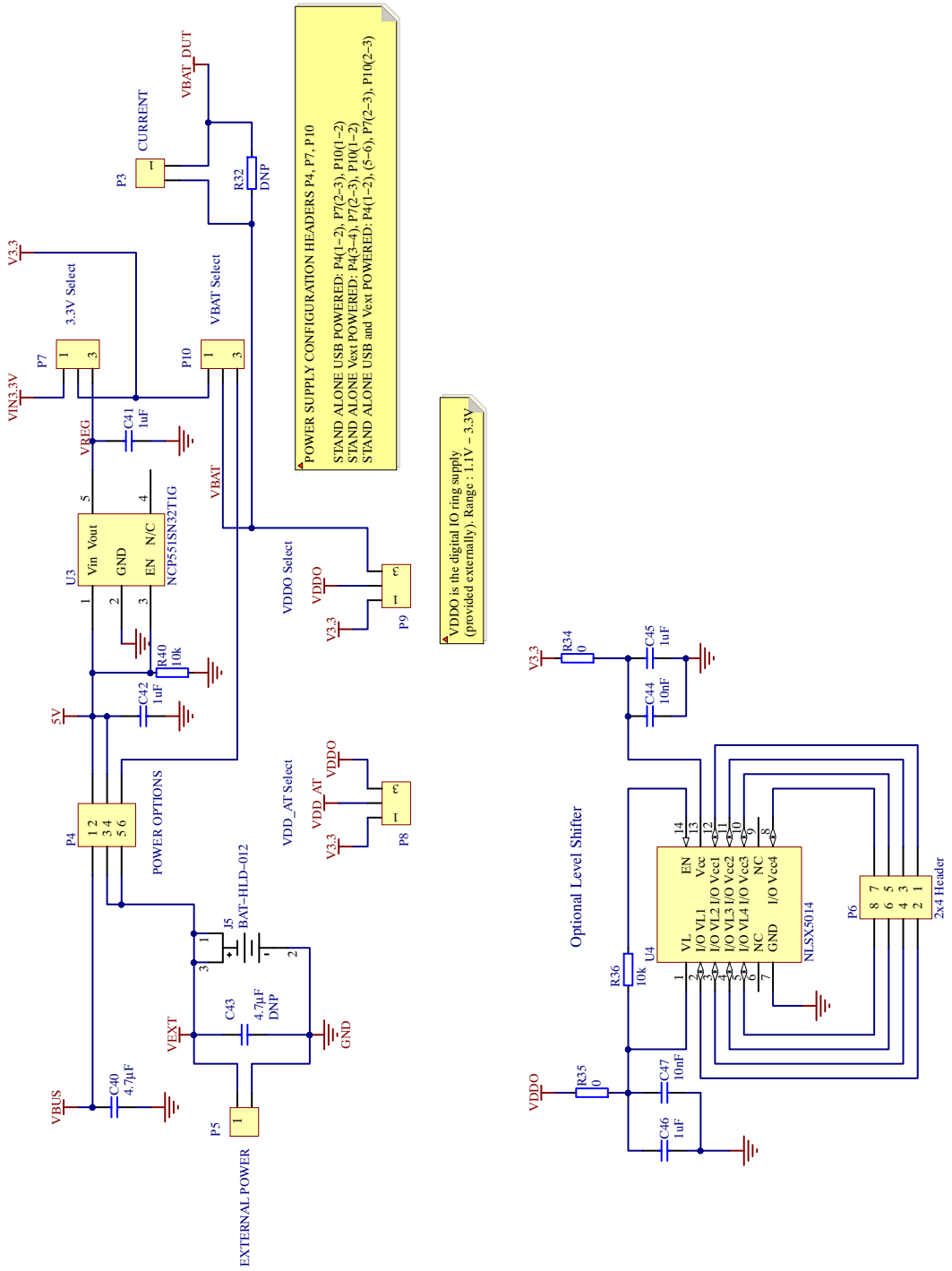

Figure 10. Power Supply Schematic

APPENDIX C – BILL OF MATERIALS

Table 7. BILL OF MATERIALS FOR RSL10 SIP EVALUATION AND DEVELOPMENT BOARD VERSION

Designator	Description	Footprint Doc
AD1	Arduino Stackable Header 6-pin	N/A
C9, C40, C43	CAP CER 4.7 μF 10 V X5R 0603, CAP CER 4.7 μF 25 V X5R 0603	0603
C1, C10, C18, C19, C20, C21, C23, C25, C27, C29, C30, C31, C32, C33, C36, C37, C38, C39	Capacitor, NP0, ±2%	0402
C22	Capacitor, NP0, ±2%	0402
C24, C34, C35	Capacitor, X5R, ±10%	0603
C26, C28	Capacitor, NP0, ±2%	0402
C41, C42, C45, C46	Capacitor, NP0, ±10%	0402
C44, C47	Capacitor, NP0, ±2%	0402
D1	Ultra low capacitance double rail-to-rail ESD protection diode	SOT−143B
IOH1	Arduino Stackable Header 10-pin	
IOL1, POWER1	Arduino Stackable Header 8-Pin	
J2	MicroUSB−B−SMT	FCI_10118193−0001LF
J5	HOLDER BATTERY 12 MM COIN	
LD1	Ultra bright AlInGaP Bi-Color LED	LED_DUAL_0606
LED 1	LED SMARTLED GREEN 570NM 0603	0603
P1, P4	Header 2x3 SMT	
P2	SAMTEC – CONN HEADER 10POS DUAL .05″ SMD KEYING SHROUD	FTSH−105
P3, P5	HEADER, 2POS, 1ROW; Series: 961; Pitch Spacing: 2.54 mm; RA	
P6	2x4 Pin Header	
P7, P8, P9, P10	HEADER, 3POS, 1ROW; Series: 961; Pitch Spacing: 2.54 mm	
Q1	NMOS Transistor	SOT65P210X105−3N
R1, R2, R4, R9, R30, R31	Resistor, ±1%, 0.063 W	0402
R3, R5, R6, R26, R27, R32	Resistor, ±1%, 0.063 W	0402
R7, R36, R40	Resistor, ±1%, 0.1 W	0402
R10, R11	Resistor, ±1%, 0.1 W	0402
R12, R13, R14, R20	Resistor, ±1%, 0.1 W	0402
R15, R16	Resistor, ±1%, 0.1 W	0402
R17, R18, R19, R29	Resistor, ±1%, 0.1 W	0402
R21, R34, R35	Resistor, ±1%, 0.1 W	0402
R22, R23, R24, R25, R28	Resistor, ±1%, 0.1 W	0402
R54	Resistor, ±1%, 0.1 W	0402
SW1, SW2	ALPS – SKHUALE010 – Tactile Switch, SPNO, SMD, 6.5 x 6.2 x 2.5 mm	ALPS_SKHUxxx010_WO_GND
U1	RSL10 SIP	N/A
U2	IC MCU 32 bit 128 kB flash 100LQFP	LQFP−100
U3	IC REG LIN 3.3 V 600MA 5TSOP	TSOP−5IPC

Table 7. BILL OF MATERIALS FOR RSL10 SIP EVALUATION AND DEVELOPMENT BOARD VERSION (continued)

Designator	Description	Footprint Doc
U4	TRANSLATOR LEVEL 4BIT 14−TSSOP	TSOP65P640X120−14N
X3	XTAL SMD 3225, 12 MHz, 18 pF, ±30 ppm	BT−XTAL_3225
See Jumper Location	CONN JUMPER SHORTING GOLD FLASH	CONN JUMPER (2.54 mm) Gold
See Installation	MACHINE SCREW PAN PHILLIPS 4−40	N/A
See Installation	HEX STANDOFF 4−40 NYLON 3/8″	N/A

NOTE: ON Semiconductor reserves the right to substitute materials for equivalent or similar parts.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales