NCP51705SMDGEVB

NCP51705 Mini SMD Evaluation Board User's Manual

NCP51705 SiC Driver SMD Evaluation Board for Existing or New PCB Designs

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EVAL BOARD USER'S MANUAL

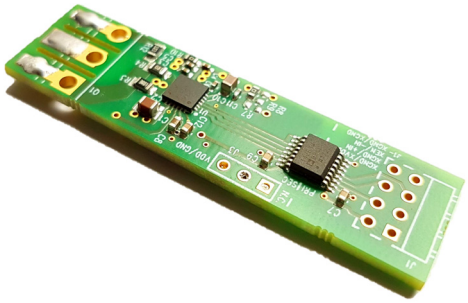

Figure 1. Evaluation Board Photo

Purpose

This document describes the use and applications for the NCP51705 SiC driver mini SMD EVB. The EVB is designed on a four layer PCB and includes the NCP51705 driver and all the necessary drive circuitry. The EVB also includes an on−board digital isolator and the ability to solder any MOSFET or SiC MOSFET in a TO−247 high voltage package. The EVB does not include a power stage and is generic from the point of view that it is not dedicated to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these EVBs can be configured in a totem pole type drive configuration. The EVB can be considered as an isolator+driver+TO−247 discrete module.

NCP51705 Description

The NCP51705 driver is designed to primarily drive SiC MOSFET transistors. To achieve the lowest possible conduction losses, the driver is capable of delivering the maximum allowable gate voltage to the SiC MOSFET device. By providing high peak current during turn−on and turn−off, switching losses are also minimized. For improved reliability, dv/dt immunity and even faster turn−off, the NCP51705 can utilize its on−board charge pump to generate a user selectable negative voltage rail. For full compatibility and to minimize the complexity of the bias solution in isolated gate drive applications the NCP51705 also provides an externally accessible 5 V rail to power the secondary side of digital or high speed optical isolators. The NCP51705 offers important protection functions such as under−voltage lockout monitoring for the bias power and thermal shutdown based on the junction temperature of the driver circuit. Internal simplify block diagram can be seen in Figure 2. More detailed information about all blocks could can be found in datasheet.

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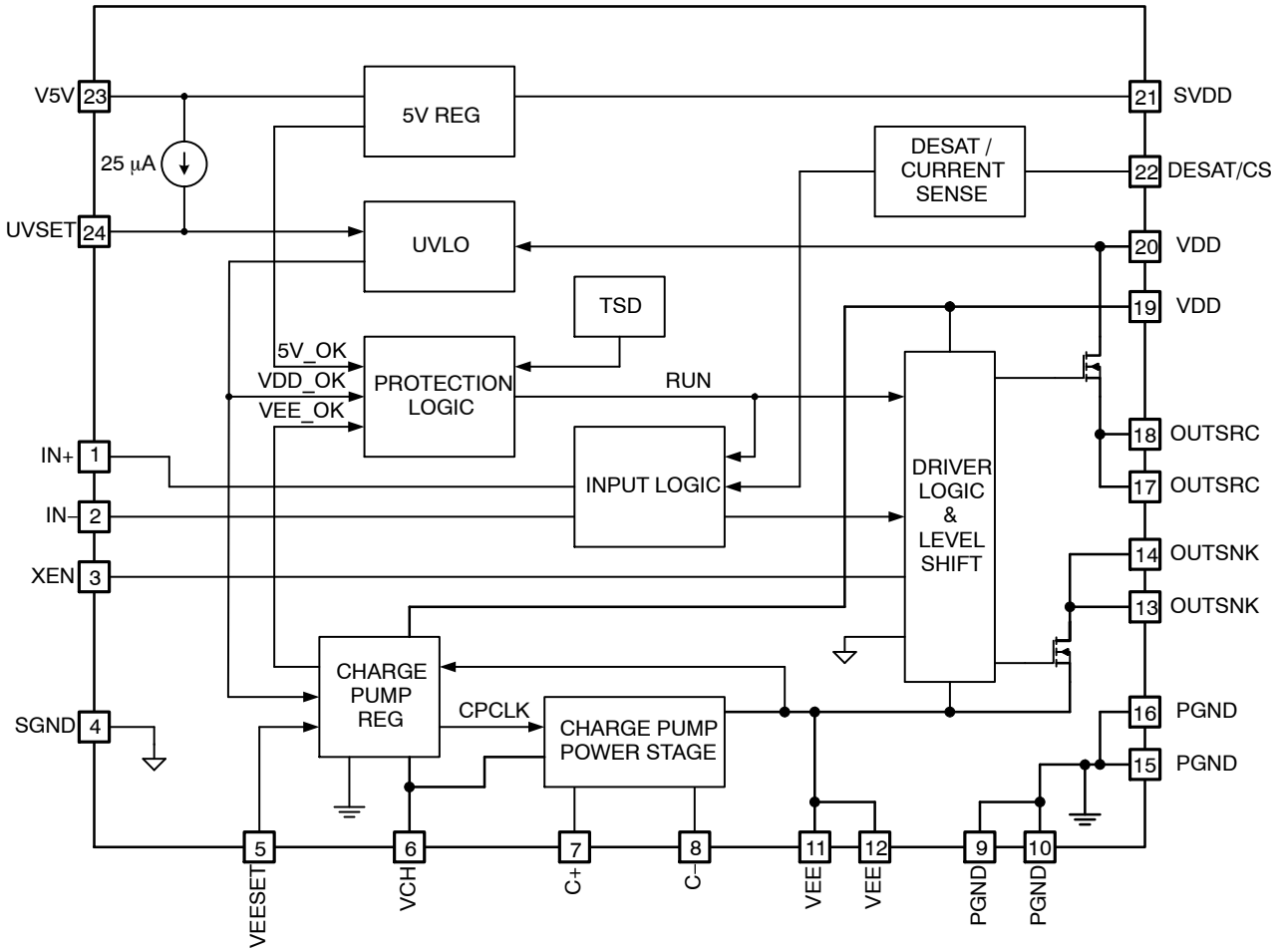

Figure 2. Simplified Block Diagram

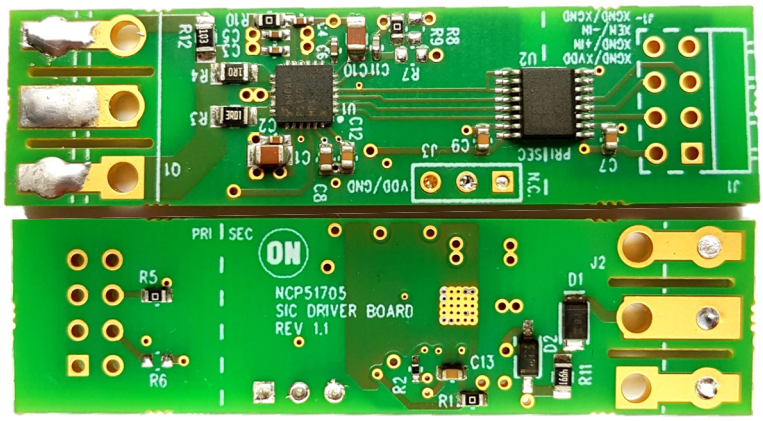

Figure 3. NCP51705 SMD Mini Board – Top and Bottom View

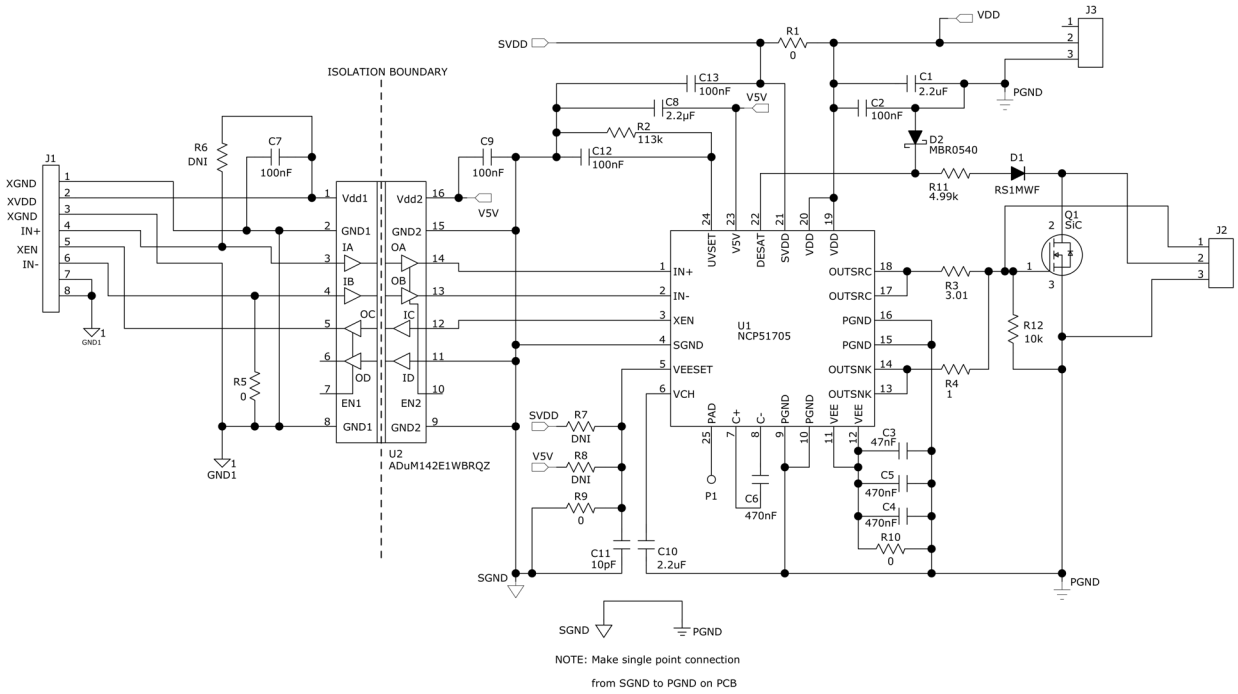

Figure 4. NCP51705 SMD Mini Board Schematic

Table 1. NCP51705 SMD MINI BOARD BOM

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
1	2	C1 C10	2.2 µF	CGA4J3X7R1H225M125AE	CAP, SMD, CERAMIC, 50V, X7R	TDK	805
2	1	C2	100 nF	C1005X7R1H104M050BE	CAP, SMD, CERAMIC, 50V, X7R	TDK	402
3	1	C3	47 nF		CAP, SMD, CERAMIC,25V, X7R	STD	402
4	3	C4−6	470 nF		CAP, SMD, CERAMIC, 25V, X5R	STD	402
5	3	C7 C9 C12	100 nF		CAP, SMD, CERAMIC, 10V, X7R	STD	603
6	1	C8	2.2 µF		CAP, SMD, CERAMIC, 10V, X7R	STD	603
7	1	C11	10 pF		CAP, SMD, CERAMIC, 50V, NPO	STD	402
8	1	C13	100 nF	C1608X7R1E104K080AA	CAP, SMD, CERAMIC, 25V, X7R	TDK	603
9	1	D1		RS1MWF	Diode, Fast, 1A, 1000V, Std. Rec.	Vishay	SOD123F
10	1	D2		MBR0540	Diode, Shottky, 40V, 500mA, 510mV	ON Semiconductor	SOD−123
11	1	J1		90122−0762	CON. 8P, RA, 266mil Mate, 114mil Post.	Molex	Thru−Hole
12	1	J2		10081031	Header, 3 pin, 5.08mm Spacing	Molex	Thru−Hole
13	1	J3		61300311121	Header, 3 pin, 100mil Spacing	Wurth	Thru−Hole
14	1	Q1		SiC	MOSFET, N−CH, 600V, 20A, 190mOhm	ON Semiconductor	TO−247
15	4	R1 R5 R9−10	0		RES, SMD, 1/10W	STD	603
16	1	R2	113k		RES, SMD, 1/16W	STD	402
17	1	R3	3.01		RES, SMD, 1/8W	STD	805
18	1	R4	1		RES, SMD, 1/8W	STD	805
19	3	R6−8	DNI		RES, SMD, 1/10W	STD	603
20	1	R11	4.99k		RES, SMD, 1/8W	STD	805
21	1	R12	10k		RES, SMD, 1/8W	STD	805

Table 1. NCP51705 SMD MINI BOARD BOM

22	1	U1		NCP51705	SiC Driver, Single, 6A, Single, MLP4x4−24	ON Semiconductor	MLP
23	1	U2		ADuM142E1WBRQZ	Digital Isolator, RF, 4−Channel	Analog Devices	QSOP−16

PCB Assembly and Layers

Figure 5 and Figure 6 shows the top and bottom assembly and the four − layers of the PCB. The PCB is 54 mm x 14 mm x 3 mm (length x width x height) where the width of the PCB is approximately the width of a TO − 247 body. The length of the boards can be reduce by cutting the board if 90° header connector (on the right hand side) and SMD pads on left hand side are not necessary.

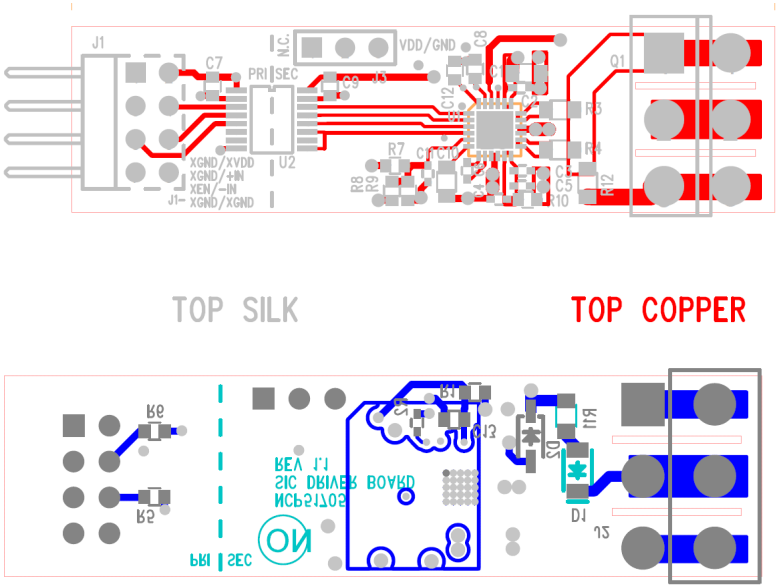

Figure 5. NCP51705 SMD Mini Board TOP/BOTTOM Assembly Drawing

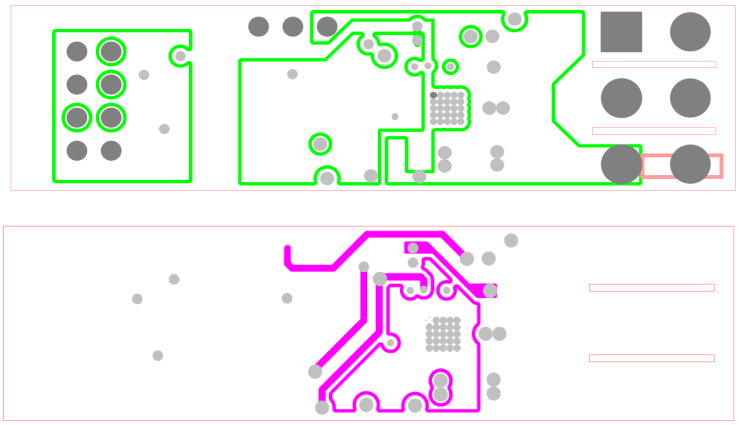

Figure 6. NCP51705 SMD Mini Board INNER_1/INNER_2 Layer Layouts

I/O Connectors

There are 3 I/O connectors including 17 pins described in Table 2 below. The uC (or PWM control IC) output (J1.4, J1.6), the XVDD and XGND (J1.2, J1.1) and the XEN (J1.5) signals are noted as “primary” ground referenced. There is no true “primary” and “secondary” ground but there is 1.5 kV galvanic isolation across the isolation boundary. It is especially important to maintain isolation in high−side, high−voltage, switching applications where the “secondary” VDD (J3.2 and J3.3) floats VDD volts above the power supply input voltage:

Table 2. I/O CONNECTORS DESCRIPTIONS

Ref Def	Name	I/O	GND Ref	Type	Description	Value [V]
J1.1	XGND	Power	Primary	Plated Hole	Ground	0 V
J1.2	XVDD	Power	Primary	Plated Hole	Positive primary power supply	5 V (Note 1)
J1.3	XGND	Power	Primary	Plated Hole	Ground	0 V
J1.4	IN+	Input	Primary	Plated Hole	Non−inverting PWM input	3.3 V – 5.5 V
J1.5	XEN	Output	Primary	Plated Hole	Fault flag or sync signal from NCP51705	5 V or 0 V
J1.6	IN−	Input	Primary	Plated Hole	Inverting PWM input	3.3 V – 5.5 V
J1.7	XGND	Power	Primary	Plated Hole	Ground	0 V
J1.8	XGND	Power	Primary	Plated Hole	Ground	0 V
J2.1	Gate	Output	Secondary	Plated Hole	Gate pin of a power switch	< 20 V
J2.2	Collector	Output	Secondary	Plated Hole	Collector pin of a power switch	≤ 1200 V
J2.3	Emitter	Output	Secondary	Plated Hole	Emitter pin of a power switch	0 V
J3.1	NC	NA	NA	Plated Hole	Not connected	NA
J3.2	VDD	Power	Secondary	Plated Hole	Positive branch Power supply	< 20 V
J3.3	GND	Power	Secondary	Plated Hole	Ground of the power supply	0 V
Q1.1	Gate	Output	Secondary	Plated Hole	Gate pin of a power switch	< 20 V
Q1.2	Collector	Output	Secondary	Plated Hole	Collector pin of a power switch	≤ 1200 V
Q1.3	Emitter	Output	Secondary	Plated Hole	Emitter pin of a power switch	0 V

1. The digital isolator requires that the amplitude of the PWM input (IN+ or IN−) be equal to XVDD and less than or equal to 5 V.

Mounting into Existing PCB

The NCP51705 SMD mini EVB can be mounted into an existing power board, shown as “Main PCB” in Figure 7. If there are no components or low profile surface mount components only, the mini SMD EVB can be mounted parallel to the main PCB as shown in Figure 7. The TO−247, power device leads would pass through the mini SMD EVB plated thru−holes and into the main PCB. Or, if necessary, the gate lead of the TO−247, power device can be soldered to the plated thru−hole on the mini SMD EVB and cut so that it does not contact the main PCB. For mechanical strength, it is preferred that the TO−247 gate lead pass through both PCB’s.

For SMD connection of the EVB board has prepared SMD pads to use TO−247 as SMD connection to the board as could be seen in Figure 7. This configuration is helpful for already existing application with horizontal TO−247 positions. SMD pads with 6 through−holes brings another degree of freedom how to mount the board.

Recommended procedure for Option 1 Mounting into an existing PCB:

1. On the main PCB, isolate the gate drive to the TO−247. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Place Kapton or non−conductive tape over the main PCB area directly beneath the mini SMD EVB.
   This is to avoid the possibility of having any components on the bottom of the mini SMD EVB touch components or conductive surfaces on the main PCB.
5. Solder a flying lead of bus wire to the main PCB, PWM signal and so on. Make sure there is enough length of the PWM input (flying lead) to reach through the mini SMD EVB.
6. For non−inverting PWM input logic, verify that R5 (0 Ω) is installed and R6 is removed. This is the correct configuration of the mini SMD EVB for non−inverting PWM input logic.
7. For inverting PWM input logic, verify that R6 (0 Ω) is installed and R5 is removed. This is the correct configuration of the mini SMD EVB for inverting PWM input logic.
8. Solder the TO−247 through just the mini SMD EVB first
9. With the TO−247 installed into the mini SMD EVB, install and solder the TO−247 leads into the main PCB.

10. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
11. Using the same size bus wire, solder the remaining connections between the mini SMD EVB to the appropriate locations on the main PCB.
12. Solder flying leads for bias voltage to the NCP51705. Note that J3 are across the isolation boundary from.

Mounting into Existing PCB − Option 2

If components mounted on the main PCB interfere with mounting the mini SMD EVB as described by Option 1 (Figure 7), the TO−247 leads can be formed (lead length may need to be added) with the mini SMD EVB mounted perpendicular to the main PCB as shown in Figure 8, option 2. If required, both mounting options allow the application of a heat sink to the TO−247 package. If high dv/dt is present on the drain of the TO−247, the EVB should be angled, away from being parallel to the TO−247, as much as possible.

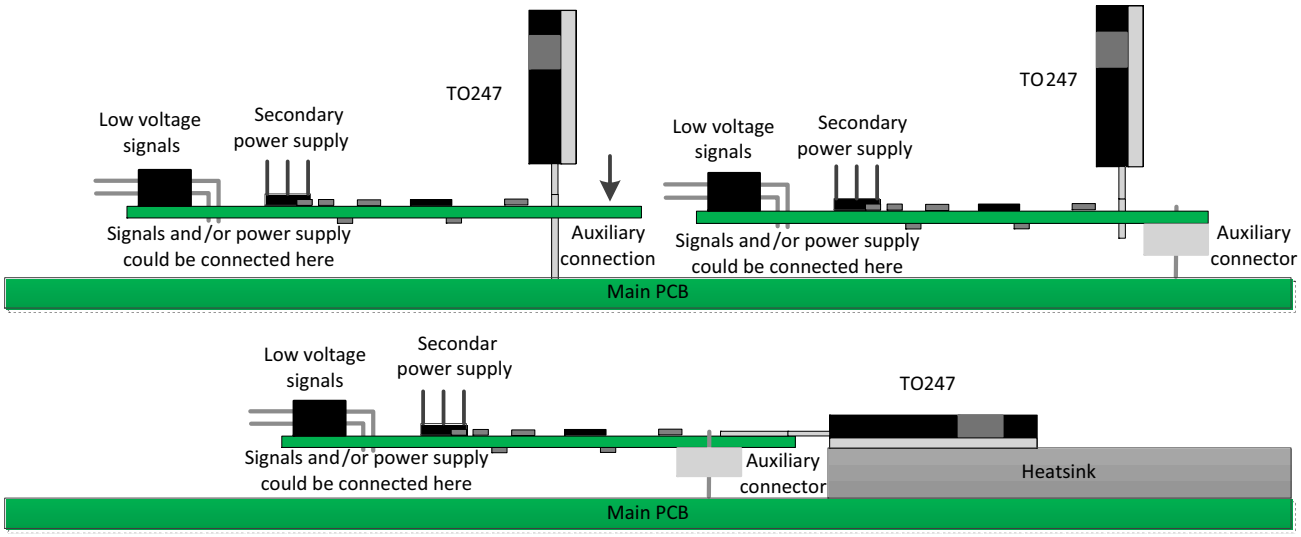

Figure 7. NCP51705 SMD Mini Board Installations

Mounting into Existing PCB − Option 2 (continued)

1. On the main PCB, isolate the gate drive to the TO−247 power device. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Solder a flying lead of bus wire to the main PCB, PWM signal. Make sure there is enough length of the PWM input (flying lead) to reach through the mini SMD EVB plated thru−hole.
5. For non−inverting PWM input logic, verify that R5 is installed and R6 is removed. This is the correct configuration of the mini SMD EVB for non−inverting PWM input logic.
6. For inverting PWM input logic, verify that R6 is installed and R5 is removed. This is the correct configuration of the mini SMD EVB for inverting PWM input logic.
7. After the TO−247 leads have been formed, check for fit through the mini SMD EVB and down into the main PCB
8. Solder the TO−247 through just the mini SMD EVB first
9. With the TO−247 installed into the mini SMD EVB, install and solder the TO−247 leads into the main PCB
10. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
11. Using the same size bus wire, solder the remaining connections between mini SMD EVB to the appropriate locations on the main PCB.
12. Solder flying leads from bias voltage to the NCP51705. Note that power supply connector is across the isolation boundary.

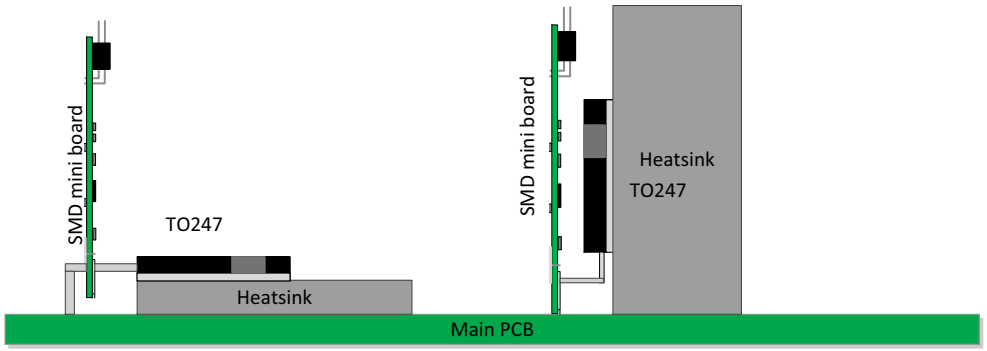

Figure 8. NCP51705 SMD Mini Board Installations

Mounting into New PCB Design

The NCP51705, SiC Driver mini SMD EVB can also be used as an isolator+driver+TO−247 “driver module” that can be integrated into a new PCB design. The gate lead of the TO−247 between the mini SMD EVB and the main PCB is for mechanical strength only. For main PCB layout, the gate lead extends down through the main PCB and can be soldered to an isolated plated thru−hole. As shown in Figure 9, shoulder pins with appropriate flange are one option that can be used as mounting pins between mini SMD EVB and the main PCB. Another option is to use a 100 mil center on center header which is a row of pins through a plastic header. The plastic header is used as a standoff for setting the mounting height between the mini SMD EVB and the main PCB.

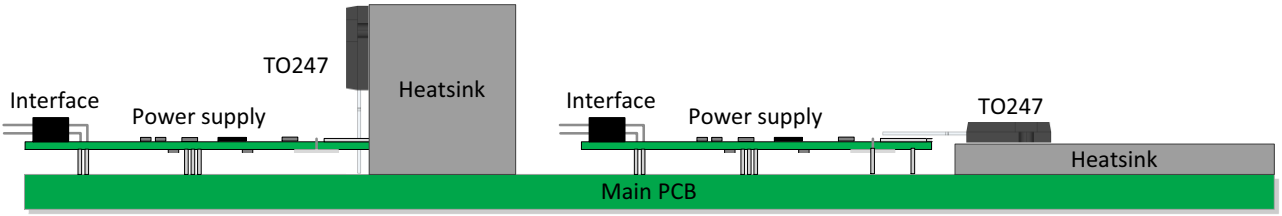

Figure 9. NCP51705 SMD Mini Board New Design Installations

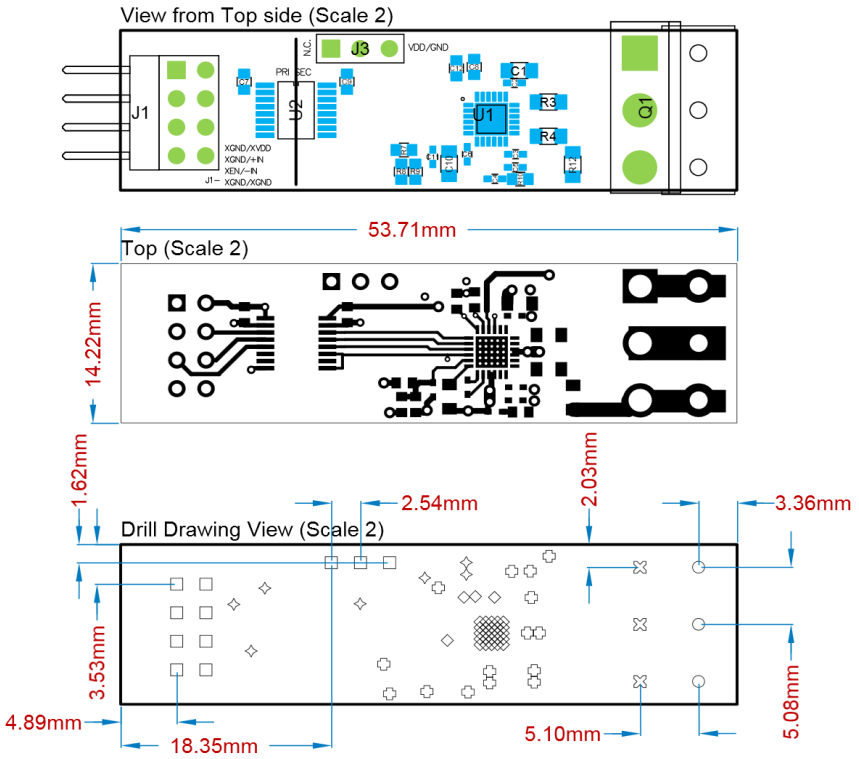

Figure 10. NCP51705 SiC EVB PCB Hole Pattern

Testing without Installing into a PCB

The NCP51705, SiC Driver mini SMD EVB can also be tested without installing into a main PCB. However, since this EVB was designed for small form factor there are no test points included for connecting voltage probes. The EVB should be hand probed carefully since the components are very fine pitch or flying leads connected to desired probe points can be attached. Note that the IN+/IN− PWM amplitude must be equal to the XVDD (5 V). The 20 VDC bias (VDD and GND) is on the secondary side of the digital isolator and therefore has a separate/isolated return ground from the 5 VDC bias (XVDD and XGND). The recommended series load of below 1 nF and 4.7 Ω is close to what might be representative of a SiC gate drive input impedance. Leaded passive components can be soldered into the TO−247 holes as shown in Figure 9. Alternatively, a TO−247 SiC MOSFET can also be soldered in place for Q1 and used as a load for the NCP51705. Note that testing without installing into a power stage, leaves the DESAT pin open since there is no active drain signal. The effect of operating DESAT this way is explained in section ‘DESAT’.

Turn−on Procedure

1. Apply XVDD = 5 V (Voltage for primary side of the digital isolator, U2)
2. Apply VDD = 20 V (VDD bias voltage for the NCP5170, SiC driver, Note: $UVLO_{ON}$ = 17 V)
3. Apply IN+ = 5 V_{pk}, 150 kHz, 50% (Reducing the frequency to less than ~90 kHz will show DESAT active as described in section ‘DESAT’)

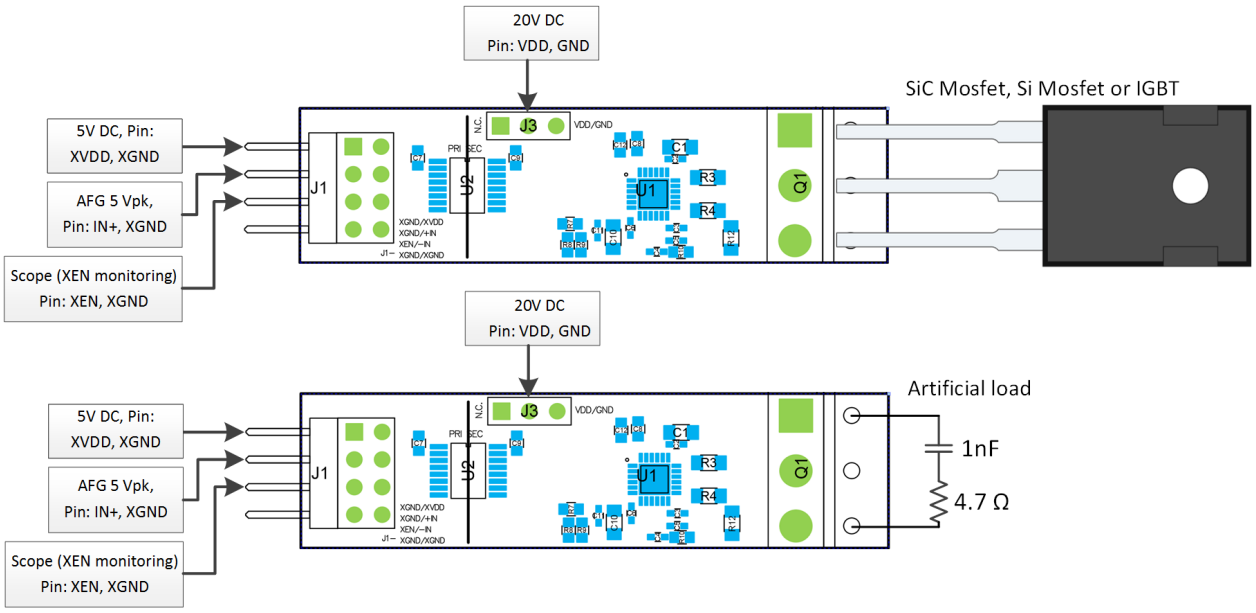

Figure 11. Test Configuration of EVB without Installing into Main PCB

VEE

The EVB is preconfigured for VEE = 0 V. Operating the EVB this way will result in switching between 0V < OUT < VDD. Several other options for negative VEE configuration are easily set by removing/installing resistors according to Table 3. Note that R10 must be removed for any VEE configuration other than 0 V. VDD_{UVLO} is programmable by the UVSET resistor as described in section 'UVSET' but VEE_{UVLO} is fixed at 80% of the VEE regulate value. If desired, the NCP5170 internal VEE charge pump can be disabled and an external negative voltage can be applied to VEE. When providing VEE from an external negative voltage supply, it is recommended to apply VEE prior to VDD. Any time the internal VEE charge pump is disabled (VEESET = 0 V), VEE_{UVLO} is disabled and is therefore shown as "NA" in Table 3.

Table 3. VEESET CONFIGURATION OPTIONS

VEESET	Comment	VEE	VEE_{UVLO}
VDD	Install R7 = 0 Ω, Remove R8, R9, R10, 9V < VEESET < VDD	−8 V	−6.4 V
V5V	Install R7 = 0 Ω , Remove R7, R9, R10	−5 V	−4 V
OPEN	Remove R7, R8, R9, R10	−3 V	−2.4 V
GND	Install R9 = R10 = 0 Ω , Remove R7, R8	0 V	NA
GND	Remove R7, R8, R9, R10. Apply negative external voltage within the range of −8 V < Vext < 0 V	−Vext	NA

UVSET

The UVSET function is set by R2 and determines the UVLO turn−on threshold. The EVB is preconfigured with R2 = 113 kΩ which equates to UVLO turn−on (V_{ON}) of ~17 V. The UVLO turn−on threshold can be changed by selecting R2 according to a desired UVLO turn−on threshold, V_{ON}:

$$R_2 = \frac{V_{on}}{6 \cdot 25\ \mu A} \qquad \text{(eq. 1)}$$

DESAT

DESAT is a type of over−current protection dedicated to monitoring the $I_D \cdot R_{DS}$ of the SiC MOSFET. The EVB is preconfigured with R11 = 4.99 kΩ (DESAT resistor). The internal DESAT threshold is fixed at $V_{DESAT(TH)}$ = 7.5 V and the DESAT signal amplitude is adjustable by R11. R11 = 4.99 kΩ may not be the correct resistor value for some applications. If V_{DESAT} > 7.5 V during normal operation, decrease R11 to lower the signal amplitude. If DESAT is active, the trailing edge of the OUT pulse is terminated or reduced with respect to the input pulse (IN+). The waveforms shown in Figure 14, show V_{DESAT} < 7.5 V during normal operation. Since DESAT is operating with no load, the amplitude is varied by varying the IN+ frequency. Figure 13 shows IN+ increased to 150 kHz and VDESAT = 7.5 V. The trailing edge of OUT is clearly terminated compared to IN+ indicating that DESAT is active.

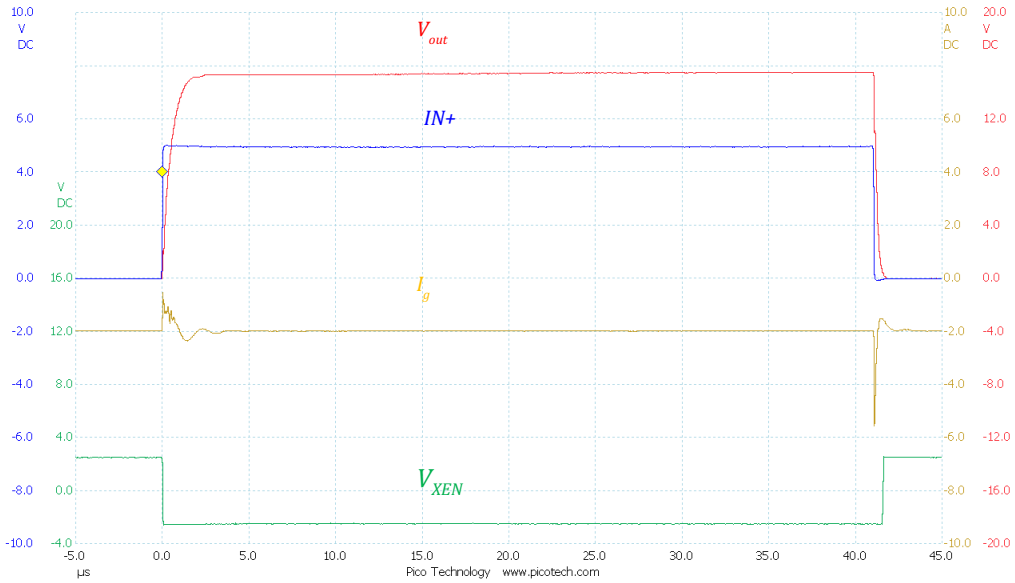

Figure 12. Normal Operation for Turn−on and Turn−off

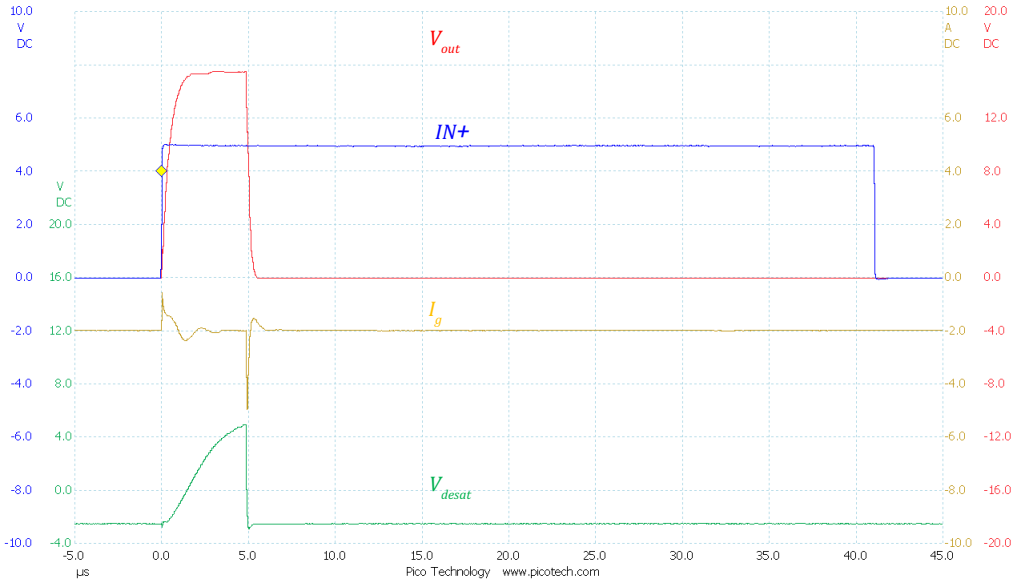

Figure 13. DESAT Functionality Test

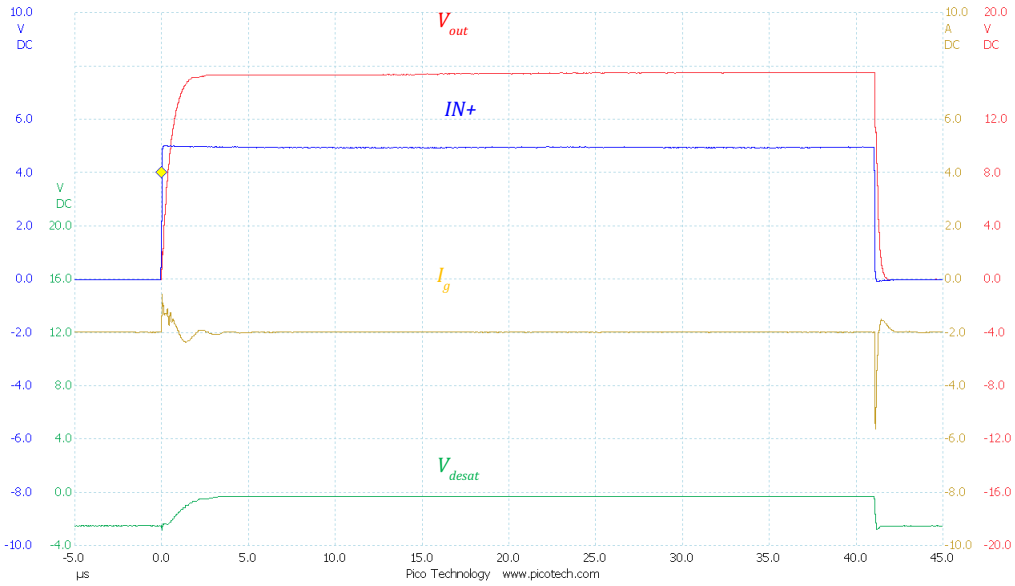

Figure 14. Normal Operation including DESAT Pin

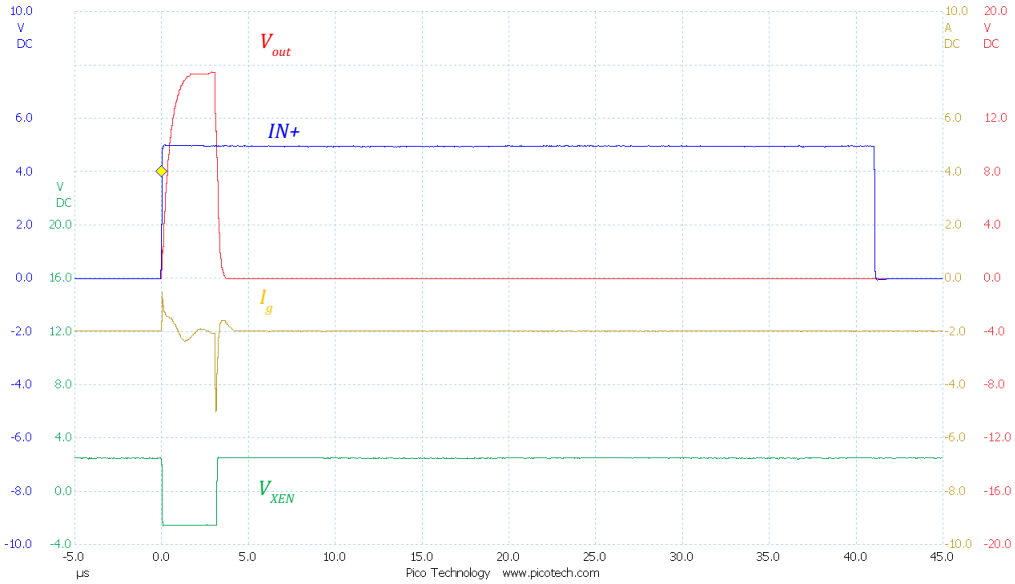

Figure 15. Reaction of XEN Pin on DESAT Fault State

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