NCV7422V1GEVB

NCV7422 Dual LIN Transceiver Evaluation Board User's Manual

ON Semiconductor®

www.onsemi.com

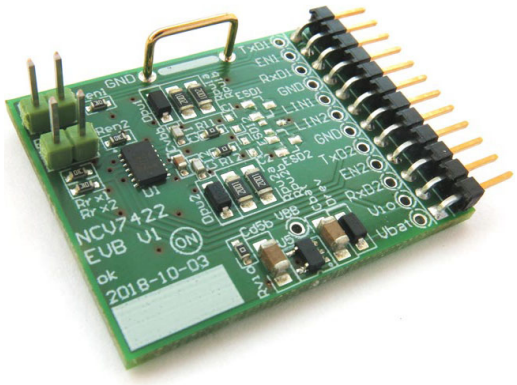
EVAL BOARD USER'S MANUAL

INTRODUCTION

This document describes the evaluation board for the ON Semiconductor two channel LIN transceiver NCV7422. The board provides basic connections for a device evaluation.

EVALUATION BOARD FEATURES

- One−row pin header providing access to all the device pins, enables easy insertion of the evaluation board into a more complex application setup.
- On−board 5 V LDO for RxD1/2 pull−up resistors and EN inputs
- Standard LIN master terminations
- Position for optional ESD protection



NCV7422V1GEVB
Evaluation Board

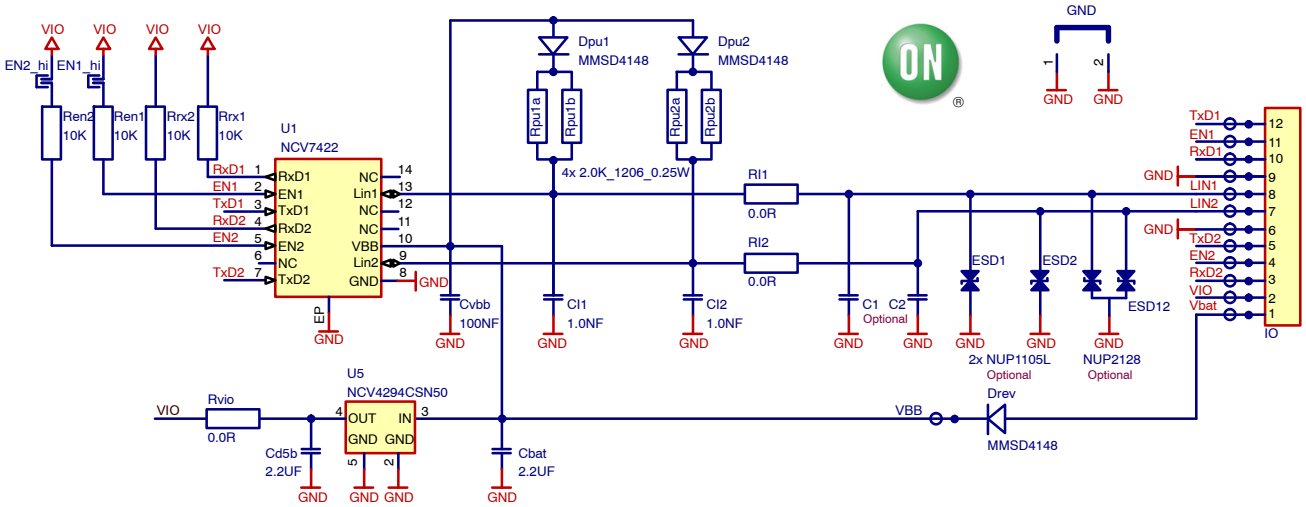


Figure 1. NCV7422 Evaluation Board Schematic

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Pins	Min	Max	Unit
Battery supply voltage	Vbat	−42	42	V
Digital inputs/outputs supply voltage	VIO (Rvio not used)	−0.3	7	V
Digital inputs/outputs voltage	TxD1/2, RxD1/2, EN1/2	−0.3	7	V
LIN bus line voltage	LIN1, LIN2	−42	42	V
NCV7422 junction temperature		−40	+150	°C
Board temperature		−40	+125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED BOARD OPERATING CONDITIONS

Rating	Pins	Min	Max	Unit
Battery supply voltage	Vbat	5	18	V
Digital inputs/outputs supply voltage	VIO (Rvio not used)	2.8	7	V
Digital inputs/outputs voltage	TxD1/2, RxD1/2, EN1/2	0	VIO	V
LIN bus line voltage	LIN1, LIN2	0	Vbat	V
NCV7422 junction temperature		−40	+150	°C
Board temperature		−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

OPERATIONAL GUIDELINES

NCV7422 evaluation board allows easy evaluation of NCV7422 two channel LIN transceiver. It provides connection to all the device's pins as well as positions for all the necessary master / slave LIN bus external components.

Configurations and assembly options are listed in Table 3.

For more information please check NCV7422 transceiver datasheet at www.onsemi.com.

Table 3. ASSEMBLY OPTIONS AND CONFIGURATIONS

Component	Master (Default)	Slave	Function
Dpu1, Dpu2	MMSD4148	–	Master pull−up diodes
Rpu1a/b, Rpu2a/b	2.0k	–	Master pull−up resistors
Cl1, Cl2	1nF	220pF	LIN bus capacitors
C1, C2	–	–	LIN bus capacitors
Rl1, Rl2	0R		LIN bus serial impedance
ESD1, ESD2	optional		LIN bus ESD protections
Rvio	0R		Connection on−board LDO to TxD1/2 and EN1/2 pull−up resistors. If removed, external supply can be used (connected to VIO).
EN1/2_hi	Closed		EN1/2 pin connections: Open = EN1/2 weak internal pull−down = Sleep mode Closed = EN1/2 pulled up to VIO (5 V by default) = Normal mode

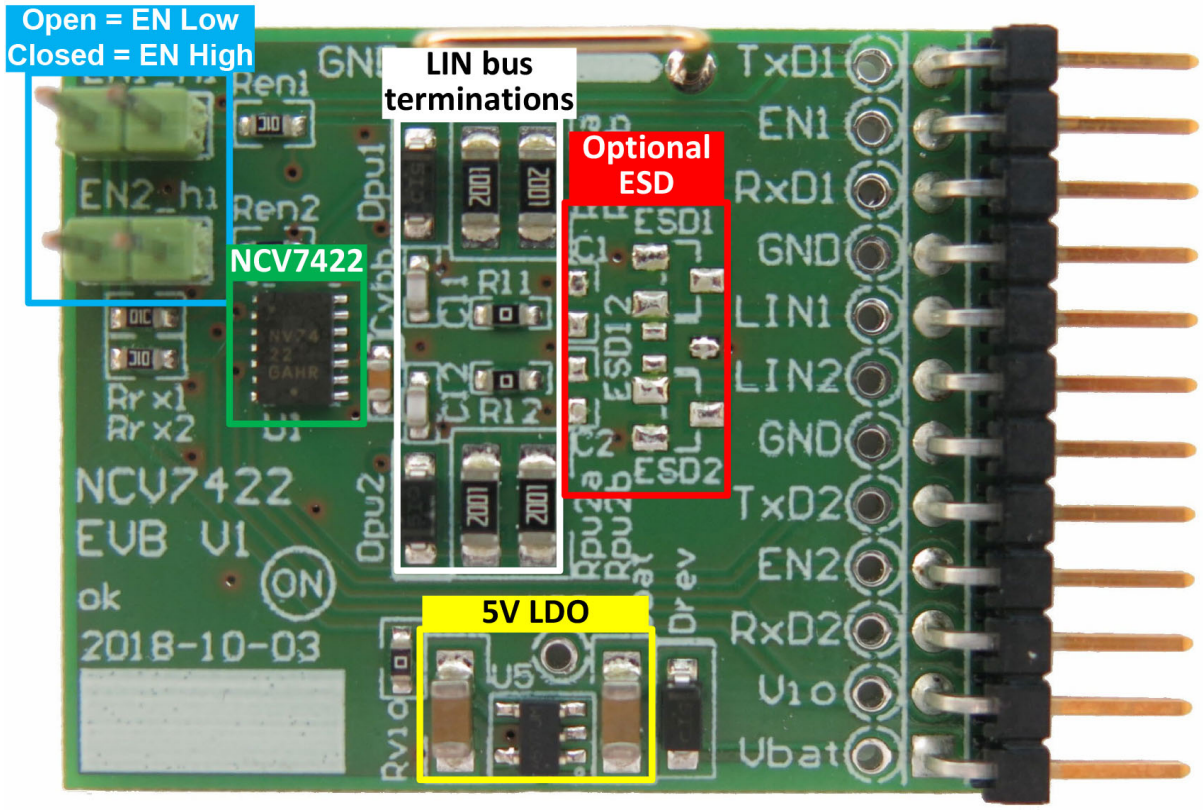


Figure 2. NCV7422 PCB Bottom Composite Drawing (Mirrored)

PCB DRAWINGS

Composite Drawings

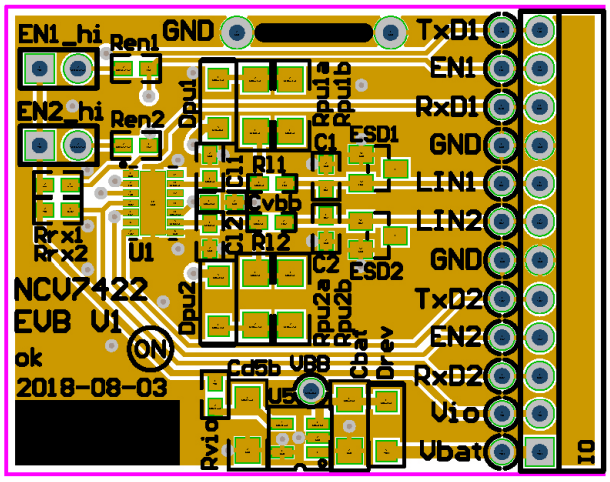


Figure 3. NCV7422 EVB PCB Top Drawing

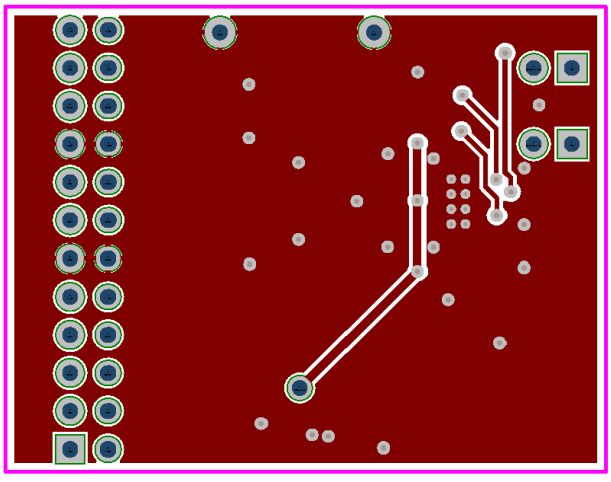


Figure 4. NCV7422 EVB PCB Bottom Drawing (Bottom View)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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