EVBUM2663

NCD57200 Evaluation Board

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Introduction

The NCD57200 Evaluation module is designed for evaluation of the NCD57200 IGBT Half−Bridge driver products family.

The NCD57200 is a high voltage gate driver with one non−isolated low side gate driver and one galvanic isolated high or low side gate driver. It can directly drive two IGBTs in a half bridge configuration. Bootstrap technique can be used for powering up the isolated high side gate driver for easy use.

The galvanic isolation for the high side gate driver guarantees reliable switching in high power applications for IGBTs that operate up to 900 V, at high dv/dt. The optimized output stages provide a mean of reducing IGBT losses. Its features include two independent inputs with accurate asymmetric UVLOs, and short and matched propagation delays. The NCD57200 operates with its V_{DD}/V_B up to 25 V.

Description

The board was created for the ability to verify and test the datasheet parameters or to be externally connected to power devices. It contains all the necessary peripheral components for direct connection to the power device. All connections are made by surface−mount test point loops allow easy probe connection. The input bias is configured so the VB high−side bias can be sourced from VDD, or an external additional bias can be added to provide VB directly. The high−side and low−side retuns are separated on VS and GND to allow evaluation of the NCD57200 high−side negative voltage capabilities. The PCB design is optimized to reduce loop areas and provide clear and simple measurement of all signals. All the parts are TOP mounted which allows easy replacement and can serve as an ideal reference design for future use.

Features

- High Peak Output Current (+1.9 A/−2.3 A)
- Low Output Voltage Drop for Enhanced IGBT Conduction
- Secured Output Low State without VDD/VB
- Floating Channel for Bootstrap Operation up to +900 V
- CMTI up to 50 kV/μs
- Reliable Operation for VS Negative Swing To −900 V
- VDD & VBS Supply Range up to 25 V
- 3.3 V, 5 V, and 15 V Logic Input
- Asymmetric Under Voltage Lockout Thresholds for High Side and Low Side
- Matched Propagation Delay 110 ns
- Built−in 20 ns Input Noise Filter
- Built−in 300 ns Dead−Time and High and Low Inputs Interlock
- Output in Phase with Input Signal
- PCB Layout Optimized for Power Supply Bypassing Capacitor, Gate−driver Loop
- Capacitive Load with Separated External Gate−drive Resistors (RG_{ON}, RG_{OFF})
- Allows Quick Verification of most of the Data Sheet Parameters
- Test Points Allow Probing all the Key Pins of the NCD57200

PIN Description

Table 1. EVALUATION BOARD PIN DESCRIPTION

Pins Name	Pins Number	Description
VDD	TP1	VDD positive input of NCD57200, Powers the driver on primary side
VB	TP2	VB power input, Powers the driver on secondary side through Current limiting resistor
VCC	TP3	VCC power input of evaluation board, Powers the driver on primary side through Current limiting resistor
HO	TP5	High−side output pin
HIN	TP6	High−side input pin
HS−LD	TP7	High−side output at capacitive load
PWMIN−H	TP8	High−side signal input
LO−LD	TP12	Low−side output at capacitive load
LO	TP13	Low−side output pin
LIN	TP17	Low−side input pin
PWMIN−L	TP18	Low−side signal input
VS	TP9, TP10, TP21	Multiple test point − Negative VB input, high−side power ground
GND	TP4, TP11, TP14, TP15, TP16, TP19, TP20, TP22	Multiple test point − Negative VDD input, primary ground of DR1

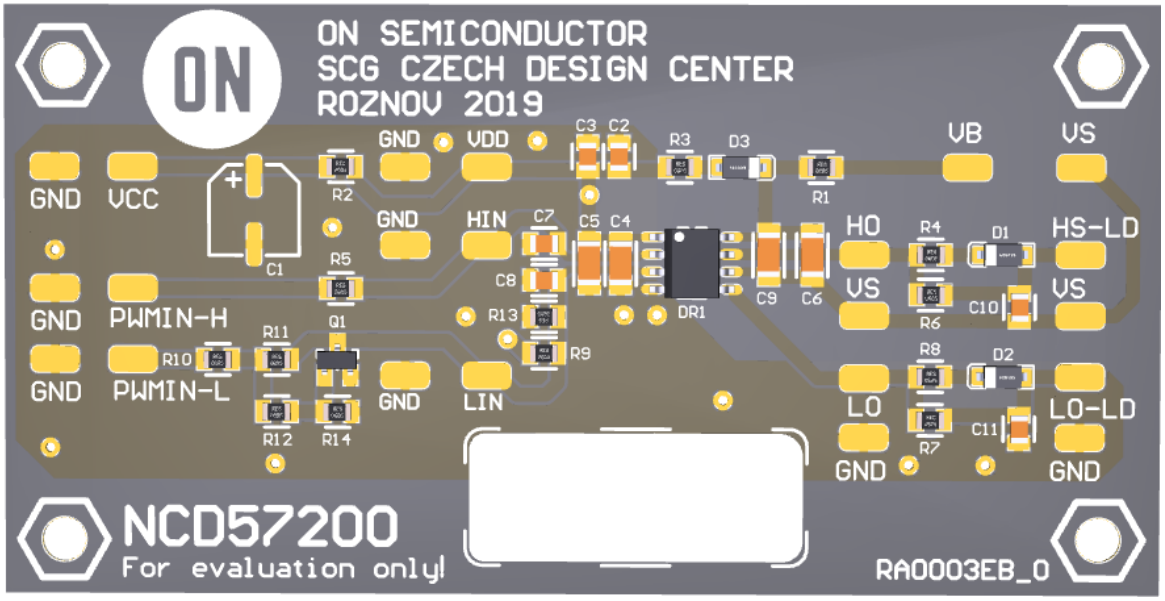

Figure 1. PCB TOP View

Electrical Specification

Table 2. NCD57200 ELECTRICAL SPECIFICATION

Description		MIN	TYP	MAX	Unit
V_{DD}	Input bias power supply	13		25	V
V_B	High−Side power supply (ready for bootstrap power supply)	12		25	V
PWMIN−X	Input signal switching frequency	0		500	kHz
T_J	Operating junction temperature range	−40		125	°C

TEST SPECIFICATION

This section provides details how to configure the NCD57200 Evaluation board. Basic laboratory equipment will be required to perform the tests.

Equipment

- Power supplies
  - A DC power supply providing minimally 25 V/1 A
- Function generator
  - Two channel functional generator providing the required testing frequency
- Oscilloscope
  - Oscilloscope 2 channel (4 channel optional)
  - Passive probes
  - Current probe (optional)
- Digital multimeter
  - Allows DC current measurement

Bench Test setup

The bench test setup shows the equipment connections. Use basic setup procedure as a reference:

- Make sure the power supplies & outputs of signal generators are powered off / disabled
- Connect functional generator to the PWMIN−H and PWMIN−L signal inputs and GND
- Connect power supply positive lead to the VCC (use digital multimeter to measure input current)
- Connect power supply negative lead to the GND
- Connect oscilloscope probes to HO−LD and LO−LD test points

Power Up

1. Before the power−up, verify the correct connection of all signals and power leads
2. Enable power supply and check the current consumption on the digital multimeter. If is less than 1 mA, everything is set correctly
3. Enable function generator outputs
4. Check the signals at each outputs

Power Down

1. Disable functional generator outputs
2. Disable power supply
3. Disconnect equipment

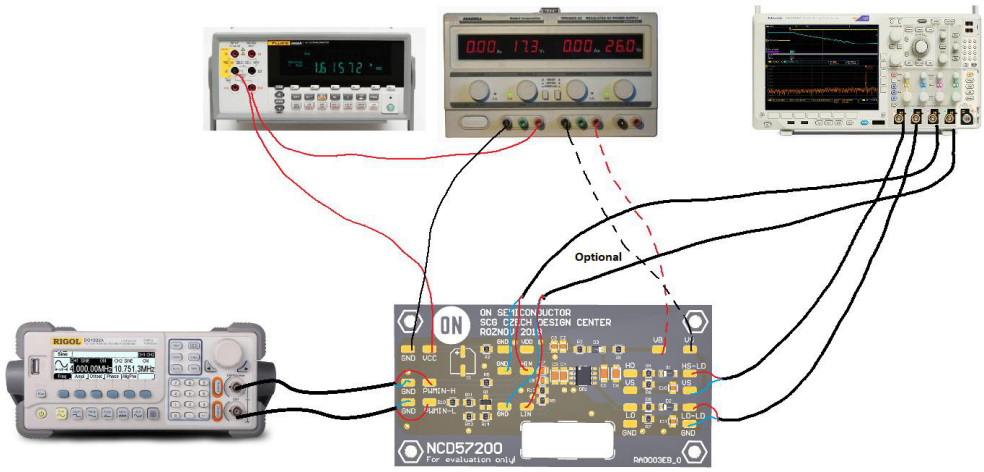

Figure 2. Test 1−2 Setup Diagram

Test 1: Current Consumption

To evaluate the Driver at
(A) no switching current consumption and
(B) current consumption at different signal frequencies

A. Power up the setup, turn off the signal generator outputs
   - Digital multimeter displays the standby current under 1 mA

B. Power up the setup, gradually set the output frequency
   ($R_{G-ON/OFF}$ = 0 R, C_{LOAD} = 1 nF)
   - Digital multimeter displays the current dependent on input signal frequency

Table 3. NCD57200 CURRENT CONSUMPTION

PWMIN Frequency (kHz)	IDD (mA)
0	0.6
10	2.2
50	4
100	6
200	11
500	23

Test 2 – Typical Performance Waveforms

To evaluate propagation delay, the input signals must have dead time greater than the internal dead time. (Depend on the driver version – see the specific values in the datasheet).

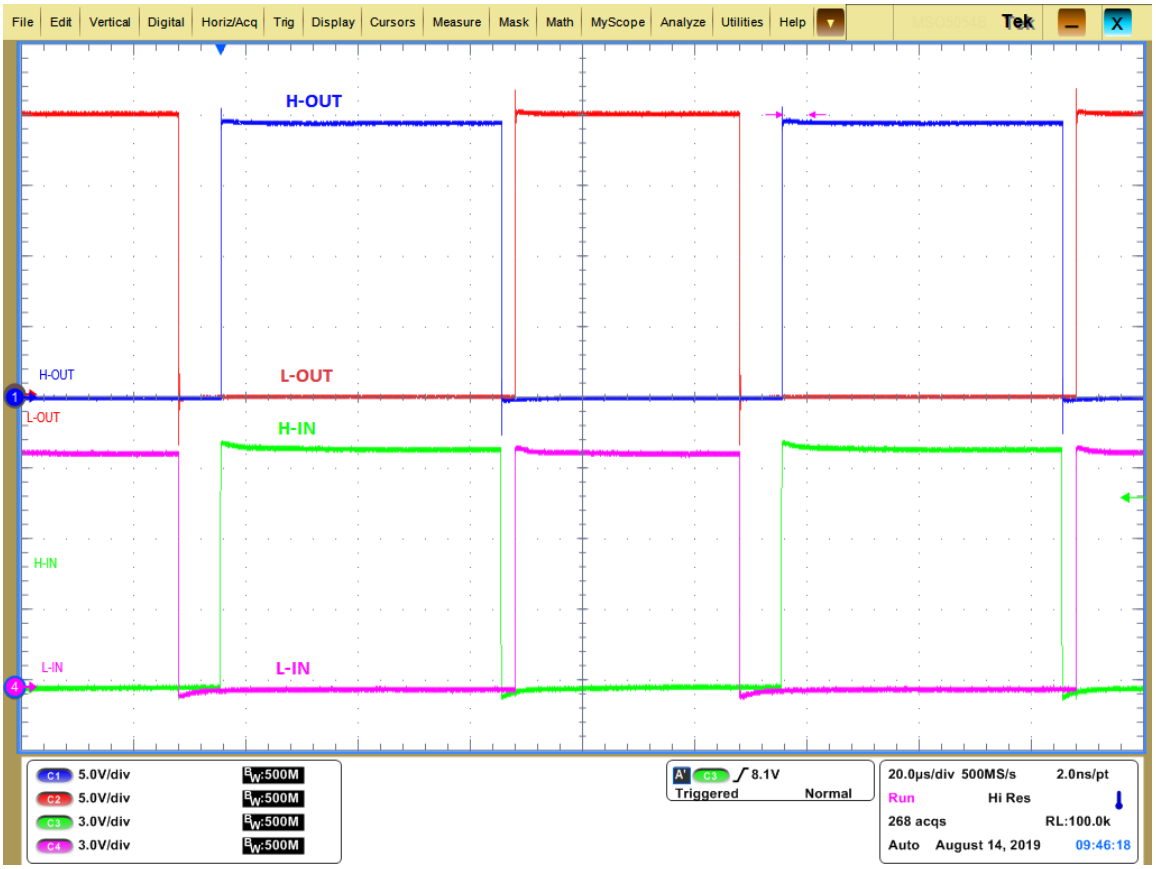

Figure 3. INPUT and OUTPUT Waveforms

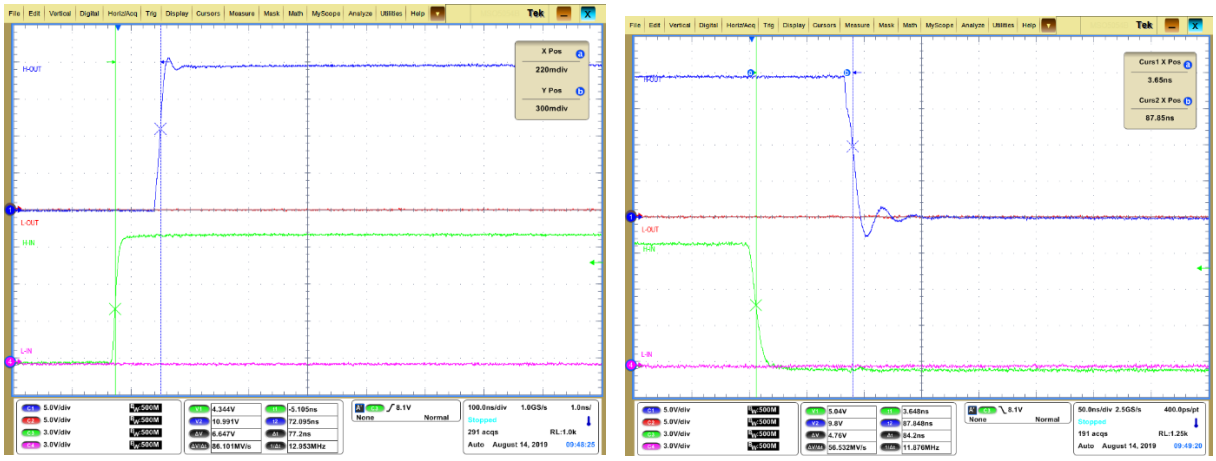

Figure 4. HS−IN and HS−OUT Waveforms

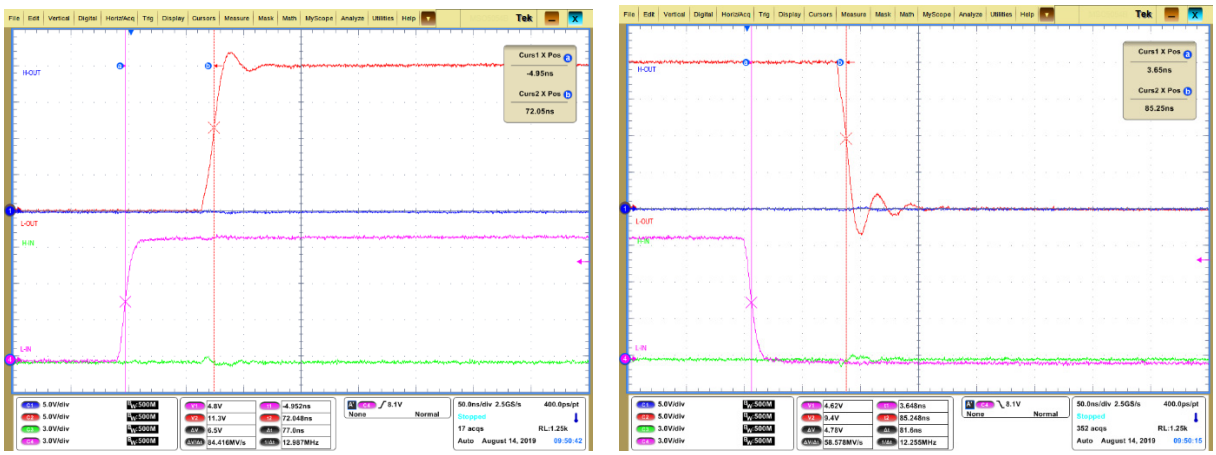

Figure 5. LS−IN and LS−OUT Waveforms

Test 3 – Typical Performance Waveforms – Output Current (Optional Advanced)

To evaluate maximum output peak current, the input signals must have dead time greater than the internal dead time. (Depend on the driver version – see the specific values in the datasheet). Setup need to be adjusted to allow maximum peak current measurement.

Required Changes:

- Current probes are required
- Place (solder) loading capacitors to the output loading point HS−LD/VS and LS−LD/GND
  - Typical testing value is 100 nF/50 V
  - Recommended using leaded package to create a current measuring loop

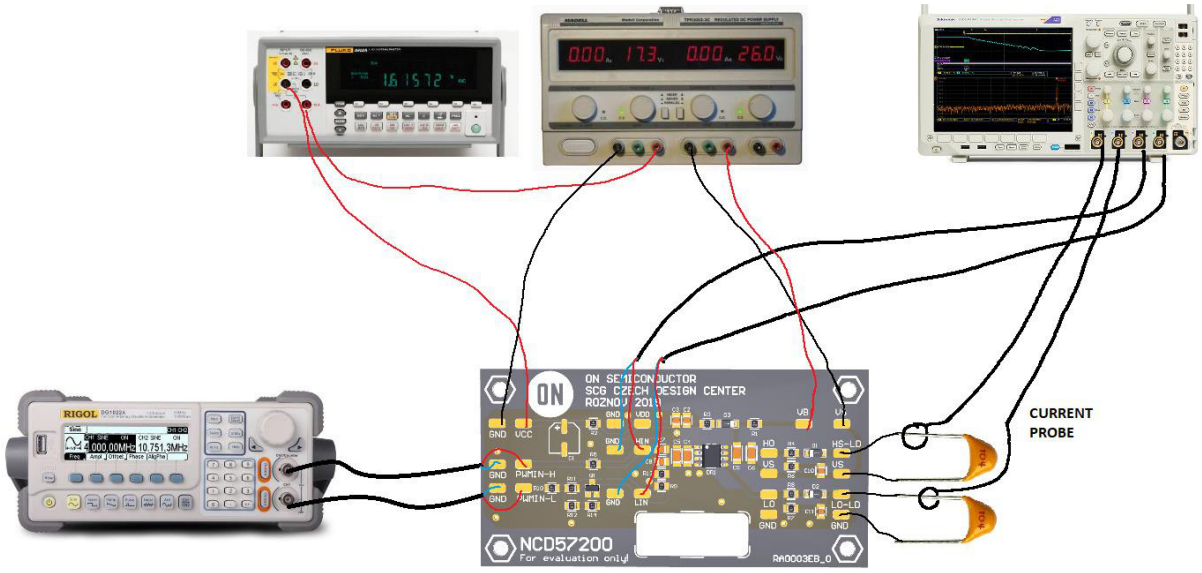

Figure 6. Test 3 Setup Diagram

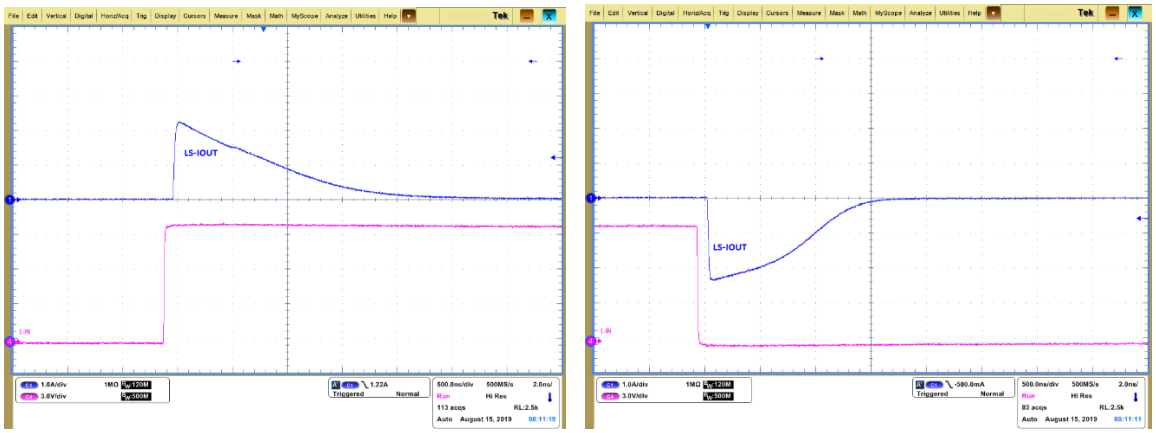

Figure 7. LS Current Waveforms

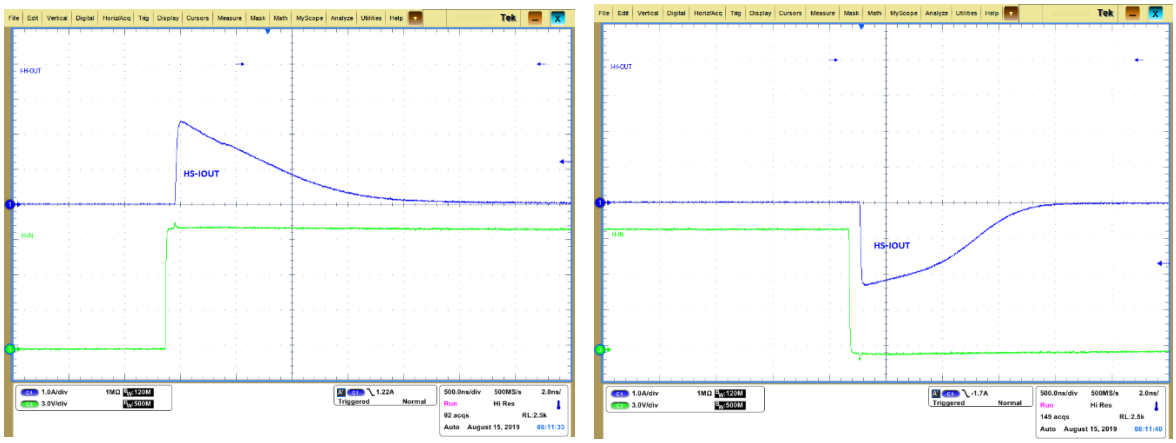

Figure 8. HS Current Waveforms

SCHEMATIC & LAYOUT DIAGRAMS

Schematic Diagram

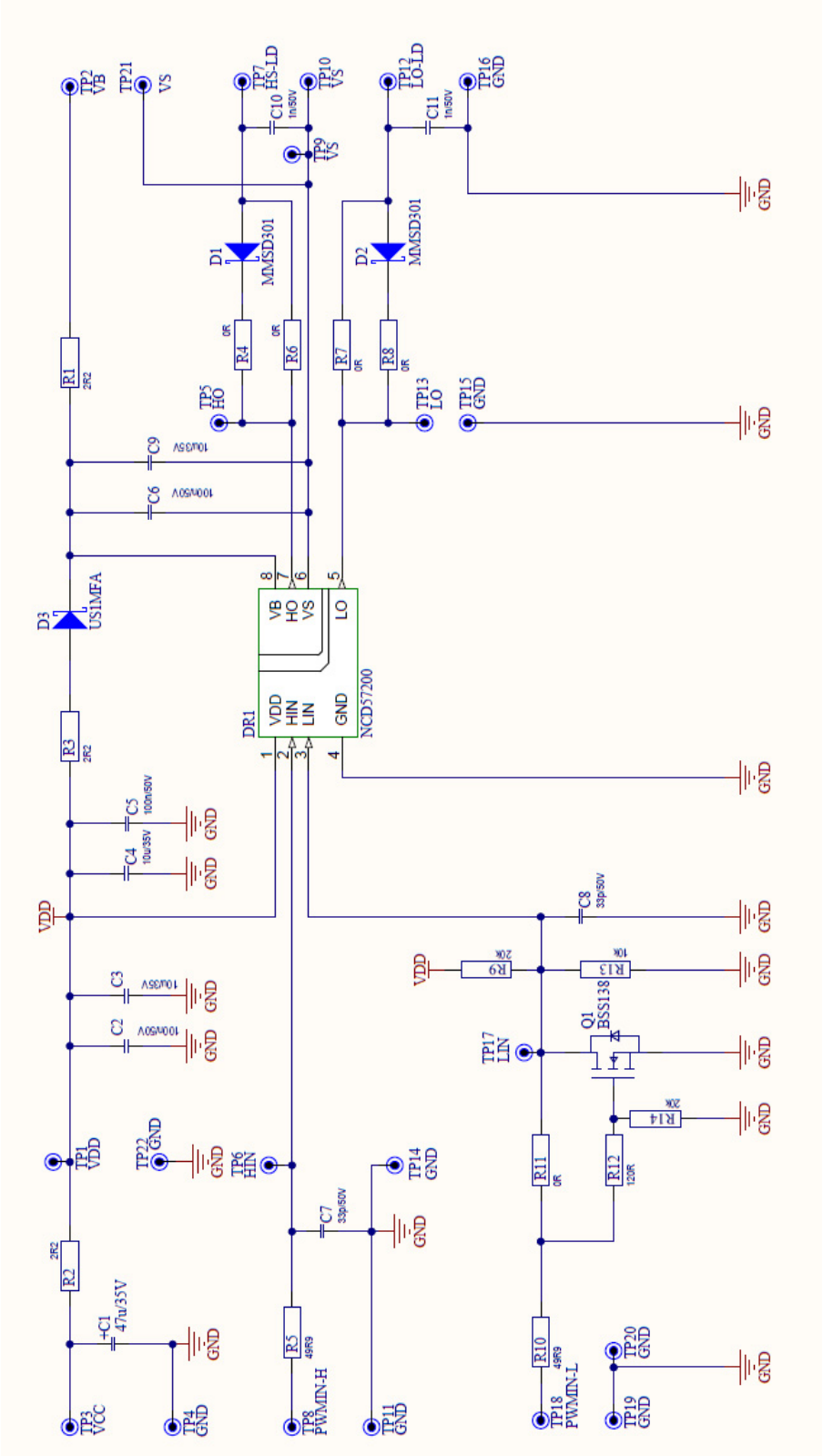

Figure 9. Schematics

Layout Diagrams

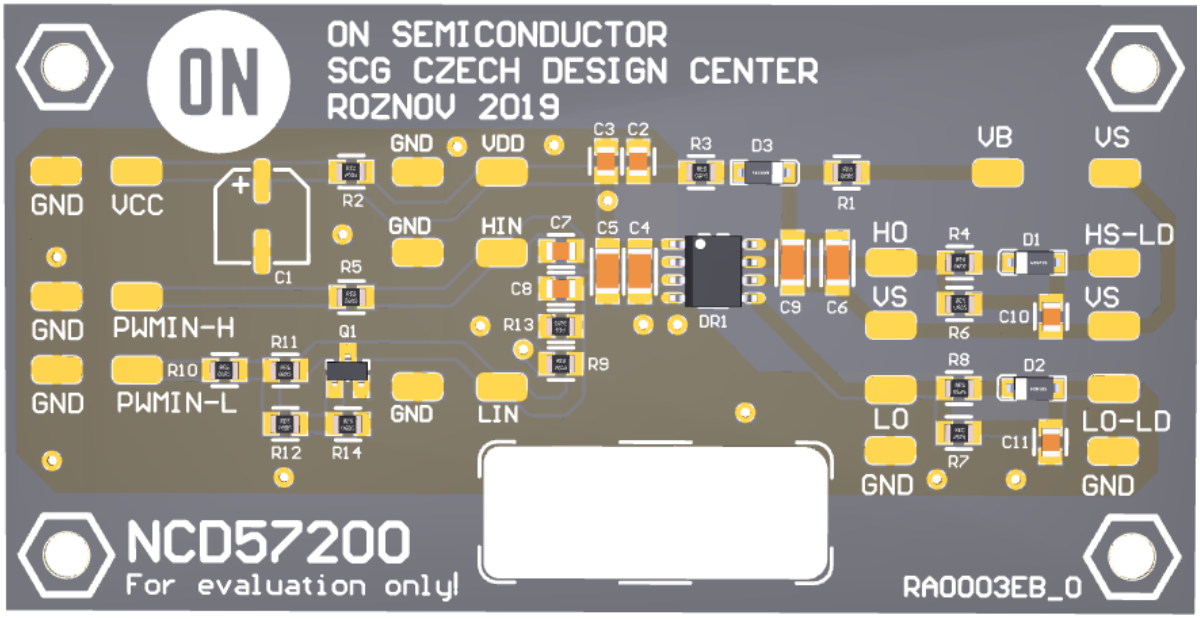

Figure 10. Assembled PCB TOP View

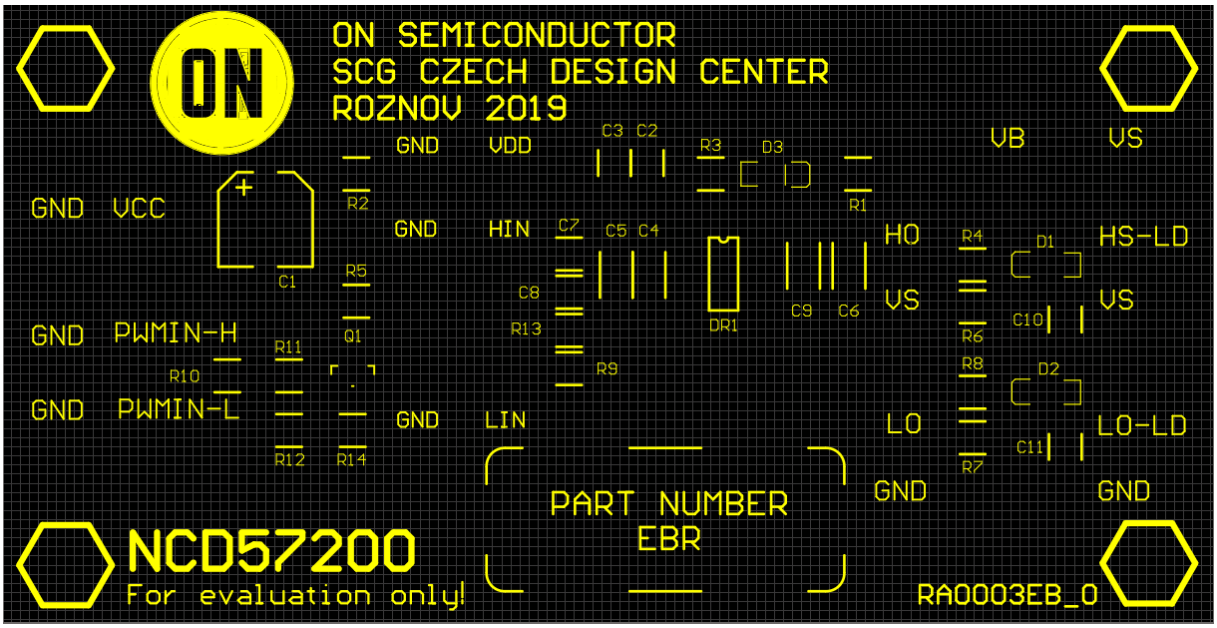

Figure 11. TOP Overlay

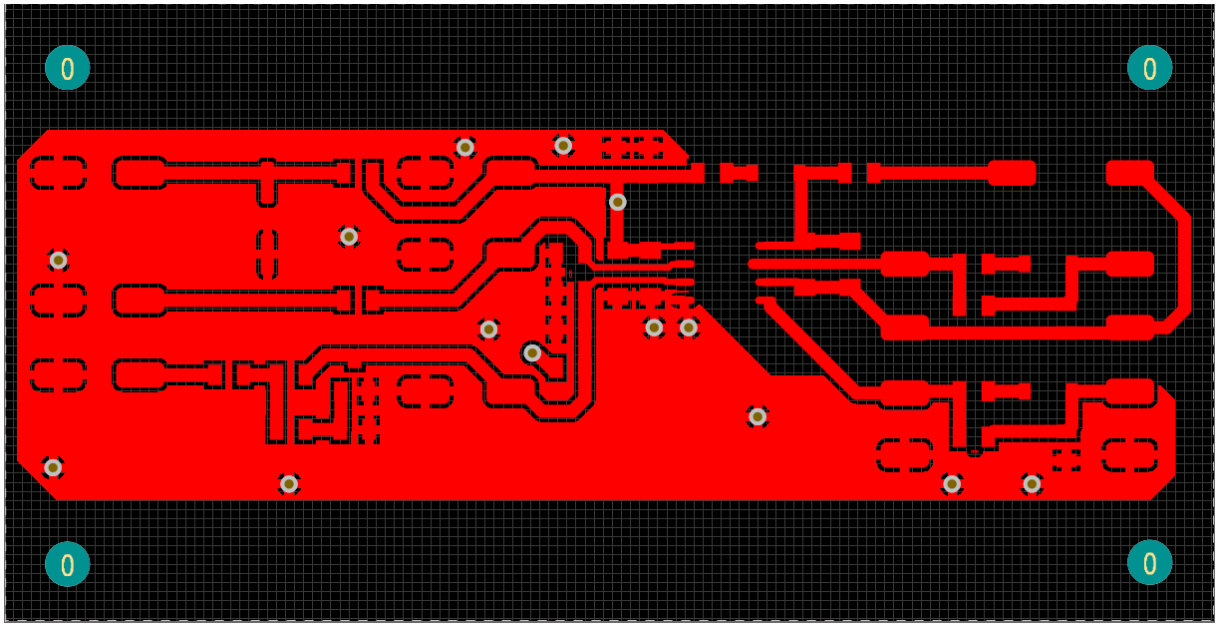

Figure 12. TOP Layer

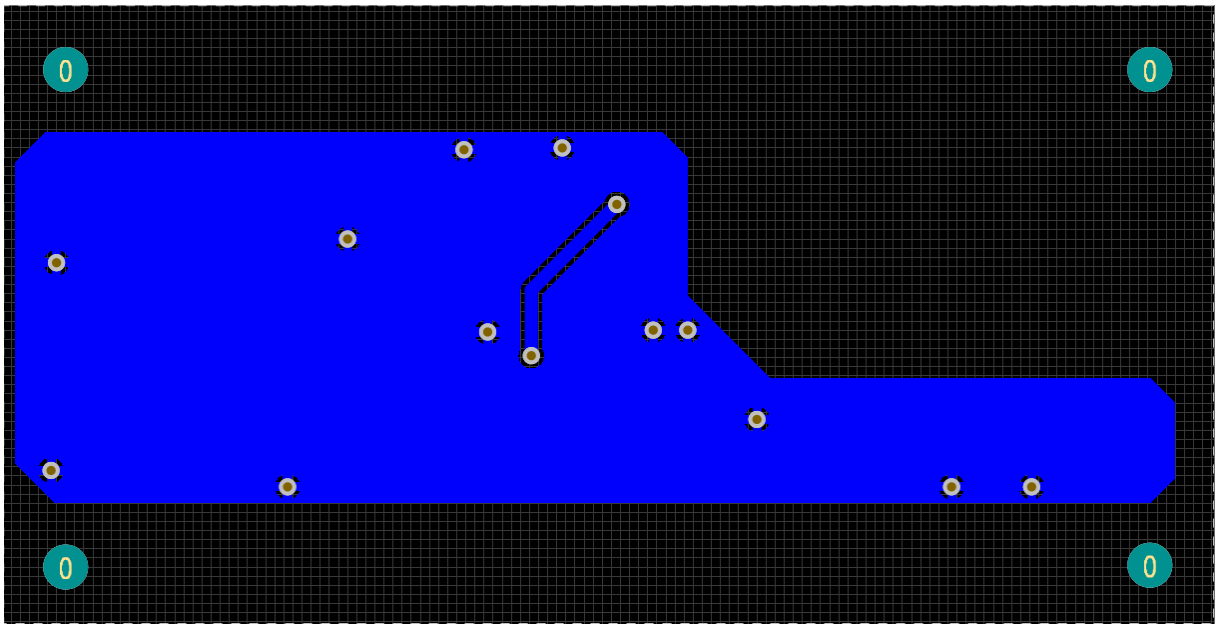

Figure 13. BOT Layer

Figure 14. BOT Overlay

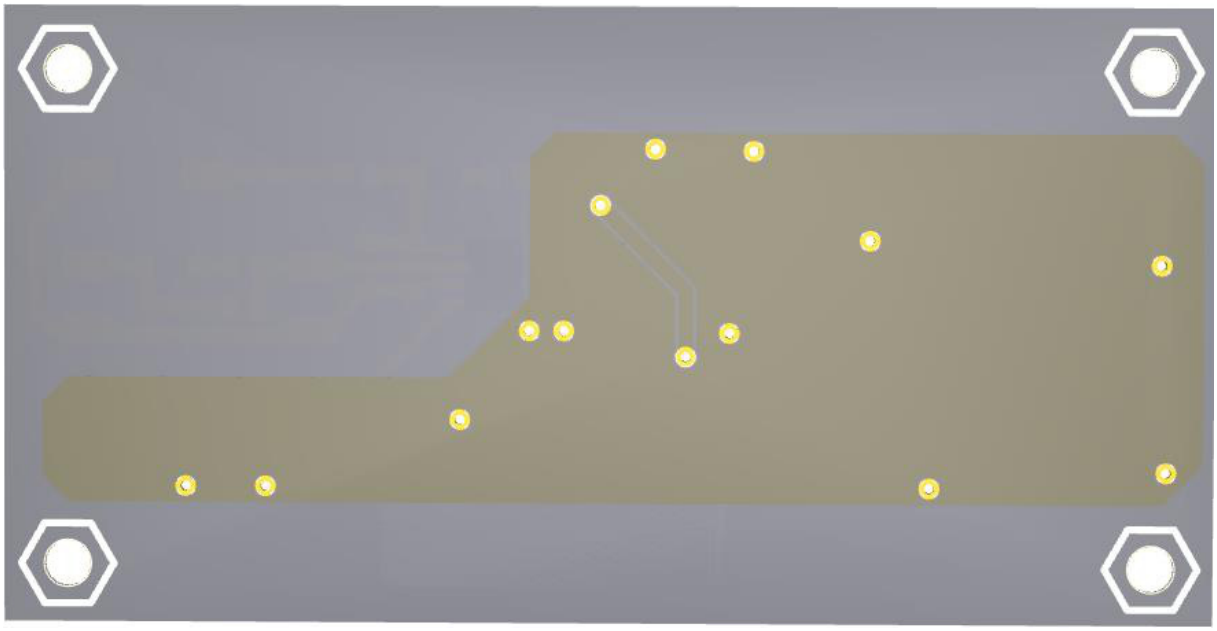

Figure 15. Assembled PCB BOT View

BOM

Table 4. BILL OF MATERIAL

Quantity	Assembled	Designator	Value	Description	Package	Manufacturer
1	YES	DR1	NCD57200	IGBT Driver	SOIC−8	ON Semiconductor
2	YES	D1, D2	MMSD301T1G	Schottky diode 30 V	SOD−123	ON Semiconductor
1	YES	D3	US1MFA	Super fast rectifier 1000 V	SOD−123 FL	ON Semiconductor
22	YES	TP1, ..., TP22		SMD test point		Harwin
1	YES	C1	47 μF / 35 V	Electrolytic capacitor	SMD radial d8x6.2	Panasonic
2	YES	C7, C8	33 p / 50 V	Ceramic capacitor	0805	Kemet
1	YES	C2	100 n / 50 V	Ceramic capacitor	0805	Kemet
1	YES	C3	10 μ / 35 V	Ceramic capacitor	0805	Murata
2	YES	C4, C9	10 μ / 35 V	Ceramic capacitor	1206	TDK
2	YES	C5, C6	100 n / 50 V	Ceramic capacitor	1206	Kemet
2	YES	C10, C11	1 n / 50 V	Ceramic capacitor	0805	Kemet
2	YES	R5, R10	49R9	Resistor	0805	Vishay
3	YES	R1, R2, R3	2R2	Resistor	0805	Vishay
5	YES	R4, R6, R7, R8, R11	0R	Resistor	0805	Vishay
4	YES	SP1a, SP2a, SP3a, SP4a	M3x10	plastic spacer		Duratool
4	YES	SP1b, SP2b, SP3b, SP4b	M3x10	plastic screw		Duratool
1	YES	Part Number 1	paper sticker 10x25 mm	DR1 part number and EBR specification		
1	YES	PCB	RA0003EB_0	PCB	43x85 mm	any
1	NA	Q1	BSS138	N−mosfet 50 V/220 mA	SOT−23−3	ON Semiconductor
1	NA	R13	10k	Resistor	0805	Vishay
1	NA	R12	120R	Resistor	0805	Vishay
2	NA	R9, R14	20k	Resistor	0805	Vishay

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