NCP13992UHD300WGEVB

GaN Based Ultra-high Power Density Adapter 300 W

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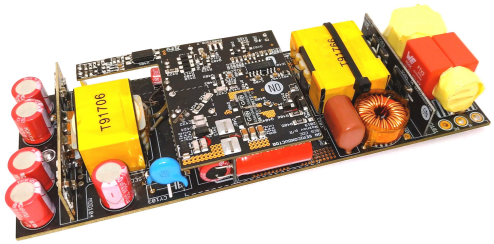
EVAL BOARD USER'S MANUAL



Description

This evaluation board user manual describes implementation of the 300 W Ultra−high Power Density Adapter and its main parameters; efficiency, no−load input power consumption, transient responses, EMI signature etc. The evaluation board demonstrates ON Semiconductor's high performance controllers, drivers and discrete semiconductor content capabilities that enable efficient UHPD designs implementation. This reference design includes the Synchronous PFC boost converter which is operating in the Discontinuous Conduction or Critical Conduction Mode (DCM/ CrM) depends on loading and LLC power stage with secondary side synchronous rectification. The PFC front stage is driven by NCP1616 controller, which assures unity power factor and low input current THD. Synchronization of the PFC boost SR switch is secured by the NCP4306 high performance SR controller. The LLC stage operates at 500 kHz switching frequency while nominal load is applied. Power stage is managed by the NCP13992 high performance current mode LLC controller. Thanks to the GaN High Electron Mobility Transistors (HEMT) implemented in both power stages at primary side, the high efficiency is easily maintained despite that system operates at high frequency. GaN Systems' GS66504B are incorporated as primary side power switches. Synchronous rectifier (SR) stage used in the secondary side composes from NCP4306 and two paralleled 60 V power MOSFETs for each branch. SR MOSFETs and controllers are implemented on the dedicated SR MODULE daughter card to ease main power board PCB design and to achieve maximum efficiency. Ultra−high power density is achieved thanks to the modular design, used controllers/ drivers, GaN HEMT and dedicated power magnetics design. This evaluation board manual focuses mainly on reference design description, adapter operation principles and connections. For more comprehensive information please refer to datasheets of individual parts that have been used.

Key Features

- GaN HEMT Based Design with Ultra−high Power Density Up to 32 W/inch^3
- Simple Two Layer PCB Design for all Board Modules
- 300 W Maximum Power with Peak Power Up to 340 W at Fixed Output Voltage 19 V
- Wide Input Voltage Range 90 – 265 V_{rms}
- Synchronous CrM PFC with using GaN HEMT
- 500 kHz LLC Stage Incorporated with 600 V HB GaN Driver and High Performance Current Mode LLC Controller
- Complies with CoC5 Tier2

Table 1. GENERAL PARAMETERS

Device	Applications	Input Voltage	Output Voltage / Current	V_{OUT} Ripple	I/O isolation
NCP51820 NCP1616 NCP13992 NCP4306 FAN3180 NCP431	Notebook adapter, TV power supplies	90 – 265 V RMS	19 V/ 16 A 18 A max	500 mV @ full load	Isolated
Efficiency	**Standby Power**	**Operating Temperature**	**Cooling**	**Topology**	**Board size**
see Figure 31 and Table 3	<150 mW @ 110 V_{rms} <150 mW @ 230 V_{rms}	0 – 50°C	Passive cooling* refer to Evaluation Demo−board Connections and Power−up and Test Procedure notes	Synchronous CrM PFC, LLC + SR	55 x 159 x 18 mm

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IMPORTANT NOTES

- GaN Based Ultra−high Power Density Adapter 300 W was designed as a trade−off between form−factor, efficiency, output voltage ripple, noise and protection features
- The maximum output voltage ripple is 550 mV pk−pk during skip mode operation (full load 500 mV pk−pk), due to implemented high efficiency skip mode. Additional post filter can reduce voltage ripple below 220 mV in skip operation range (full load < 120 mV pk−pk)
- For this design, the NCP13992 (the LLC Stage Controller) is implementing dedicated setup:
  - Fixed dead−time 80 ns with additional adjustment freedom via NCP51820, which enhancing dead−time to 110 ns
  - Output current is limited via auto−recovery FB−fault timer 100 ms, which is triggered at load above ≈18 A
  - Short−circuit protection enters to autorecovery fault after 5 consecutive pulses above 4.35 V at CS pin
  - Maximum on−time protection is activated when 2.7 μs on−time is exceeded, this results in autorecovery fault
  - Brown−out protection allows LLC Stage for an appropriate bulk voltage range
  - Over voltage protection may latch system; however it's not used in this demo−board
  - Over temperature protection latches controller in case of overheating, but to applying this feature, additional NTC resistor needs to be assembled
- This reference design has not been optimized for surge, lightning, etc
- It is recommended to consider additional thermal management especially at very low line voltage

MODULAR CONCEPTIONS

The demo−board is constructed using a modular system that composes from the MAIN BOARD (Figures 2, 3, 4, 5) and several daughter−card modules. Following daughter−cards are inserted into MAIN BOARD:

- BRIDGE RECTIFIER MODULE MOD101 (Figure 11, Figure 12)
- CBULK MODULE MOD102 (Figures 13, 14)
- LLC STAGE MODULE MOD103 (Figures 83, 16, 17)
- SR MODULE MOD104 (Figures 21, 22, 23)

Each module is indicated in schematic diagram in Figure 2 as MOD10x. Refer to Figure 1 for better understanding of assembly approach. Modular concept brings several advantages as versatility, possibility to test own daughter cards, easy design update, opportunity for checking functionality separated module and spare room for additional features. These allow the user to enhance experimenting with daughter−cards. Used type of construction helps to reduce PCB area, thus increases power density and also allows reducing number of PCB layers needed. All PCBs are designed as 2−layers with 70 μm copper plating for better thermal management. Also, the 70 μm copper helps to reduce conduction losses especially at secondary side which carries relatively high output current.

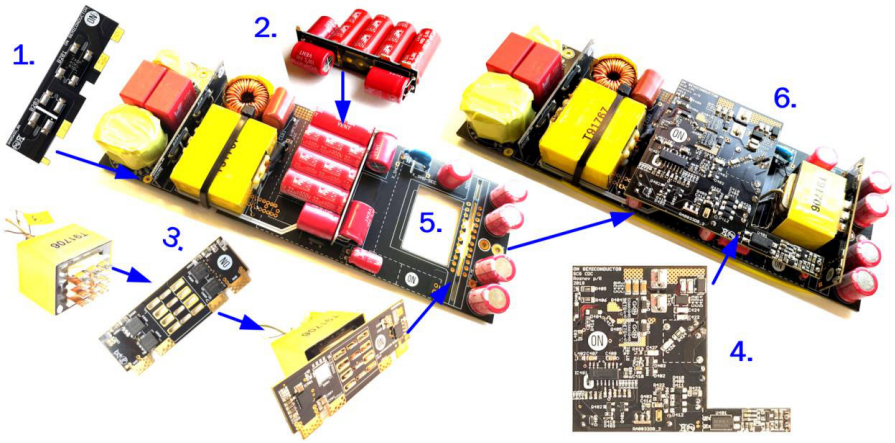


Figure 1. Photograph of Adapter Assembling Principle

Detailed Descriptions of the Evaluation Board

The MAIN BOARD is portrayed in first few figures; schematic diagram in Figure 2, PCB layout, assembly plan in Figure 3, Figure 4 and photographs in Figure 5. MAIN BOARD contains input/ output terminals, protection elements, EMI filter, synchronous PFC stage, output filter capacitors and slots or pins for inserting and connecting daughter card modules. It is also equipped with terminals needed for connecting of magnetic elements shielding as PFC inductor, LLC transformer and so on. MAIN BOARD is based on 1.8 mm width core PCB with 70 μm copper plating. 70 μm copper plating was selected in order to improve thermal management of the PFC stage power switches.

The MAIN BOARD is protected by the F101 5 A fast−acting type fuse on the input which is capable withstand the inrush current which is not significantly high, thanks to selected bulk capacitor capacitance. The varistor R101 serves as input overvoltage protection in case of distribution line voltage spikes or disturbances. A differential mode lighting surge protection has not been optimized in this board. The inrush current limiting element as NTC thermistor is not used, see the schematic diagram in Figure 2. In case that higher bulk capacitor capacitance is

necessary, for instance for longer hold−up time, then the fuse properties and inrush NTC resistor should be considered. *The EMI Filter* consists from several components which are described further. The common−mode power line chokes L102 and L101 reduce common mode noise in low–middle frequency band and higher frequency band respectively. L102 has implemented shielding to avoid noise coupling from PFC stage. The differential EMI noise in lower frequency region is limited by differential capacitor built from C101 and C102. Three Y−capacitors CY101 – CY103 are intended to minimize the common−mode noise. CY103 usually attenuates the lowest frequency band. The input terminal PE is connected together with output ground terminal. Connection is done via copper wire with diameter 1.5 mm and it has two purposes. First goal is safety grounding and second reason is creating short and low impedance path for EMI filter to reduce EMI noise. PFC stage pre−filter is arranged from polypropylene capacitor C103 and differential mode inductor L104. Pre−filter mainly resolves noise that comes from commutation charge of PFC power stage to input side of EMI filter and thus helps to further EMI signature reduction. *The PFC Front Stage* implements critical conduction mode PFC boost converter with active synchronization of boost diode i.e. synchronous rectification. All elements needed to build PFC front stage are located on MAIN BOARD except to bridge rectifier and bulk capacitor. The PFC front stage (Figure 2) consists of below mentioned parts. BRIDGE RECTIFIER MODULE MOD101 (Figure 11, Figure 12) is replacing standard bridge rectifier device. The controller NCP1616 IC103 is the “brain” which is managing PFC stage. The CBULK MODULE MOD102 (C301−307 in Figure 7, Figure 8) serves as energy storage bank. The MAIN BOARD’s local high−frequency decoupling is made of multi−layer ceramic capacitors (MLCC) C114, C116, C118 and C120. Capacitors improve EMI signature thanks to covering commutation charge caused by PFC power stage transitions. The inrush diode D108 creates alternative path for initial bulk capacitor charging. Also it reduces boost diode D111 current stress in case connection to distribution line or line interruption. The sensing shunt composed of R121, R125 and R128 which set maximum peak current flowing through inductor and power switches. The NCP1615 IC103 senses inductor current directly as a voltage drop at shunt via R119 at combined CS/ZCD pin. The PFC inductor L105 features auxiliary winding that is intended for zero current detection (ZCD). Voltage from auxiliary winding is rectified by D106. This signal is divided by resistors divider R109, R119 connected to NCP1616 CS/ZCD pin which guarantees zero current sensing and detects power switches drain voltage valleys. The PFC GaN HEMT power switches GS66504B Q106−7 from GaN Systems are used instead of standard Silicon MOSFETs. The driver FAN3180 IC102 drives PFC power switches, driver uses local decoupling capacitor C108. Driving slope is set by D110, R117, R120 and R124. The driver voltage pre−regulator is made of Q101, R102 and D103. Simple driver supply filter L103 and R114 is implemented to reduce HF current flowing from auxiliary supply. The bulk voltage divider R132, R133, R134, R135, R136, R137, R138 with filtering capacitor C119 is connected to the FB pin of PFC controller. This information is used for bulk capacitor voltage regulation and protection purposes. The boost diode D111 is rectifying current delivered from PFC inductor L105 after power switches are turned−off. The synchronous switch Q105 GS66504B reduces conduction losses of D111 especially at higher output power levels. The synchronous switch driver IC101 is implemented with NCP4306 with 5 V driver voltage clamp option. Its local decoupling is done by ceramic capacitor C109. 200 V CS pin voltage range is enhanced with MOSFET Q104. Supply voltage for IC101 is bootstrapped through diode D104 with option for higher boot voltage via R106 or lower voltage level R107. Supply voltage for IC101 is prepared after several switching cycles of power switches. PFC controller necessary compensation circuitries and components are located very close to controller itself. PFC Stage over temperature protection (OTP) is based on SMD NTC resistor R126 which is y located close to the power switches. *The HV Start−Up, Brown−Out and X2 Discharge Capability* – both primary controllers are equipped with High Voltage Start−up current sources (NCP1616, NCP13992). The NCP1616 (IC103) has an integrated high voltage start−up circuit accessible by the HV pin. The start−up circuit is rated at a maximum voltage of 700 V. A start−up regulator consists of a constant current source that supplies current from a high voltage rail to the supply capacitors (C105, C106, C107) on the VCC pin. The internal high voltage start−up circuit eliminates the need for external start−up components and thus helps to reduce no−load power consumption. Once supply capacitors are charged to the start−up threshold, the start−up current is disabled and the controller operation is enabled. The start−up regulator remains disabled until V_{CC} falls below the lower supply threshold. Once reached, the PFC controller is disabled reducing the bias current consumption of the IC. The controller is also disabled once a fault is detected. Operation is then restarted again when VCC reaches $V_{CC(on)}$ or after all non−latching faults end. The supply capacitor provides power to the controller during power up. The HV pin has additional features and provides access to the brownout and line voltage detectors. The brownout detector detects mains interruptions and the line voltage detector determines the presence of either 110 V or 220 V AC mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance. The HV pin also offers X2 capacitor discharge feature. The X2−capacitor is discharged after disconnecting power cord from the distribution line socket. The HV pin connection to input (AC) side of adapter is assured via serial circuit R103, R105, R108, and two diodes D101 and D102 (Figure 2). *The Output Filter* is built from the polymer electrolytic and ceramic capacitors C122−131, which are located on the MAIN BOARD to support easy PCB design. Polymer electrolytic capacitors were selected to handle high AC output current ripple and suppress output voltage ripple. Ceramic capacitors reduce ripple at high frequency range (above 1 MHz) at which impedance of electrolytic capacitors is relatively poor or can have inductive character. It should be noted that output filter capacitor bank is fed from SR MODULE MOD104 which is soldered directly on the secondary transformer turns.

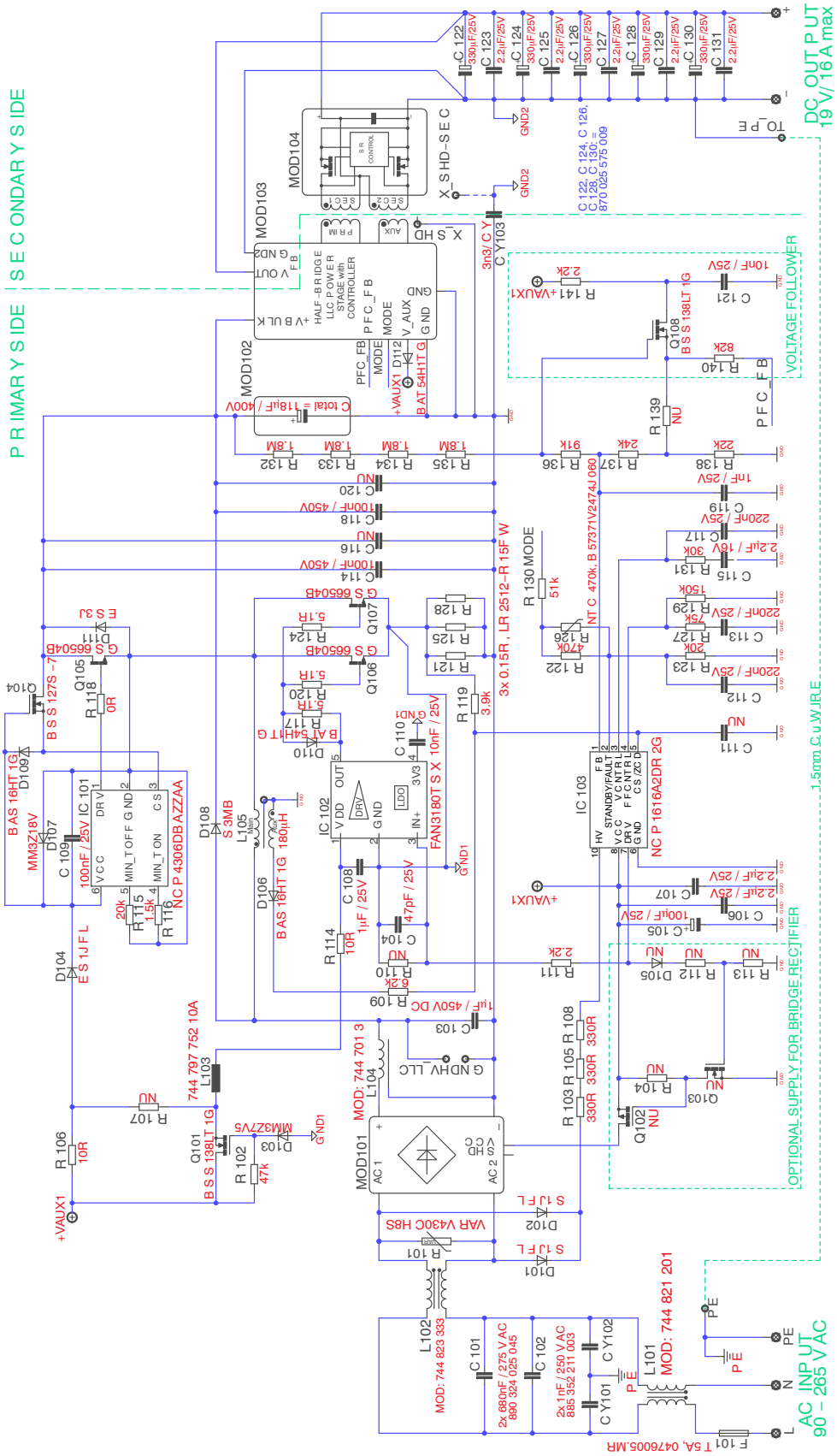


Figure 2. Schematic Diagram of MAIN BOARD

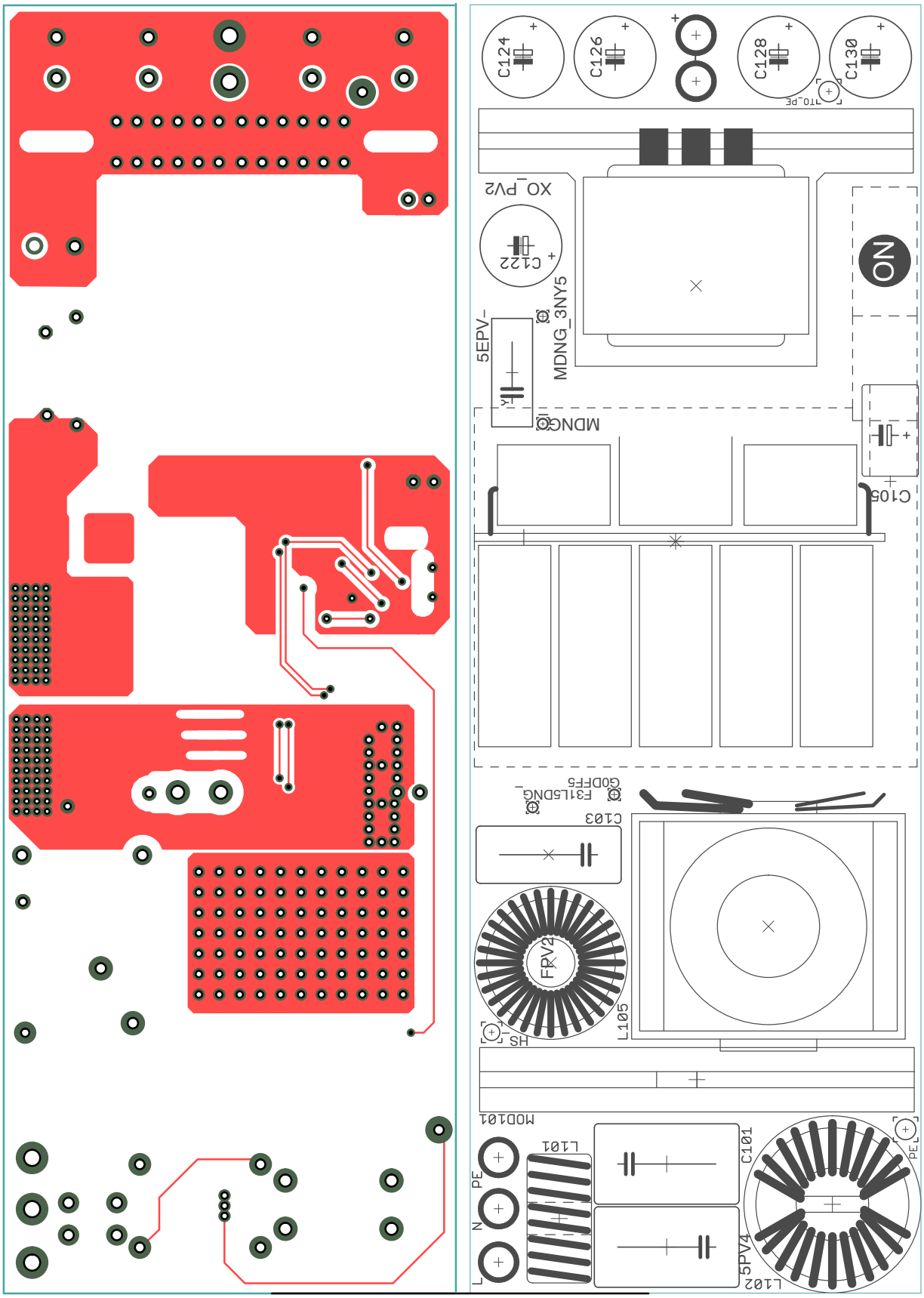


Figure 3. Top Layer PCB Layout and Assembly Plan of MAIN BOARD

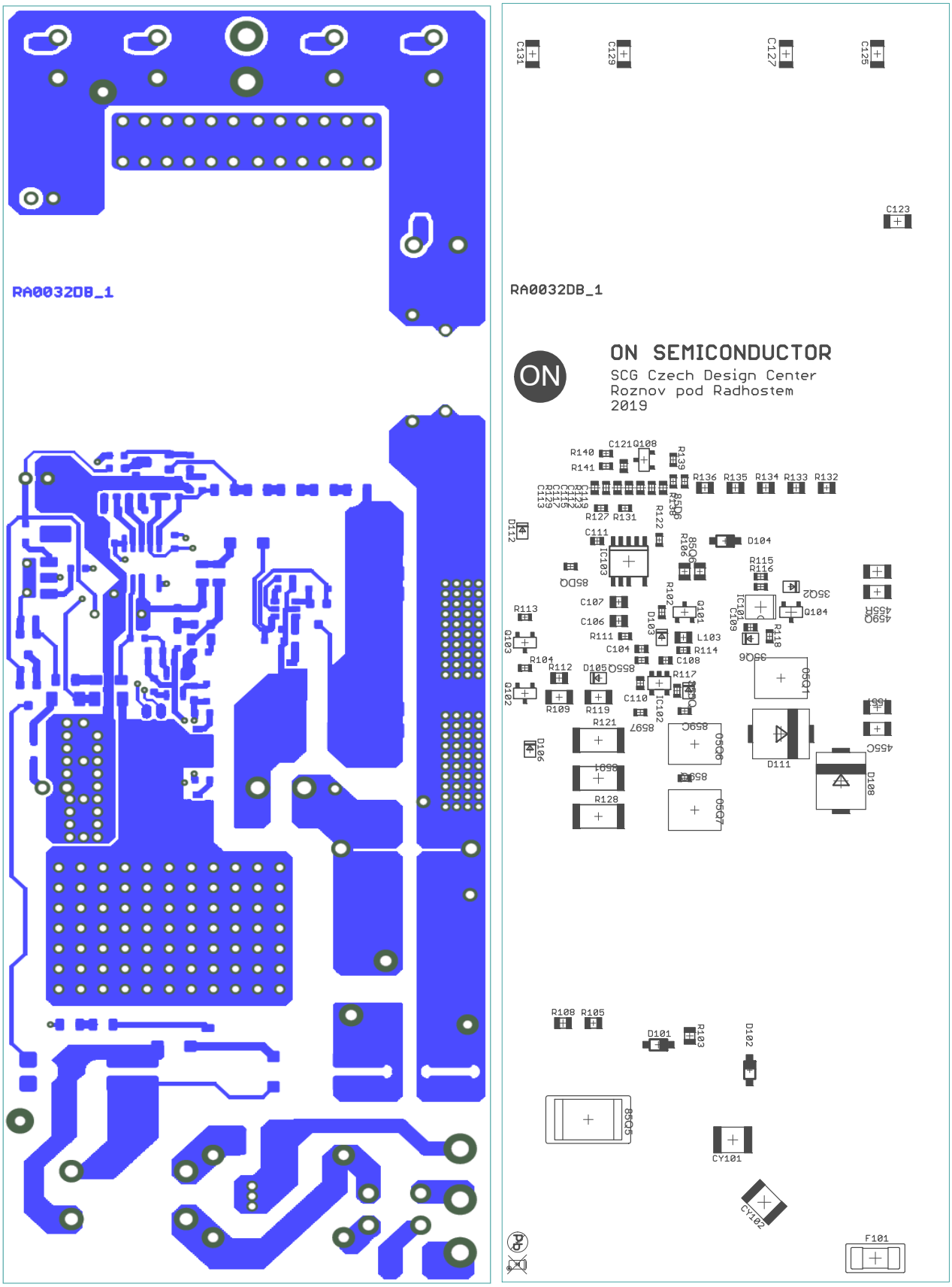


Figure 4. Bottom Layer PCB Layout and Assembly Plan of MAIN BOARD

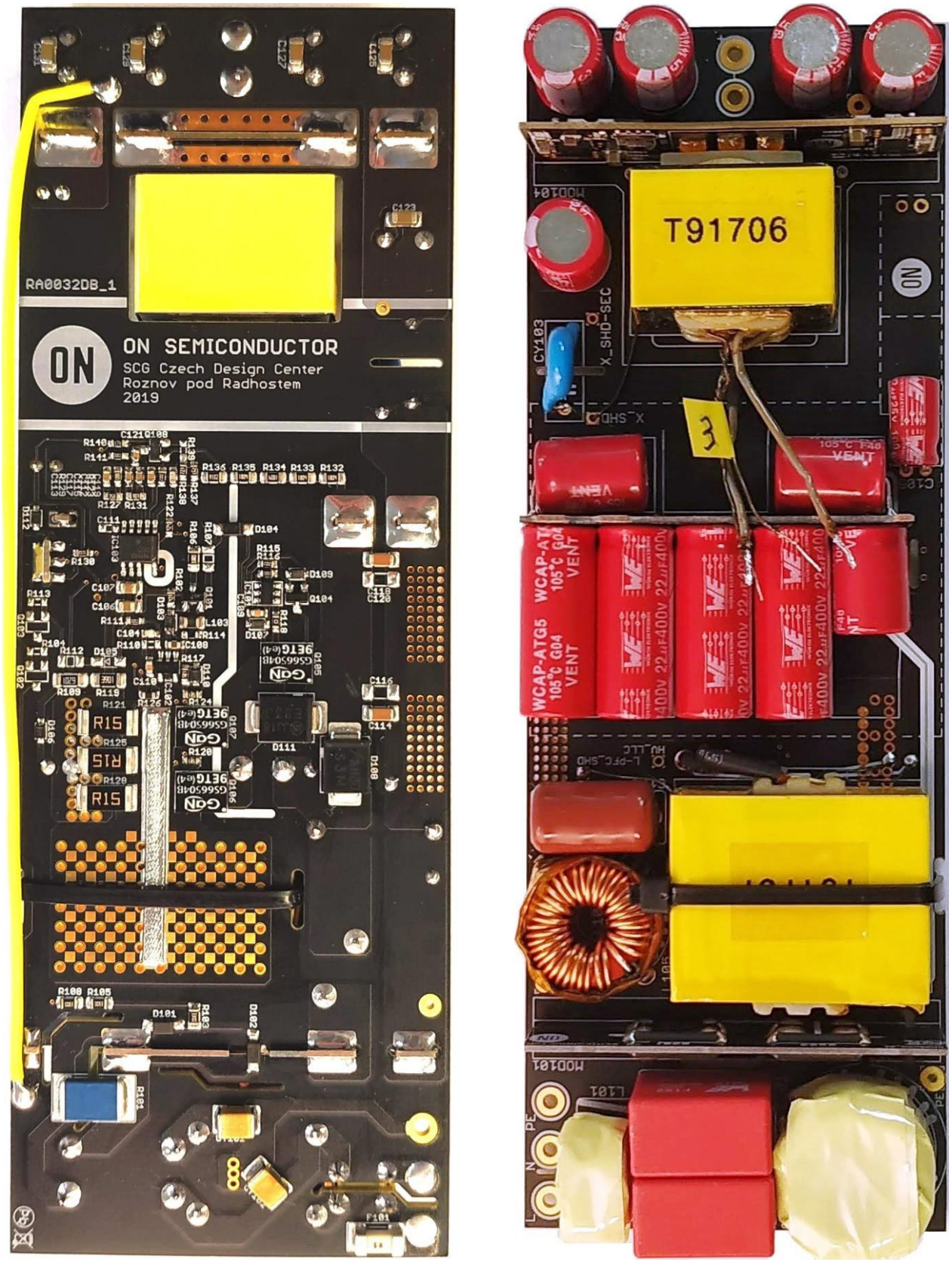


Figure 5. Photographs of MAIN BOARD

GaN HEMT based Power Stage application requires several design rules to be met to secure proper and reliable system operation. It should be realized such way that power loop inductance is as small as possible. The optimum solution for loop inductance reduction is the flux cancelation loop technique. Usage of this technique results in lower stored inductance energy, so voltage spikes at the drain of GaN power device becomes lower. Refer to Figure 6 in which flux cancelation loop example is depicted. Power stage main devices are placed in one line to reduce area of the power loop and easily prepare space for ground return path. Compact placement also improves EMI performance.

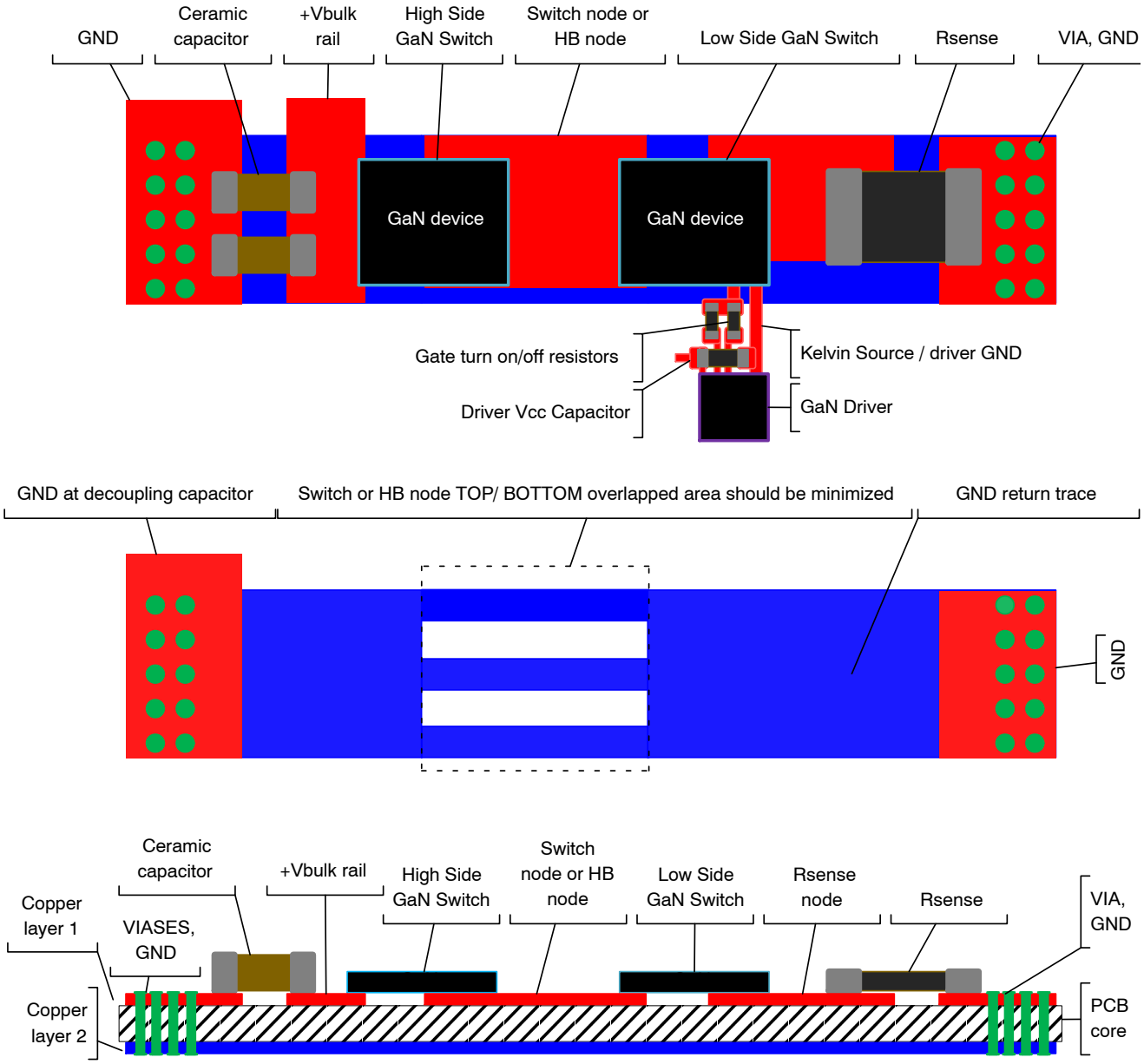


Figure 6. GaN HEMT Power Stage Design Principle

The example provided in Figure 6 is a simple half−bridge stage with sensing shunt resistor connected to the source of low side switch. Resistor is necessary for positive type of current sensing and limitation. It can be omitted in case that is not needed and the return ground should be connected to the source of low side switch. Ground return trace should be routed from low side switch source to decoupling capacitor ground, directly under GaN devices such way that overlapped area between switching node and return ground is minimized, see Figure 6 again. This reduces parasitic capacitance created at switching node and possible noise coupling. Ground return trace beginning and end are interconnected through multiple vias. Because used GaN HEMT devices are cooled through source pad, the cooling area should be considered and projected according to generated losses. In generally, removing heat from GaN

device is advanced topic which is not focus of this manual and for more information refer to GaN Systems' part datasheet and related application notes. Half−bridge stage needs to be decoupled with a high voltage ceramic capacitor which should be close to high side switch drain to maximize its decoupling effect. Power stage is supplied directly to ceramic capacitor from main energy storage, usually bulk capacitor, which shouldn't be too far from the power stage. It is recommended to use at least 100 nF decoupling capacitor to handle energy stored in power loop inductance during transition states and also energy stored in power rails inductances. Lower value capacitance capacitor is not usually robust enough solution and can't receive energy stored in stray inductances and thus may be destroyed due to overcharging after appeared transition phenomenon. Simplifying, decoupling capacitor acts two ways, once is covering commutation charge of power stage, secondly it works like a snubber and dumps voltage spikes. Both effects improve EMI performance. For real PCB layout implementation of synchronous PFC stage refer to figure Figure 7 – device indexes correspond with schematic in Figure 2.

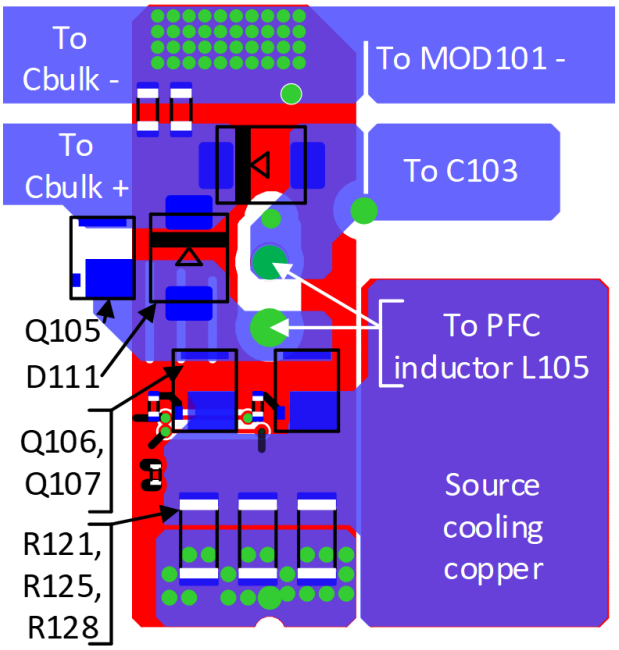


Figure 7. PCB Layout Implementation of Synchronous PFC Stage

GaN HEMT Gate driving consideration

GaN HEMT exhibit with very low parasitic capacitances/ inductances and different current conduction mechanism compare to standard silicon MOSFET. Thank to these, such device can achieve multiple times higher switching speed and significantly better total power losses performance. On the other hand ruggedness is worse compare to standard silicon MOSFET. GaN HEMT gate capacitance is usually ten times lower compare to standard MOSFET, so it's easier to destroy GaN device with improper handling and design. Thus, careful design is very important to maintain reliable and safe operation. Proper implementing includes not only power stage (which also influences driving loop), but also very important is gate drive circuit itself. Simple example is proposed in upper part of Figure 6. Driver should be located as close to GaN HEMT device as possible to reduce loop length and thus driving loop inductance. Both driving traces need to be very close to each other. It is also advantageous to use same technique for the driving loop as for the power loop (flux cancelation loop). For smooth turn−on process, free of any ringing, it is desirable to place driver decoupling capacitor at driving ground. This further reduces ground trace inductance via which is charging loop closed. Driver ground pin must be connected to a dedicated kelvin−source pad of the GaN HEMT device. If the GaN HEMT device doesn't have a dedicated kelvin−source pad, then it is preferred to join driver ground to point of source pad through which minimum current is flowing. Such connection secures smallest influence of power current loop on the driving process.

Design Tips for PFC Controller NCP1616

When PFC controller NCP1616 is going to be incorporated, several design recommendations should be taken into account to avoid unexpected or noisy performance. Vcc decoupling capacitor should be sited next to the Vcc and GND pins as demonstrates Figure 8. Controller ground should be split into so call "quiet ground" and driving/ R_{sense} ground. Splitting point should be located very close to controller GND pin. It's recommended to use quiet ground for connecting compensation elements and PFC feedback divider circuitries. Driving or R_{sense} ground should be directly connected to current sensing shunt resistor. Because current sense (CS) and zero current detection (ZCD) features are available at shared CS/ZCD pin via divider it's reasonable to connect ZCD winding beginning to R_{sense} ground. Bulk voltage or PFC feedback divider is typically built from several resistors due to safety reason. To keep good noise immunity it is important to use careful feedback divider placement, which should be far away from high dV/dt signals. In simple words it should be separated from high voltage switching nodes. Divider can be also shielded by copper polygon connected to quiet ground for further improvement. For the supply voltage distributing to surrounding or auxiliary circuitries use star connection technique and properly select distributing point based on current flowing to various loads. Distributing points are usually located near to the decoupling capacitors. In case of use external driver, especially high speed switching driver, it's important to implement filter inductor into Vcc supply line or at least few unit ohms resistor. This decreases high frequency currents flowing into Vcc supply line and also separates Vcc decoupling capacitors, which tend to cover charge each other in case of low supply line impedance.

Afore mentioned practices minimize noise injected into all controller pins and secure stable operation.

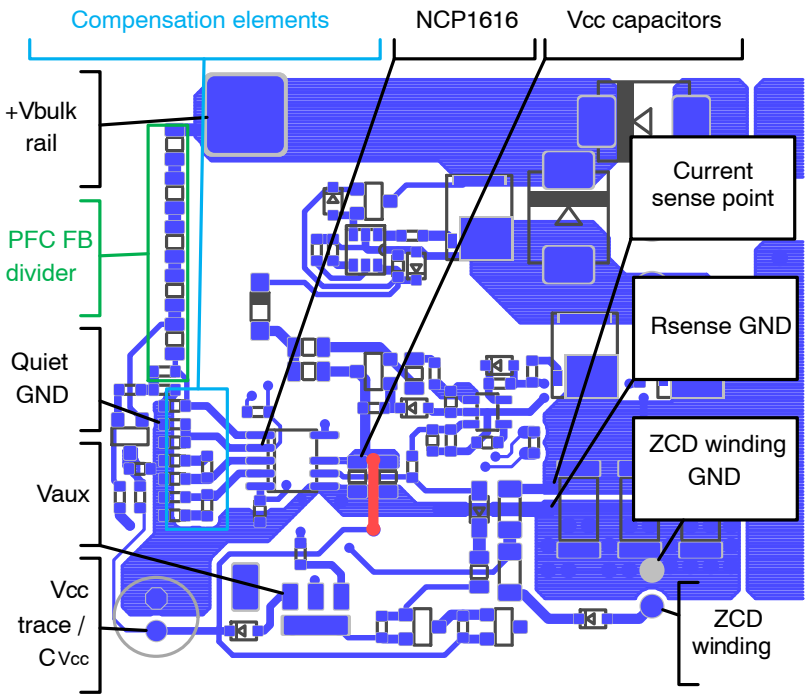


Figure 8. NCP1616 Recommended Connection Example

Design Tips for SR Driver NC4306 in High Voltage Application

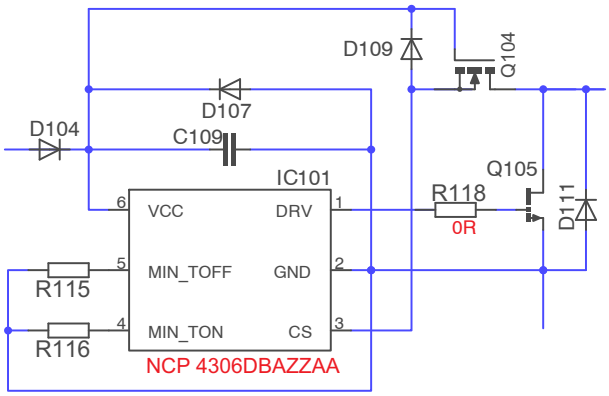
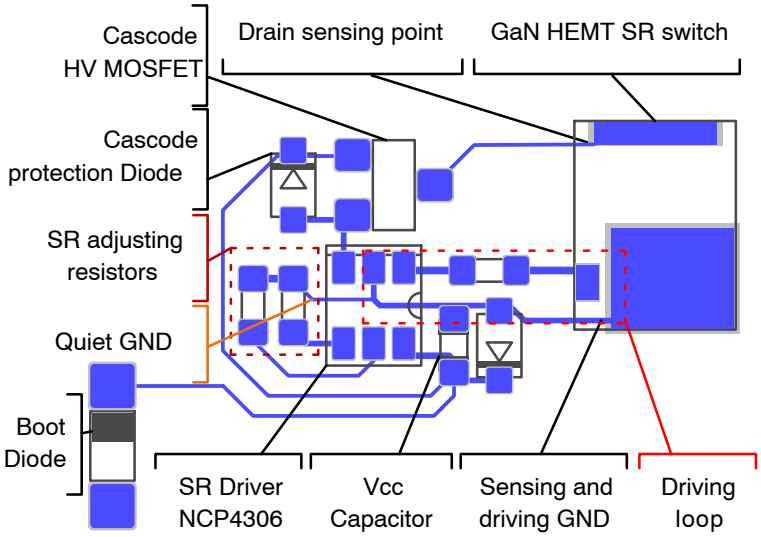


Figure 9. Schematic Diagram of HighVoltage Synchronous Rectifier using NCP4306

The NCP4306 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its features and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and resonant LLC converter. The combination of externally or fixed adjustable minimum off−time and on−time blanking periods help to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise free operation of the SR system is insured due to the Self Synchronization feature. The NCP4306 also utilizes Kelvin connection of the driver to the SR MOSFET to achieve high efficiency operation at full load and utilizes the light load detection architecture to increase efficiency at light load conditions. The precise turn−off threshold, extremely low turn−off delay time and high driver sink current capability allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency. The high driver clamp voltage accuracy (5 V) enables the use of GaN HEMTs. The NCP4306 was designed to be used as secondary side controller for maximum CS pin voltage of 200 V. To enhance input voltage range the cascode MOSFET Q104 was implemented, see detailed schematic diagram in Figure 9. Cascode MOSFET clamps maximum input voltage to level $V_{cc} - V_{th_Q104}$. Because PFC stage is based on GaN HEMT devices, it can achieve very high dV/dt slopes. To guarantee that cascode clamp stays stable during transition small switching diode D109 has been used. This diode doesn't allow Q101 source runaway to high voltage and thus protects IC101 CS pin against overvoltage. Further protection which makes HV SR application stable is Zener Diode D107. In case that supply voltage would rise, D107 will clamp it to 18 V. Despite that the synchronous PFC stage is implemented, the boost diode is still mandatory to avoid Q105 thermal runaway due to its high reverse conduction voltage drop, particularly while no driving pulses are made by IC101. Driving pulses are not present whilst PFC stage is in start−up process or when switching burst is initiated. As aforementioned, some minimum number of switching cycles must be taken to generate supply voltage for IC101.

To incorporate HV SR PCB layout design using NCP4306 and GaN HEM device following considerations should be followed. PCB layout design example is illustrated in Figure 10. This layout is implemented in MAIN BOARD. In generally, GaN HEMT devices require always the same practice as is mentioned in previous sections. Simplifying,

the driver location is next to GaN HEMT device as physical or manufacturing dimensions allows it. Driving traces should be tied closely together. Use a GaN HEMT dedicated kelvin−source pad or separated source trace, to avoid influence of power loop current to connect driver ground. Driver Vcc decoupling capacitor should be placed on driving ground trace, next to Vcc pin. NCP4306 parameters adjusting pins need to use quiet ground separated from driving ground, see Figure 10 below. Drain sensing point is selected left−down in the drain pad corner i.e. place which is far away from main current path. Cascode protecting diode D109 is positioned close to the cascode MOSFET Q104. Bootstrap diode trace to Vcc decoupling capacitor is separated from others and cannot be merged with Vcc traces for supporting circuitries.



NOTE: Trace widths were reduced for explanation purpose in order to clearly display each device connecting path. Appropriate trace widths has to be used in final design, especially for Vcc and driving loops which carry high current peaks and need to have low impedance to keep GaN HEMT device properly turned−on or off.

Figure 10. NCP4306 & GaN HEMT as Synchronous Switch Design Example

BRIDGE RECTIFIER MODULE MOD101

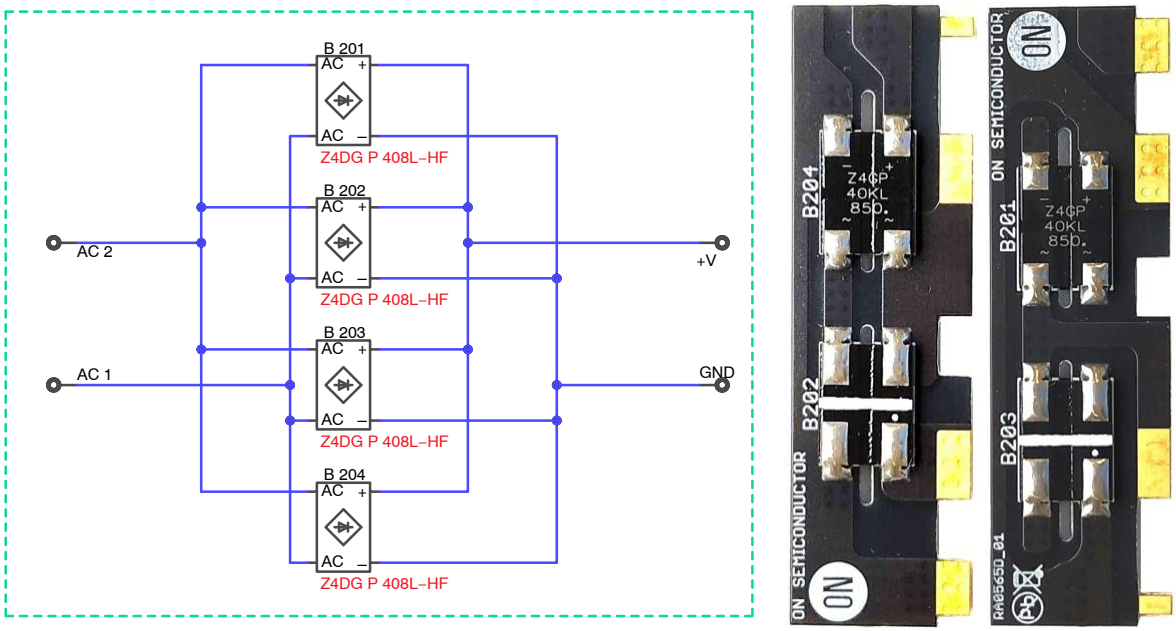


Figure 11. Schematic Diagram of BRIDGE RECTIFIER MODULE MOD101 and its Photographs

BRIDGE RECTIFIER MODULE MOD101 schematic diagram, photography and PCB layout are revealed in Figure 11 and Figure 12. This module is built from 4 pieces of small SMD bridge rectifiers that support both sides assembling, which easies PCB layout design. Main idea is to create versatile module, which can be replaced with semi−synchronous bridge rectifier module or even more advanced a fully synchronous bridge rectifier module if higher efficiency is required. Addition benefit of this design approach is reduced PCB area needed than routing interconnection for standard bridge rectifier.

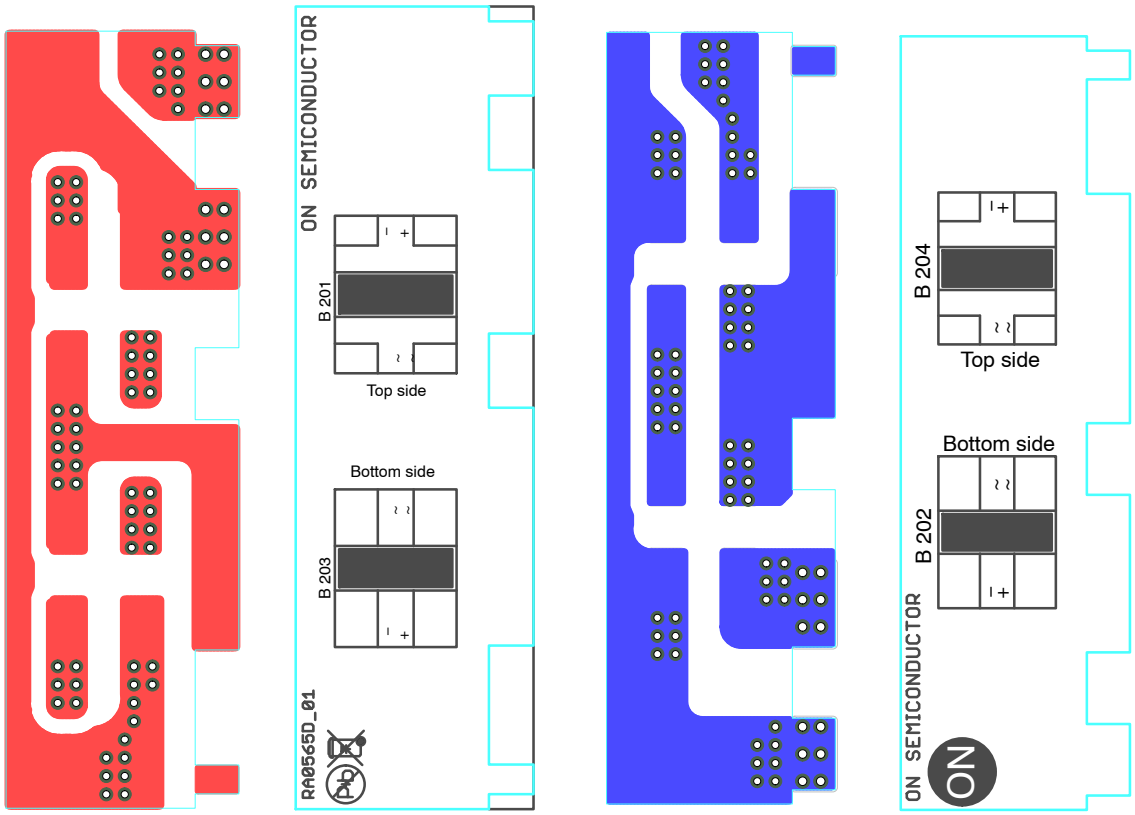


Figure 12. Top/ Bottom Layer PCB Layout and Assembly Plan of BRIDGE RECTIFIER MODULE MOD101

The semi−synchronous bridge rectifier module based on FCMT099N65S3 and NCP4306 was developed and tested. The FCMT099N65S3 is a 650 V SUPERFET III MOSFET with typical 87 mΩ on−state resistance, which is housed in a Power88 package. This very small package (8 x 8 mm) offers excellent power density that is suitable for this design. The semi−synchronous bridge rectifier design is out of scope of this user manual, but for reference few facts from real measurements are showed in Table 2. Maximum efficiency improvement reached with semi−synchronous bridge rectifier was +0.5% and in best case up to 1 W of losses were saved. Mentioned results are valid for specific configuration which was used and can differ in other arrangement.

Table 2. STANDARD BRIDGE RECTIFIER VS. SEMI−SYNCHRONOUS BRIDGE RECTIFIER COMPARISON

Output power level	Input voltage [V AC]	Standard bridge rectifier		Semi−synchronous bridge rectifier		Semi−synchronous improvement	
		Total effieciency [%]	Total power losses [%]	Total effieciency [%]	Total power losses [%]	Efficiency increase [%]	Power losses recudtion [W]
152 W	90	93	11.46	93.5	10.6	0.5	−0.86
	115	93.99	9.75	94.33	9.15	0.34	−0.6
	230	95.15	7.76	95.32	7.47	0.17	−0.29
210 W	90	92.49	17.01	92.92	15.96	0.43	−1.05
	115	93.81	13.82	94.13	13.06	0.32	−0.76
	230	95.39	10.14	95.56	9.74	0.17	−0.4
286 W	90	90.49	30.05	90.74	29.17	0.25	−0.88
	115	93.11	21.15	93.34	20.39	0.23	−0.76
	230	95.19	14.43	95.34	13.96	0.15	−0.47

The CBULK MODULE MOD102 is shown in Figure 13 and Figure 14 serves as energy storage bank which saves energy delivered from PFC Stage and provides it for LLC Stage. Main design strategy for this module was to simplify MAIN BOARD (MB) PCB layout, which moved capacitors soldering pads from MB. It also prepares room for power switches, creates interface for LLC Stage module and overall minimizes system volume.

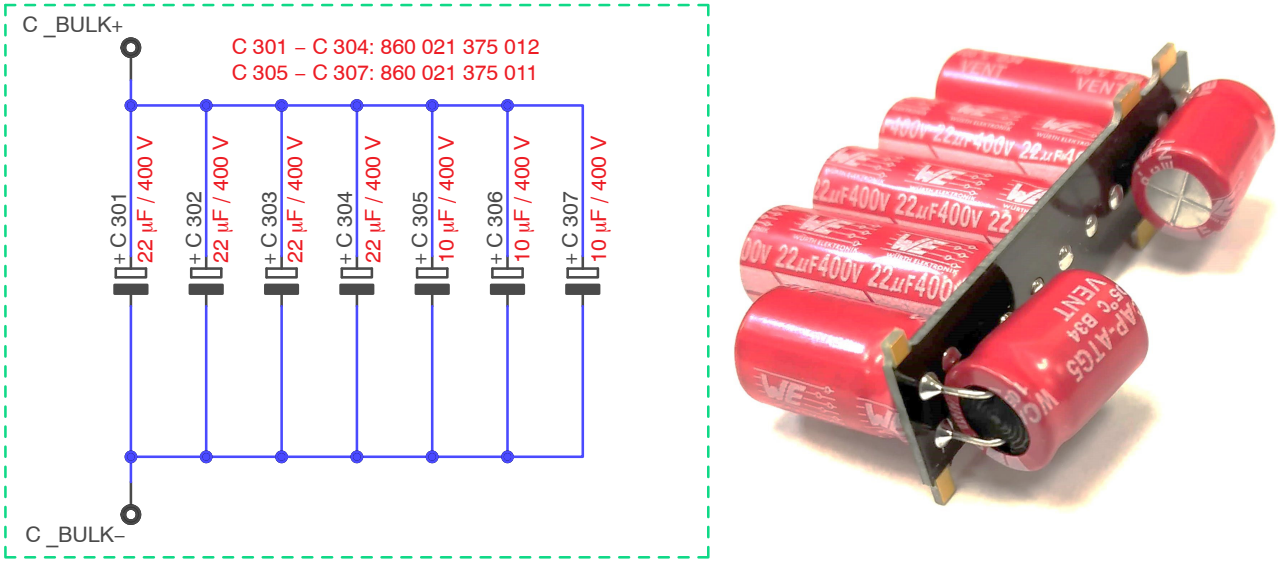


Figure 13. Schematic Diagram of CBULK MODULE MOD102 and its Photograph

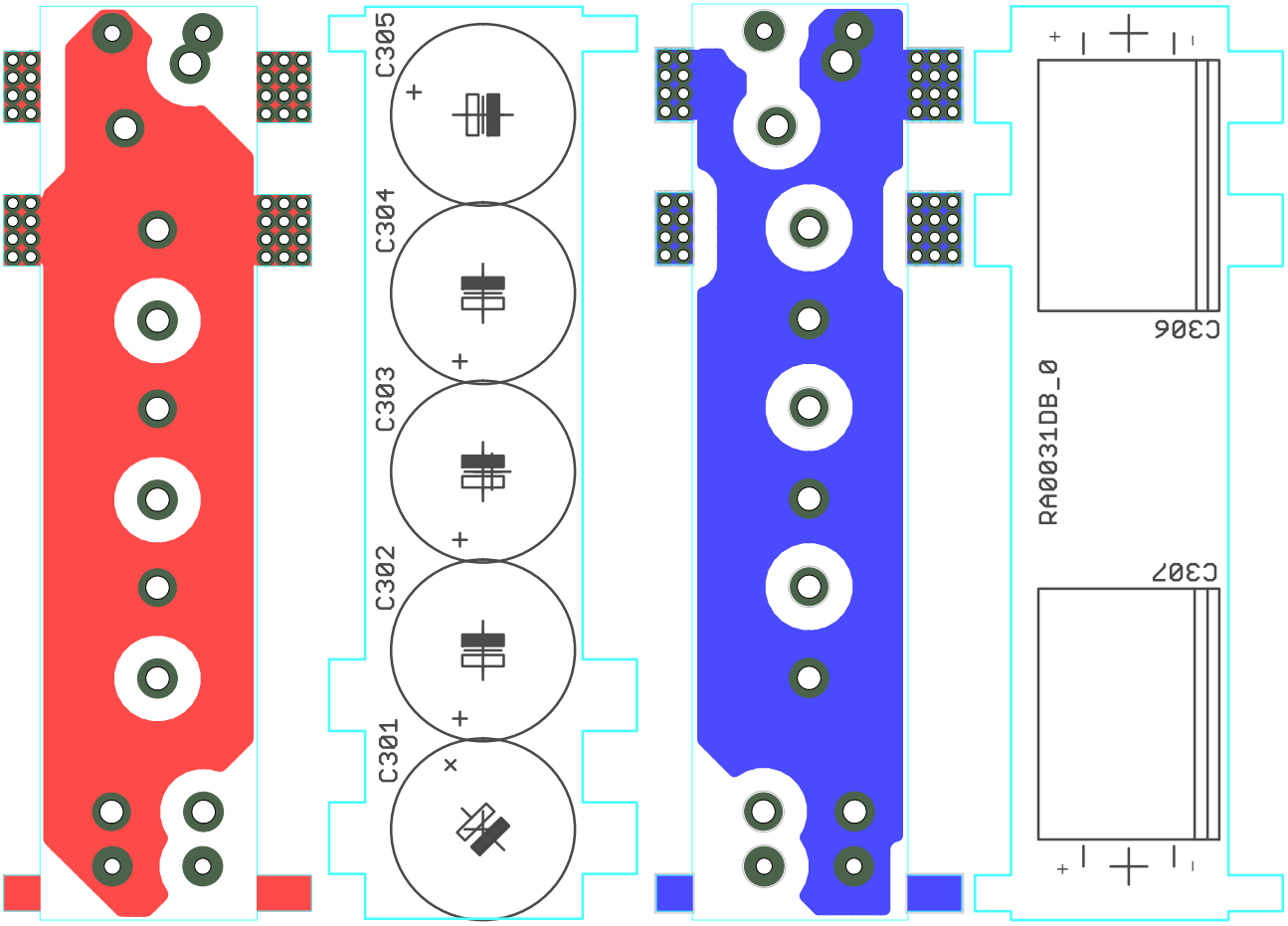


Figure 14. Top / Bottom Layer PCB Layout and Assembly Plan of CBULK MODULE MOD102

LLC STAGE MODULE MOD103 is displayed in Figure 83, Figure 16 and Figure 17. Module is constructed in such a way that it contains everything needed for LLC stage primary side implementation. LLC STAGE MODULE is based on NCP13992 IC401, NC51820 IC402 and GaN Systems' GS66504B Q404−405. Module also contains optocoupler U401 and shunt regulator NCP431 IC403 which insure output voltage regulation, see schematic diagram in Figure 83.

The primary side of LLC power stage is formed by half−bridge configured from switches Q404−405. Diodes D404 and D407 are used in parallel with power switches. Diodes help to reduce conduction losses during dead time period and protect power switches while system is in start−up process and higher operating current is present. Half−bridge is decoupled using ceramic capacitors C419, C420 and C421. Resonant tank composed of discrete resonant inductor L404, resonant capacitors C422−425 and transformer X501. Resonant capacitors are based on NP0 or C0G dielectric material. This material is very stable with frequency, voltage and temperature. Other ceramic capacitors material is not recommended. Diodes D413−414 clamp resonant capacitor voltage swing to bulk voltage level and protect resonant capacitors against overvoltage stress. Resonant inductor is built on RM5 core with shielding connected to half−bridge stage ground. The LLC transformer X501 is connected to LLC STAGE MODULE through flying wires. LLC transformer was designed as hybrid type. The primary winding as well as auxiliary winding is made from triple insulated wires, which secures insulation and safely separates secondary side from primary side. Secondary windings are created from copper plates, which are soldered directly to the SR MODULE.

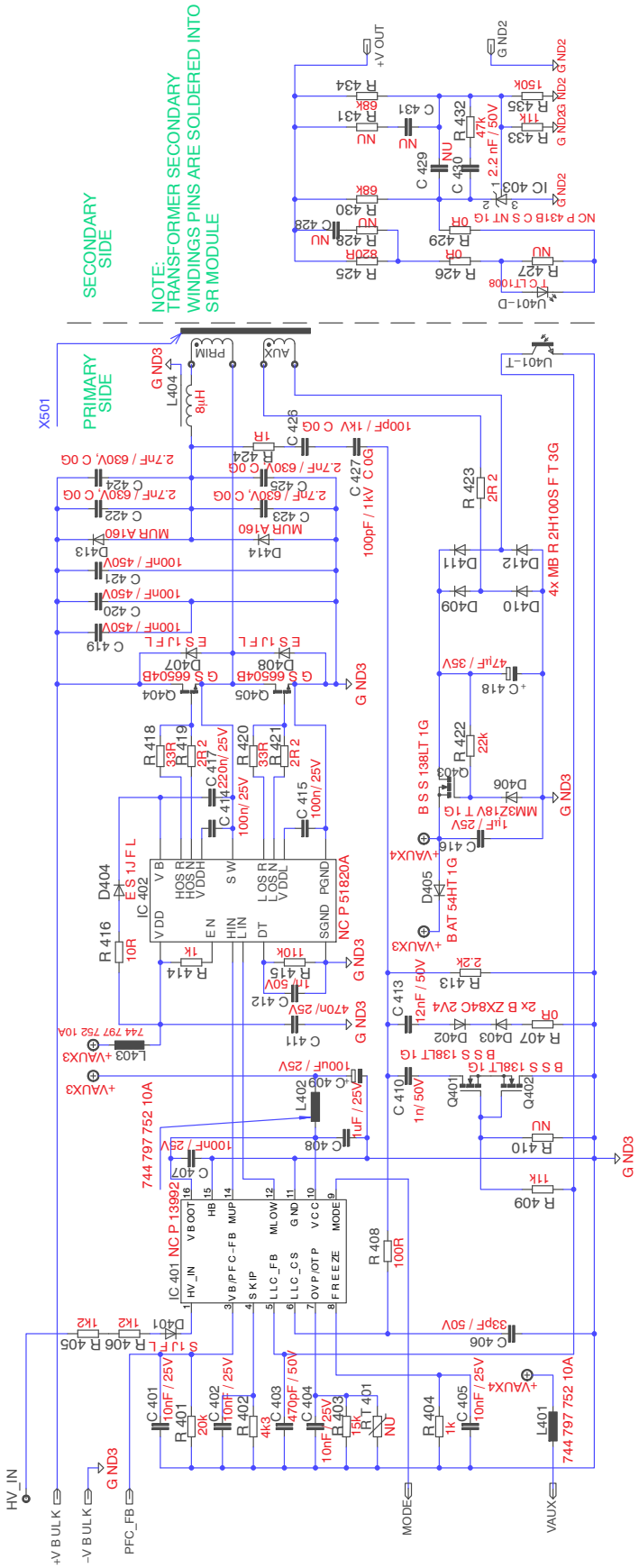


Figure 15. Schematic Diagram of LLC STAGE MODULE MOD103

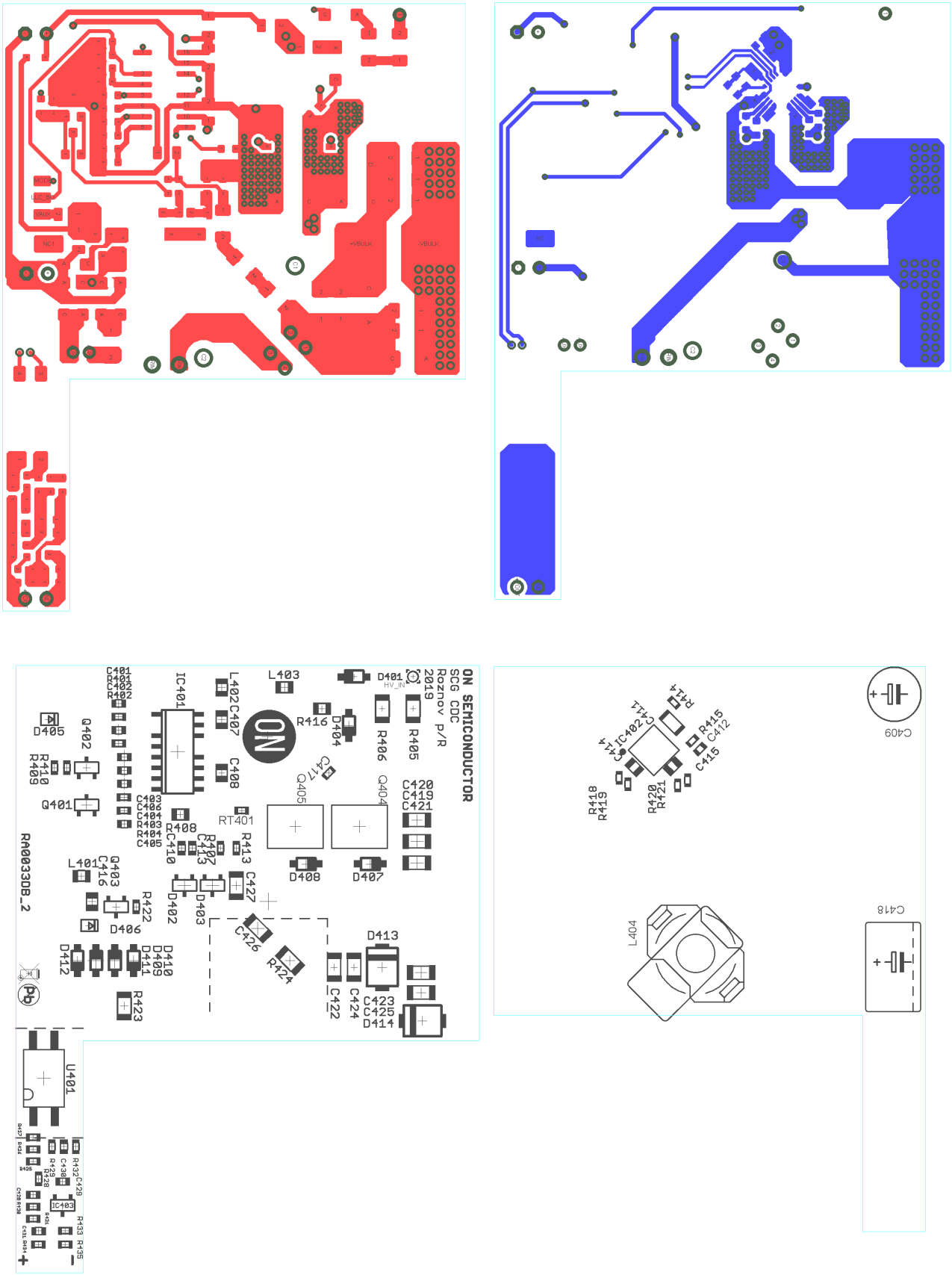


Figure 16. Top/ Bottom Layer PCB Layout and Assembly Plan of LLC STAGE MODULE MOD103

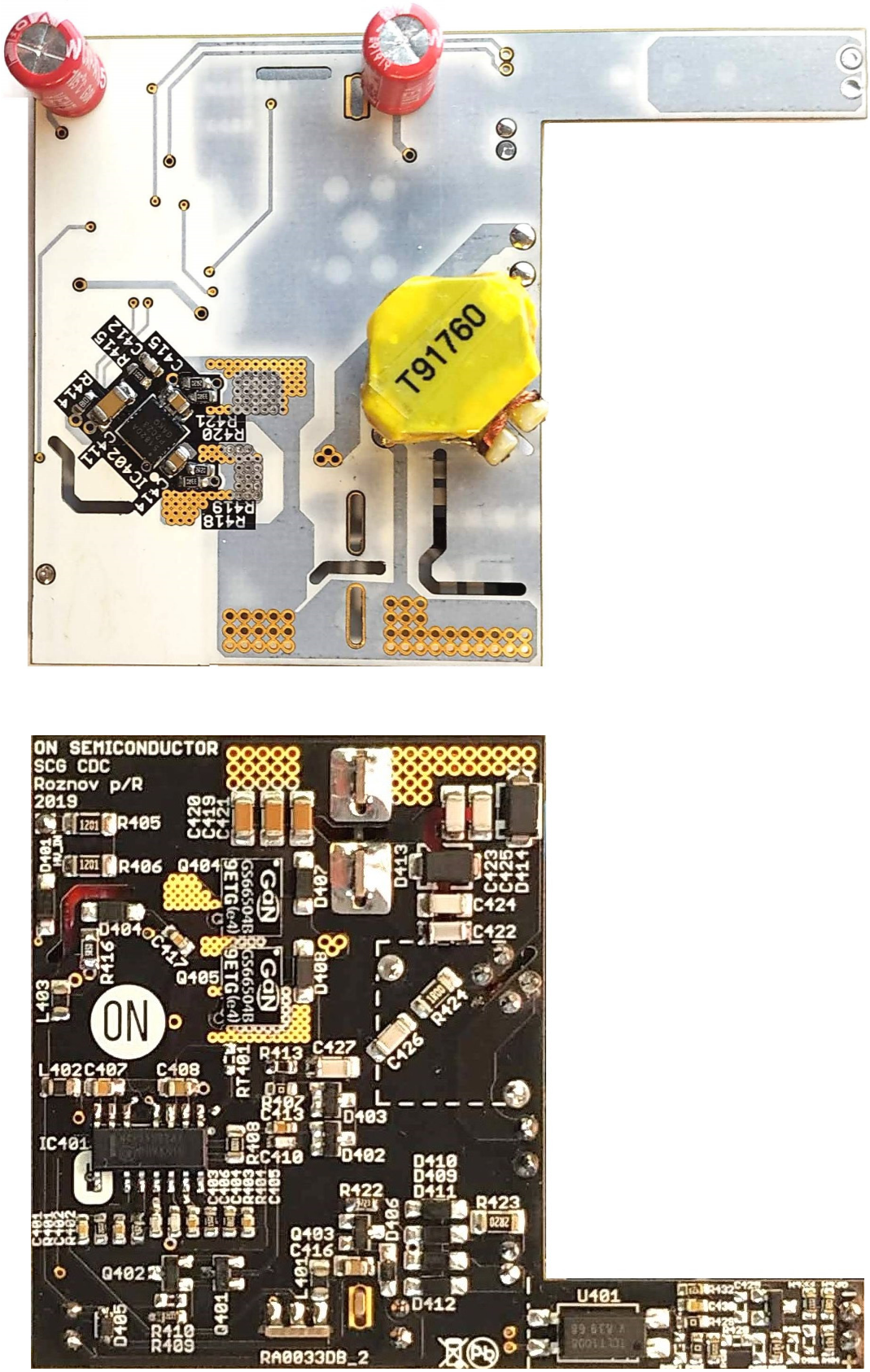


Figure 17. Photographs of LLC STAGE MODULE MOD103

LLC Controller NCP13992 Implementation

The NCP13992 is a high performance current mode controller for half bridge resonant converters. The controller implements 600 V gate drivers, simplifying layout and reducing external component count. In this case the HB pin is connected to GND and automatic dead−time function is disabled, controller operates with fix dead−time, both driver outputs are referred to ground potential and work as signal buffers only. Eternal GaN HB driver (NCP51820 IC402) is used to drive power stage switches, see schematic in Figure 83. The built−in Brown−Out input function eases implementation of the controller as LLC stage operation is enabled after BO pin receives proper signal level. Brown−out divider information is used also as PFC FB and thus voltage follower was implemented on MB (Figure 2: Q108, C121, R140, and R141). Voltage follower acts as impedance separator which cancels BO hysteresis current influence on the PFC feedback voltage, so bulk voltage regulation level is not changed, during states when hysteresis current is enabled or disabled. The NCP13992 features a dedicated output, the PFC MODE pin, which can be used to control PFC stage operation. This feature together with skip mode technique helps to improve light load efficiency of the whole application. The PFC MODE pin controls NCP1616 IC103 via divider network (R122, R123, R126, R130, and C112). PFC controller is forced to enter skip or stand−by mode when it detects signal below 300 mV at STDBY/FAULT pin. Consumption is the minimized and controller waits for bulk voltage restart level to recover operation. STDBY/FAULT pin voltage ranges between 0.5 to 1.5 V in normal operation mode. Refer to NCP1616 datasheet to skip mode procedure details. The NCP13992 provides a suite of protection features allowing safe operation in any application. This includes: overload protection, over−current protection to prevent hard switching cycles, brown−out detection, open optocoupler detection, over−voltage (OVP) and over−temperature (OTP) protections. OTP protection can be easily introduced by assembling RT401 which is placed close to Q405 source pad (see Figure 83 and Figure 16).

The NCP13992 controller features a HV startup current source (at HV pin) that allows fast startup time and extremely low standby power consumption. Two startup current levels are provided by the system for safety in case of short circuit between VCC and GND pins. In addition, the HV startup current source features a dedicated over−temperature protection to prevent IC damage under any failure mode that may occur in the application. The HV startup current source is primarily enabled or disabled based on V_{CC} level however it can be also enabled by BO_OK rising edge, auto−recovery timer restart and TSD restart events. The HV startup current source charges the VCC capacitor before IC start−up. The HV pin is interfaced to high−voltage through serial circuit R405, R406, D401 and HV_IN terminal at LLC STAGE MODULE (Figure 83) Insulated wire is used to connect to HV_LLC terminal located MAIN BOARD (Figure 2 close to C103). This kind of connection was implemented in order to simplify design and reduce HV start−up circuit losses. Diode D401 is installed to avoid any possible influence of bridge rectifier voltage (especially at near zero crossing levels) on controller's VCC supply voltage.

The auxiliary regulator and proper Vcc sequencing needed for auxiliary supplying is provided by auxiliary winding of X501 which voltage is rectified by bridge rectifier diodes D409−412 and filtered by C418. Voltage level at C418 varies two times approximately from no−load to full−load conditions. Thus the auxiliary regulator is needed to clamp +VAUX4 (also +VAUX3) voltage to approximately ≈ 16 V. Auxiliary regulator is built from Q403, R422, D406 and C416. Small signal MOSFET was selected at Q403 position to allow low bias for Zener diode D406. This minimizes regulator power consumption, especially during no−load condition. PFC controller IC103 supply voltage +VAUX4 and LLC controller IC401 supply voltage +VAUX3 are separated by diode D405. It is recommended to keep controllers supply lines independent in case that some of controller needs restart after a fault event. IC401 supply must be present before BO enables LLC stage for proper start−up sequence of whole application. GaN HB driver IC402 must be ready for operation before the first pulses are provided by IC401 to avoid missing pulses and perform suitable V_B voltage building and proper LLC stage soft−start sequence. Proper V_{CC} and start−up chaining further supports $V_{CC(on)}$ level of each IC.

The CS Divider provides LLC controller IC401 with information about current flowing through primary side of main stage. CS divider composes from R424, C426, C427, R413 and C410. C410 capacitor action is regulated via impedance of bidirectional switch (Q401−Q402) which is controlled based on feedback voltage though R409. Cs divider gain is fixed when LLC stage operates in normal mode and feedback voltage is higher as Q401−Q402 are fully switched on. As load is decreasing, LLC stage needs to enter skip mode operation to reduce switching frequency and keep efficient operation. Feedback voltage is reduced to very small level then and switch Q401−Q402 are turned off. C410 is thus disconnected and current sense divider gain is defined only with R413. As feedback is rising to initiate skip burst, feedback voltage is approaching threshold level of Q401−Q402, their impedance is modulated and system gain smoothly passes from maximum to minimum value. This technique helps to regulate burst energy and set desired skip in level, despite that resonant tank forces controller to deliver very high energy due to CS comparator delay.

The CS Divider clamp is used to avoid short circuit protection false triggering during high voltage swing transition at CS pin, which appears especially whilst LLC stage starts−up. High voltage peak is caused by transition phenomenon in CS divider which is suddenly biased by resonant capacitor voltage. CS Divider clamp composes of C413, Zener diodes D402−403 and R407. Zener diodes

connected in series (with cathodes together) create voltage off−set which in turn disconnects C413 in normal operation.

The output voltage regulation is ensured by the shunt regulator IC403–NCP435, see Figure 83 bottom right corner. The optocoupler U401 is driven via resistors R425 and R426 which determines the feedback loop gain. Resistor R430 biases the NCP431 in case that there is no current flowing through the optocoupler U401. The voltage feedback loop compensation network is created by resistor R432 and capacitor C430. The value of output voltage is set by voltage divider comprised of resistors R433, R434, R435. LLC STAGE MODULE MOD103 PCB layout implements empty part positions (C428, C429, C431, R410, R427, R428 and R431) which can be used to change feedback response in order to fulfil different application needs.

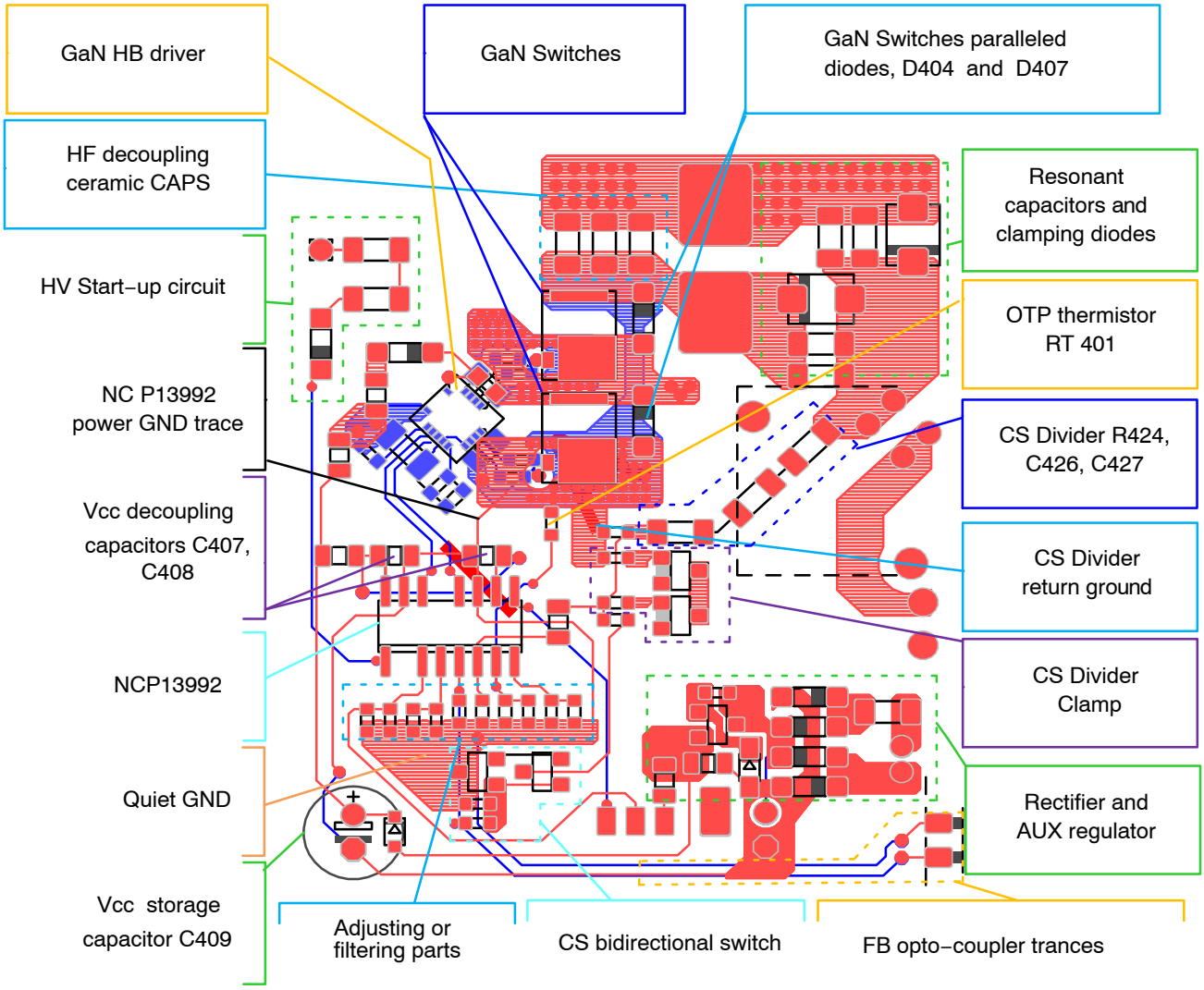


Figure 18. NCP13992 Recommended Connection Example

Design Tips for LLC Controller NCP13992 in High Frequency Application

High frequency applications exhibit higher dv/dt and di/dt signals compare to standard low frequency designs. Proper PCB layout is thus highly required to minimize switching noise. Below recommendations help with NCP13992 LLC controller integration into application and to avoid any unwanted or noisy behavior.

Vcc decoupling capacitor should be located very close to VCC and ground pins of each driver as demonstrates Figure 18. Use star connecting technique for the supply voltage distribution to supplementary circuitries. The splitting position should be selected appropriately depending on auxiliary current flow. Splitting place is mostly situated at positive pad of decoupling capacitors. Storage capacitor C409 doesn't have to be located close to the controller, however it used as distribution point for IC401 and IC402. Each driver section of IC402 produces current glitches up to 2 A peak with duration up to few tens of nanoseconds in supply line. L402 and L403 were implemented to suppress high frequency currents flowing in auxiliary supply lines. L401 is intended to filter Vcc line for PFC stage controller and sub−circuitries. It is very helpful to

separate VCC pins between controllers and drivers using resistor of few unit ohms. Higher supply line impedance separates VCC decoupling capacitors, which then cannot exchange electric charge each other like in case of low impedance connection.

Controller ground should be divided into “quiet ground” and power ground. Separating point should be located very close to the controller GND pin. Power ground is connected to Q405 source. Use quiet ground for connecting adjusting or controlling parts: BO, SKIP, FB, CS, FREEZE and OVP−OTP protection circuitries. Each pin used for protection or parameter setup, should be filtered by ceramic capacitor with capacitance at least 1 nF. The 10 nF capacitors are used in this reference design.

CS divider return ground should be connected directly to source pad of Q405. CS divider clamp should also use same ground. This minimizes current flowing from resonant capacitor, through CS divider (also CS divider clamp) via controller ground, back to power stage ground. Such situation can occur due to transient phenomena at resonant capacitor/ CS divider during start−up, skip burst or step load is applied. CS divider bidirectional switch is placed close to the controller on quiet ground.

HV pin uses relatively high voltage for controller start−up. Thus HV pin needs to be routed separately from other signals with reasonable creepage distance. The MODE pin is used for chaining with PFC controller. If this feature is omitted then MODE pin should be left open without decoupling or loading.

Few more techniques are important to assure good noise immunity of the LLC controller stage. The CS divider position and FB optocoupler placement shouldn’t be close to high dV/dt signals. FB optocoupler traces should be routed as closely coupled pair. One trace from the pair is ground extended from controller quiet ground. Use copper polygons connected to ground as a shielding against noise where possible.

The High Speed Half−Bridge Driver for GaN Power Switches NCP51820 Implementation

The NCP51820 high−speed gate driver is designed to meet the stringent requirements of driving enhancement mode (e−mode), HEMT and gate injection transistor (GIT), gallium nitride (GaN) power switches in off−line, half−bridge power topologies. The NCP51820 offers low and matched propagation delays with advanced level shift technology providing −3.5 V to +650 V (typical) common mode voltage range for the high−side drive and −3.5 V to +3.5 V common mode voltage range for the low−side drive. In addition, the device provides stable dV/dt operation rated up to 200 V/ns for both driver output stages. Both drive stages employ a dedicated voltage regulator to accurately maintain the gate−source drive signal amplitude and thus protect the gate of the GaN power transistor against excessive voltage stress. The circuit actively regulates the driver’s bias rails and thus protects against potential gate−source over−voltage under various operating conditions. The NCP51820 offers important protection functions such as independent under−voltage lockout (UVLO), monitoring VDD bias voltage and VDDH and VDDL driver bias and thermal shutdown based on die junction temperature of the device. Programmable dead−time control can be configured to prevent cross−conduction. Supply voltage applied to VDD provides bias for the digital inputs, internal logic functions, high−side floating bootstrap (VBST) bias supplying the internal high−side regulator (VDDH) as well as providing bias directly to the internal low−side regulator (VDDL). Single VDD bypass capacitor, CVDD, connected directly between the VDD and SGND pins is sufficient for decoupling because the GaN FETs receive source current locally through the dedicated internal regulators. The C_{VDD} capacitor should be a ceramic capacitor in the range from 10 nF to 100 nF, located as close to the VDD and SGND pins as possible to properly filter out all glitches caused by switching. Under voltage lockout (UVLO) is important to protect the GaN FETs and power stage. The NCP51820 includes UVLO thresholds of V_{DDUV+}> 8.5 V, ON and V_{DDUV-} < 8 V, OFF.

Dead−time of 110 ns is used in this design as it sufficiently covers whole application range. R415 is connected at DT pin to adjust dead−time period. The dead−time resistor uses simple rule 1 kΩ is equivalent to 1 ns DT increment. DT pin is decoupled by ceramic capacitor C412. GaN HEMTs switching turn−on speed is defined by resistors R418−R420, turn−off speed is then defined by resistors R419−R421. Turn−on process is slower and that’s way 33 Ω resistors were selected. On the other hand, turning−off speed must be fast to minimize turn−off losses, because device is switched off at peak of resonant tank current, thus 2.2 Ω turn−off resistor were adopted. Another important portion of the driver is bootstrap circuit, which is supplying high side section and consists of R416, D404 and C417. Resistor R416 limits charging current of C417 via diode D404 from C411. Do not insert inductor in bootstrap loop or instead of R416 to reduce bootstrap current peak as this may result in malfunction. R416 was set to 10 Ω to assure correct function through whole operating range. Vboot voltage is always built up after each low side driver pulse and is at high enough level, despite the LLC stage operates in very deep skip mode with period over 10 ms. ES1JFL bootstrap diode (D404) has been chosen due to its fast recovery character and very small junction capacitance. Low junction capacitance and low recovery charge are important to avoid discharging bootstrap capacitor and EMI issues. Another key advantage of ES1JFL is compact package taking just little area on the PCB. Resistor R414 enabling drivers operation should be low impedance to ensure that disable threshold won’t be triggered and no high side missing pulses appear, due to logic rule “low side pulse first”. Please refer to NCP51820 datasheet and related application note AND9932/D for more information regarding proper application of this driver.

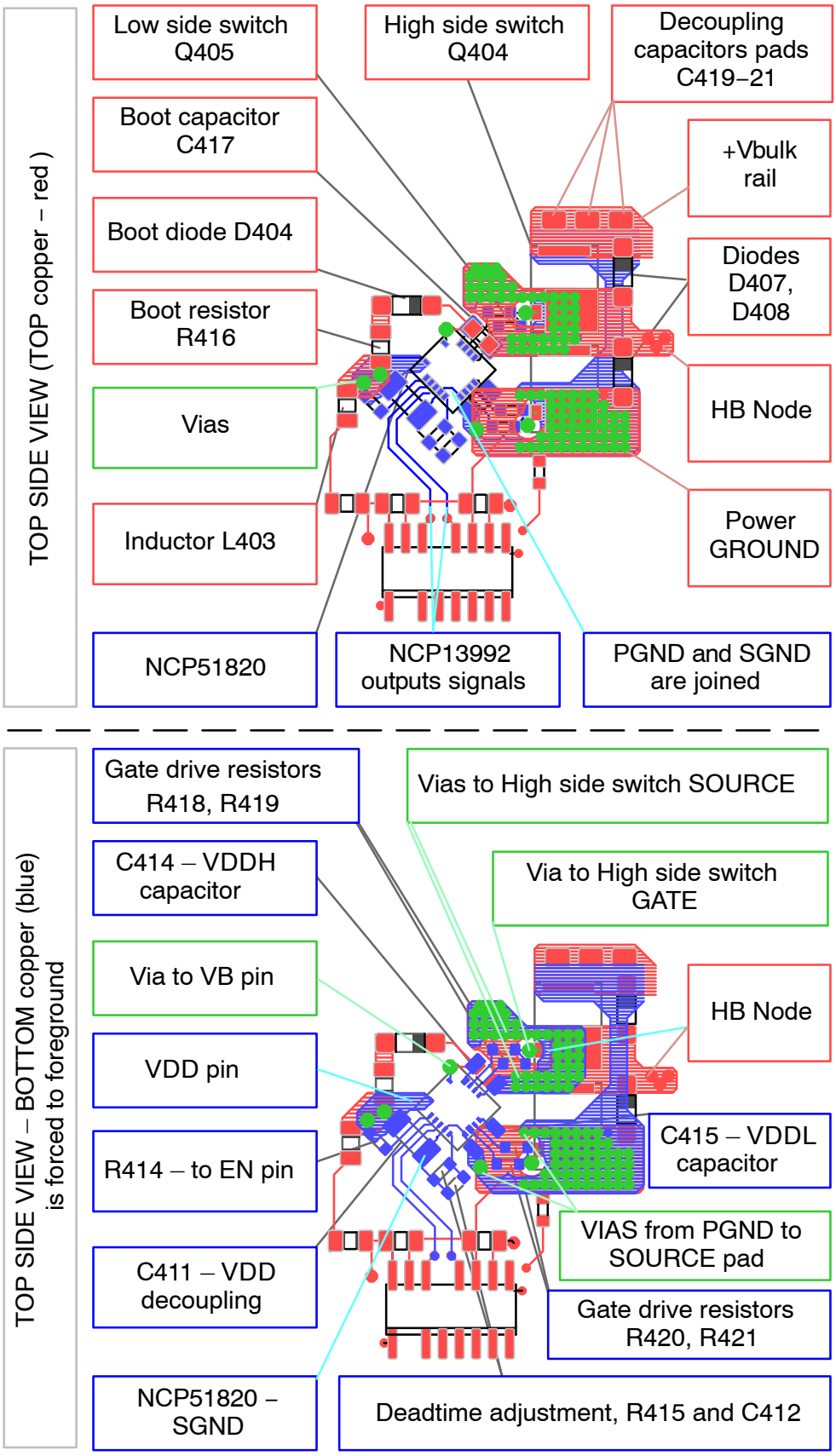


Figure 19. NCP13992 Recommended Connection Example

Design Tips for NCP51820 in High Frequency LLC Application

NCP51820 is following design rules from "GaN HEMT Gate driving consideration" section. Implementation of NCP51820 is done under specific application limitation, which include dimensions and shape see Figure 16, Figure 17. Some of components as well as power terminals had predefined positions which could not be changed. These limitations are very common in SMPS and it is usual that design is processed according to them. The LLC STAGE MODULE MOD103 design approach is described below and it tries to provide simple method how to implement NCP51820 into power stage step by step. As first step, the mandatory elements (all terminals and resonant inductor) had been placed on the PCB. Second step is placement of Q404, Q405, D407, D408 and C419−421. Ceramic capacitors C419−421 should be as close tothe high side switch drain pad as possible see Figure 19 (also better visibility in Figure 18). Considering Q404−Q405 losses ≈ 250 mW each at full power, both devices require relatively small area to remove heat and may be close each other. Diodes D407−408 are place in parallel to Q404, Q405. This arrangement allowed implementing flux cancelation loop mentioned in "GaN HEMT based Power Stage" section. The resonant capacitors C422−C425 together with clamping diodes D413−414 were located as next step in order to minimize module area. Everything was placed close to Vbulk rail terminals and resonant inductor L404 while some place was left for CS divider upper capacitors C426−C427. Resonant capacitors and related clamping diodes were sited next to each other. NC51820 with surrounding elements were linked to power switches after power stage had been routed. Positioning of NC51820 was done in such way that the driving loops are approximately same for both Q404−405 transistors see Figure 19 bottom picture. Both driving loops are almost symmetrical furthermore. Internal regulator VDDL and VDDH decoupling capacitors C414−415 are both placed near to related pins in the same layer as NCP51820. Reason for this is to minimize driving loop inductance. VDD decoupling capacitor C411 lays next to VDD and SGND pins in bottom layer. Bootstrap loop (R416, D404 and C417) connection order is highly important. Principally, VB capacitor C417 is charged from the drain, when low−side switch turns−on, subsequently C414 voltage is built from C417 via internal regulator. C417 was placed on TOP side of PCB to be closer to drain, this remove part of inductance in bootstrap loop. This solution also helps to shrink high−side driving path. Resistor R416 is connected through copper via to C412. C415 serves as primary source providing energy for bootstrap. D404 cathode is connected to C417 and from same positive pad C417 is heading trace to VB pin through PCB via, while both traces are routed separately. General rule for proper decoupling says that one trace is entering to decoupling capacitor pad from power supply and second trace must leave it to IC supply pin, while both are separated. Afore mentioned order enables simplifying of bootstrap loop layout and balancing of driving loop lengths. In this application, SGND and PGND should be connected together by the short trace, see AND9932/D.

The NCP13992 with surrounding circuitries was added to PCB right after NCP51820 PCB layout implementation had been completed.

SR MODULE MOD104 is portrayed in Figure 21, Figure 22, Figure 23 and. Figure 28. This module is built based on four single channel MOSFETs and two synchronous rectification drivers NCP4306. MOSFETs Q502−505 are packaged in SO−8FL to support high power density. Two MOSFETs are arranged in two branches of center tapped rectifier. Each MOSFET branch is protected against voltage spikes by the RC snubbers which are connected across the FETs drains and sources. RC snubber circuits are composed of C501−R501−R503 and C502−R502−R505. The synchronous rectifier drivers IC501−502 NCP4306 drive MOSFETs based on drain voltage information. Each NCP4306 uses external adjusting and decoupling elements. Module requires high frequency decoupling, which is done with ceramic capacitors C503, C504 and C507, C508. R508−R513 and R509−R512 set minimum ON−time and minimum OFF−time period respectively. Minimum ON−time is set to ≈ 110 ns and minimum OFF−time was adjusted to ≈ 680 ns. Automatic Light Load detection (LLD) timer can be tuned by R507−R514. The LLD pins must be decoupled with C509−C510. LLD timer was tweaked to 68 μs which is suitable value for most LLC converters and improves no−load consumption. For more information about LLD feature refer to datasheet of NC4306. Above mentioned timing values well cover SR setup for this reference design in whole operating range. SR MODULE contains spare components which can build simple voltage regulator in case that 10 V driver clamp would be used. NCP4306 with 5 V driver clamp option is recommended for this design to reduce driving losses. Total driving losses vs. frequency data are provided in Figure 20, while two paralleled NTMFS5C645NL MOSFETs are driven. Total driven capacitance is 4.6 nF.

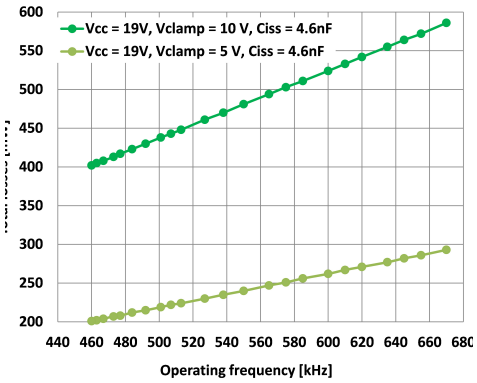


Figure 20. NCP4306 Total Losses vs. Operating Frequency for 10 V and 5 V Clamp Option

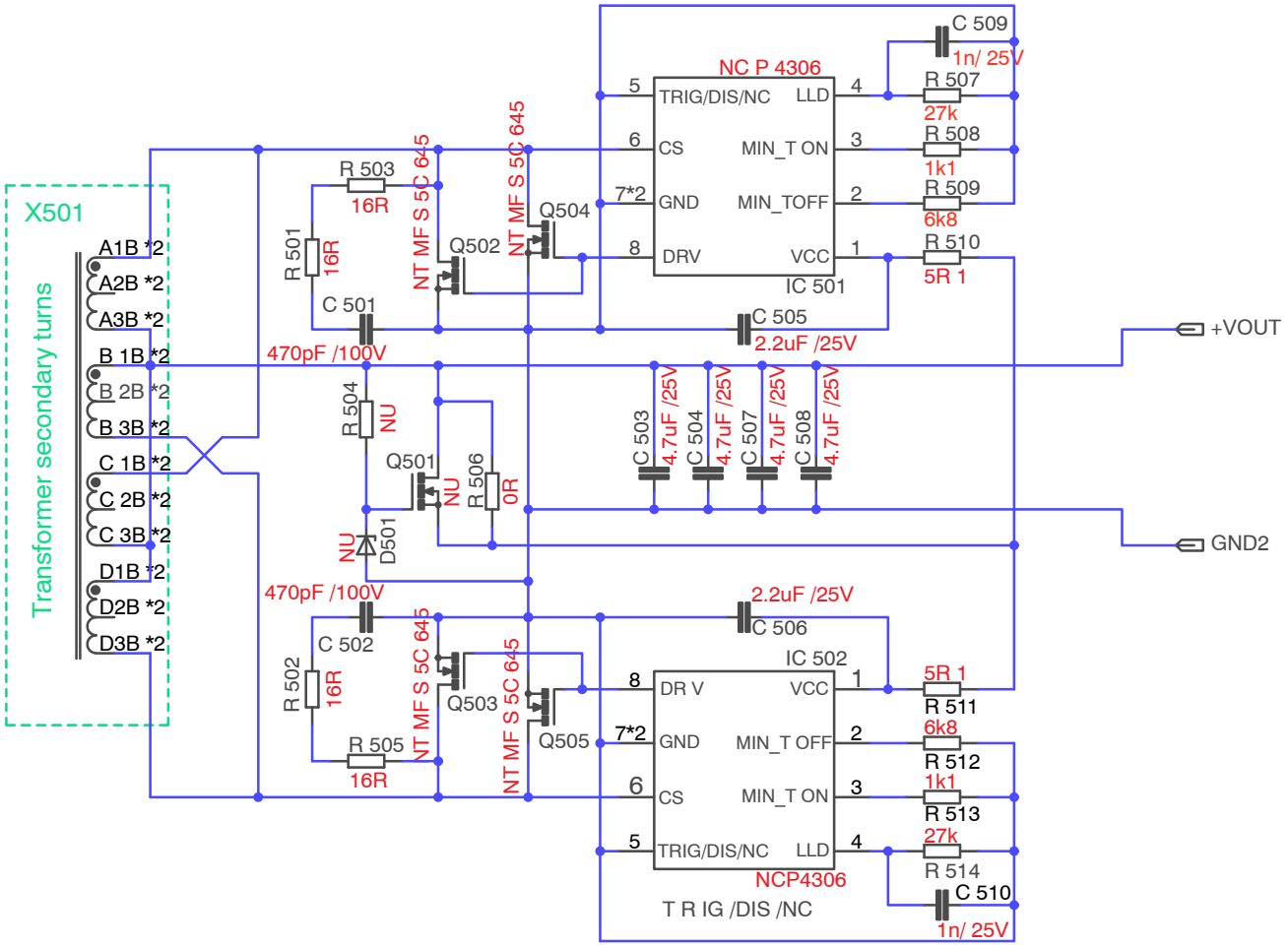


Figure 21. Schematic Diagram of SR MODULE MOD104

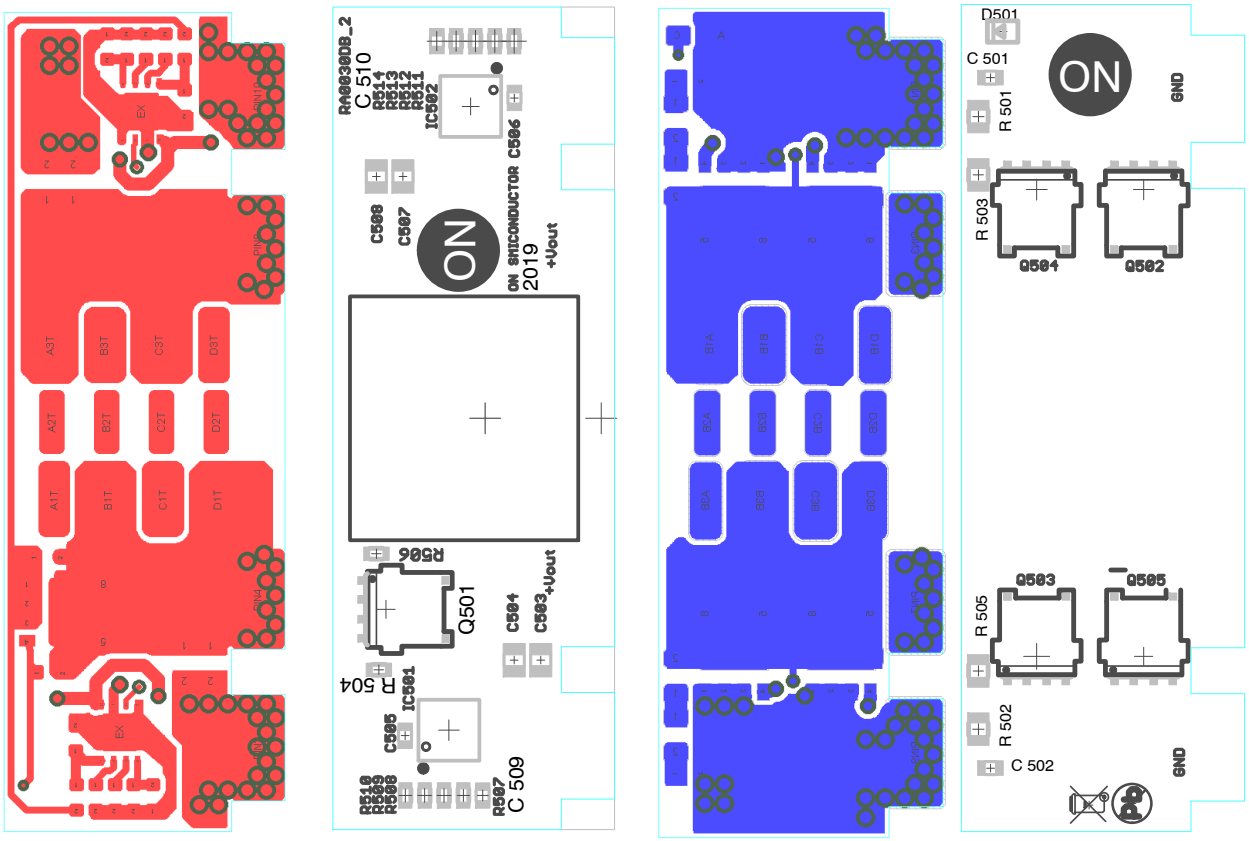


Figure 22. Top/ Bottom Layer PCB Layout and Assembly Plan of SR MODULE MOD104

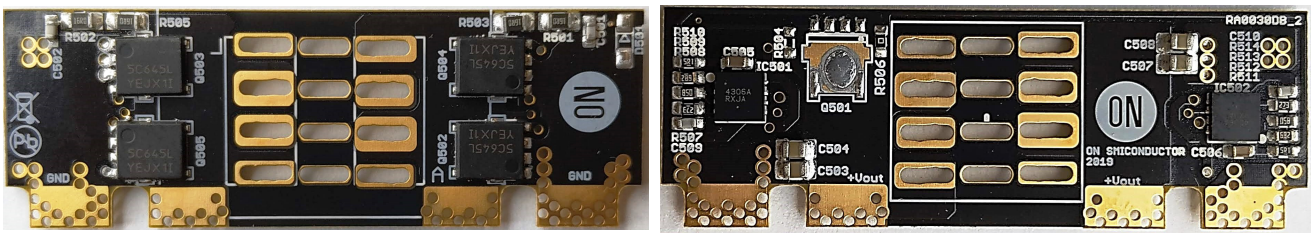


Figure 23. Photographs of SR MODULE MOD104

The LLC transformer obeys specific design rules to fit LLC power stage optimally. Two general solutions are used in practice: discrete or integrated LLC transformer tank implementation. Discrete LLC transformer features small primary leakage inductance which influence on resonant frequency is minimal when compare to integrated LLC transformer. Primary winding inductance of discrete LLC transformer as well as integrated version is derived from zero voltage switching (ZVS) conditions. ZVS is present only when energy stored in magnetizing inductance is high enough to fully charge or discharge HB node parasitic capacitances within dead−time interval. The magnetizing inductance energy depends on turn−on time, applied voltage and inductance. If magnetizing inductance energy is lower, then HB node transition takes longer time and dead−time must be longer and vice versa. The limiting factor is minimum energy which creates sufficient HB node voltage ring to activate power switch body diode, thus ZVS. It is easier maintained ZVS for lower switching frequency (or higher loads) and maximum input voltage. Operating voltage range needs to be limited. The lowest permissible voltage should be chosen for full load (or overload level), while application is still in regulation. The highest voltage is usually defined by PFC stage regulation. PFC over−voltage protection may be triggered in case that bulk voltage would achieve higher bulk voltage level. Magnetizing inductance value should be chosen for the highest expected operating frequency in normal mode to sustain ZVS.

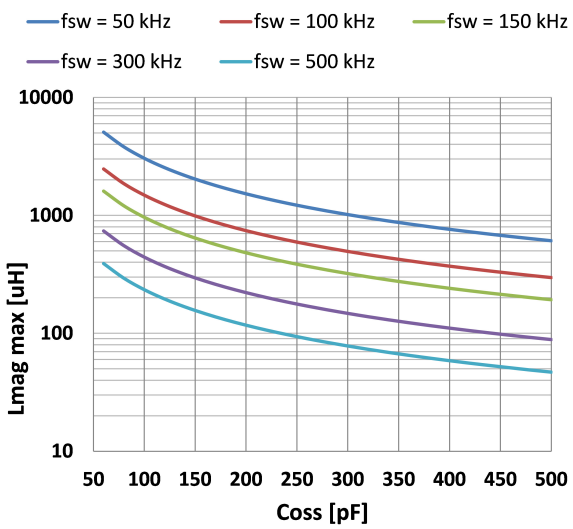


Figure 24. Maximum Recommended Magnetizing Inductance vs. COSS and Operating Frequency

Magnetizing inductance is essential for proper LLC converter operation and Figure 24 can be used to read its value and simplify selection process. Chart in Figure 24 is dedicated for half−bridge stage for first magnetizing inductance approximation. It is easy for using, firstly check power switch output capacitance C_{OSS}, most precise number is energy related output capacitance $C_{OSS(er)}$. Pick it value up at C_{OSS} axe and then read $L_{mag\ max}$ axe value for specific frequency.

The high frequency transformers can be divided into many categories, but further will be discussed only planar core transformers as high power density candidates. Also, integrated LLC transformers and PCB based planar transformers are not assumed. Considering winding embodiment may be planar core based transformers separated to:

- Transformer with fully planar windings. All windings are made of copper plates, while between plates is insulation material. This kind of transformer is more appropriate for lower input voltage application, due to limited primary turn's number and transform ratio. Benefit is simple manufacturing of windings. Drawback of this transformer is higher inter−winding capacitance
- Transformer with all windings made of litz wires. Primary winding is usually prepared from triple insulated wire (TIW) to improve and reinforce insulation between primary and secondary side. Litz wire enables to enhance primary turn's number and use transformer in high−voltage application. Litz wire usage decreases impact of skin and proximity effects. Secondary windings are typically paralleled for improving secondary side DC and AC resistance. Disadvantage is little bit higher leakage inductance of secondary side
- Hybrid windings transformer, in our case it means, that primary winding is done from TIW litz−wire and secondary windings are created from copper plates. Insulation ensures TIW at primary side and insulating turn holders for secondary turns. This kind of embodiment combines advantages of two solutions above mentioned

Hybrid windings Transformer can be prepared with multiple arrangements. During reference design developing, three transformer structures from Figure 25 were evaluated and best of them was chosen for further manufacturing. Structure number 1 in Figure 25 has three primary sections, two secondary sections and one airgap. Solution 1 delivers highest SR MOSFETs V_{DS} peak voltage, which is very hard to suppress.

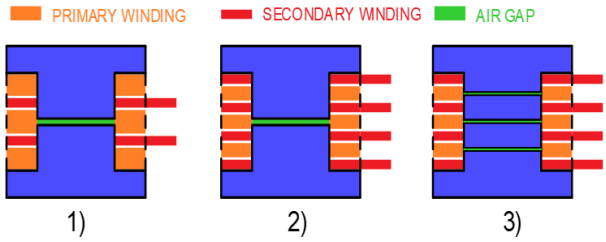


Figure 25. Hybrid Windings Transformer Possible Structures

Structure number 2 in Figure 25 has three primary sections, two secondary sections and one airgap. This configuration improves magnetic coupling and decreases secondary windings leakage inductance. Result of this is lowered SR MOSFETs V_{DS} peak voltage from ≈ 78 to ≈ 52 V. Four sections secondary winding enables use of 60 V SR MOSFETs, while for two sections secondary winding are 80 V SR MOSFETs still marginal. Structure number 3 in Figure 25 features three primary sections, two secondary sections and three airgaps. Airgaps are distributed in center leg of core. Each of them is aligned to primary winding section. Level of fringing flux which would enter to windings section is reduced thanks to distributed shorter airgaps. Thus, fringing flux generated losses (resistive character) are lowered. Main reason why this solution (Figure 27) was introduced is further reduction of transformer resistive losses. Comparing performance of three mentioned structures we can say that structure 1 is the worst and structure 3 provides best results see Figure 26 for related achieved efficiency.

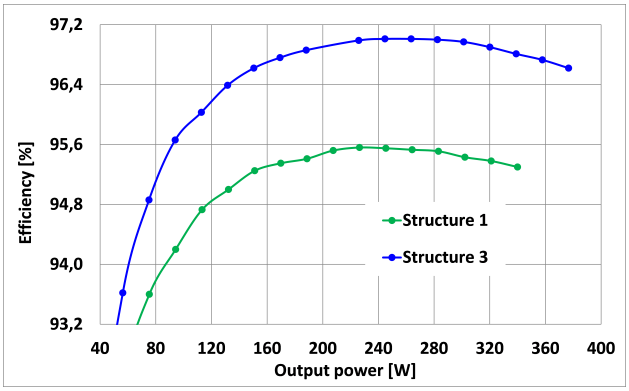


Figure 26. Efficiency Comparison of Transformer Structure 1 and 3

To summarize properties of transformer structure 3 in Figure 25 and Figure 27:

- Good manufacturability
- Lower resistive losses
- Lower leakage inductance
- Small SR MOSFET V_{DS} peak voltage
- Better thermal management, thanks to four sections of secondary turns more heat can be transferred

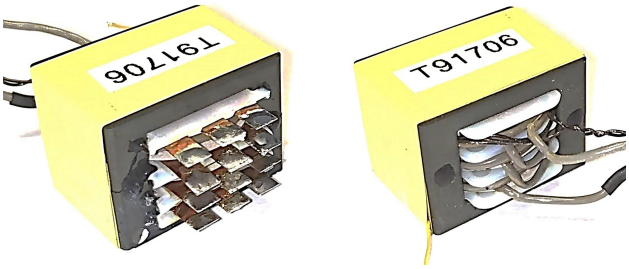


Figure 27. Hybrid windings Transformer Sample (Manufactured by Sumida America Components Inc.)

Above mentioned advantages prioritize to implement transformer structure 3 into reference design. Transformer could be further enhanced by using 5 sections of primary winding but this is too complicated from production point of view.

Based on information from transformer evaluation Sumida America Components Inc developed two transformer samples T91706 and T91715. Sample T91706 is recommended for power level 300 W and T91715 has higher power rating up to 400 W. For more information about transformer samples refer to Sumida contact in the end of document.

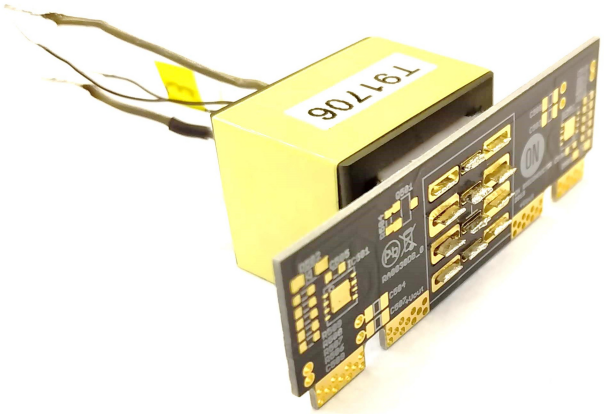
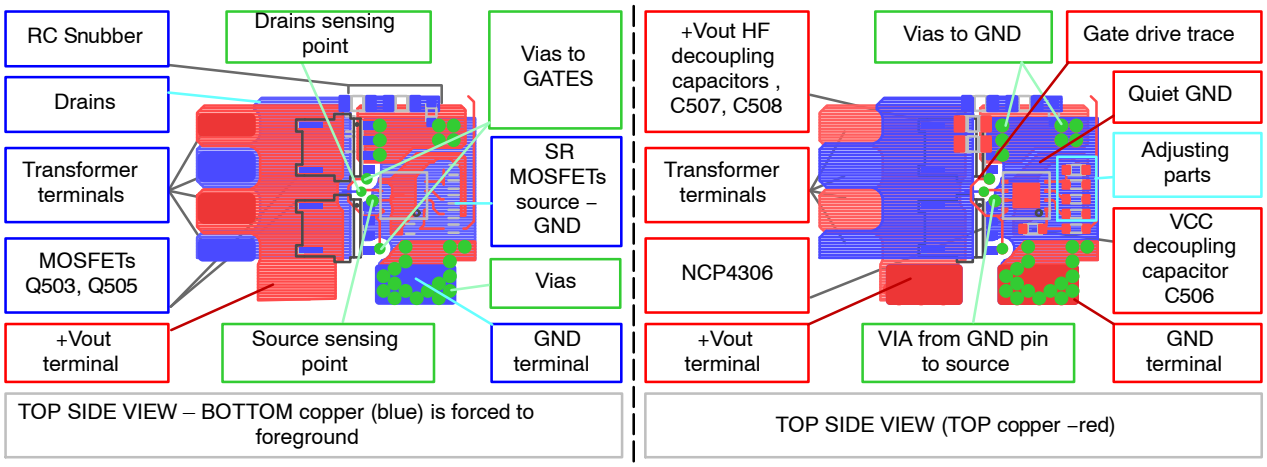


Figure 28. Photograph of SR MODULE MOD104 and Hybrid Windings Transformer

T91706 transformer sample has been used in this reference design. Transformer is inserted and soldered into the SR MODULE MOD104 PCB, see Figure 28 and then whole module is attached to MAIN BOARD visible also in Figure 1. Transformer secondary windings are connected in such way, that one outer section operates together with outlying inner section in parallel mode. This is the key for better distribution of the magneto motoric force, which supports previously mentioned benefits. Parallel operation of windings is secured by PCB layout in Figure 22. Direct parallel windings connection has been used in the design which is more effective solution than two independent SR branches merged into one. The SR MODULE would be much more complicated in case of two independent SR branches solution that would require SR driver with surrounding components including extra MOSFET with snubber.

Design Tips for NCP4306 in HF Application

Most of the rules mentioned in previous text (mainly in “Design Tips for SR Driver ...”) can be applied to NCP4306 implementation in HF application as well. NCP4306 housed in DFN−8 package (4x4 mm) has been selected for SR MODULE MOD104. Beside the low thermal resistance, the DFN−8 package offers thermal pad that can be used as ground distribution point. Vcc decoupling capacitor is placed next to the thermal pad (GND pad) and close to Vcc pin, while quiet ground is taken from opposite site. Use few units Ohms resistors (R510, R511) to separate VCC decoupling capacitors between each other and from output voltage decoupling capacitors. This smooths charge exchange between mentioned capacitors. Charge exchange can happen for example in case of step load or when SR Drivers grounds are unbalanced. Adjusting parts should use the quiet ground separated from driving ground Figure 28. Ground of SR driver should not be connected to power ground through which high output current is flowing. This secures that sensing and gate driving is not influenced by load current. Drain sensing point is selected as middle point in between drains of Q503−Q505, whilst related drain pad edge is close to source−gate pads, see left picture in Figure 28. This point is far away enough from main current path, thus influence to sensing point is minimized. Common GND for both MOSFET sources should similarly be in the middle between Q503−Q505. Use at least 0.7 mm trace width and via drill diameter 0.6 mm to allow sufficiently fast driving. The ground via drill diameter should be +0.1 mm bigger as gate via diameter, in case of paralleled SR MOSFETs. Low impedance of gate−drive loop enables very fast turn−off of SR MOSFET. Practical tests proved that it is better to use vias along edges of power traces and left central area untouched. This approach keeps trace impedance low. RC snubber placement is not so critical so it should be done in such a way that it eases PCB layout.



NOTE: The trace widths in Figure 29 were reduced, in order to clearly demonstrate connecting paths. Appropriate trace widths has to be used in final design, especially for Vcc and driving loops. For proper trace width refer to PCB layout in Figure 22.

Figure 29. NCP4306 PCB Design Example

Evaluation Demo−board Connections and Power−up and Test Procedure

Important notes:

- Do not apply extreme voltage to the input terminals!
- Be careful, high DC voltage is presented!
- Do not apply DC voltage to the input terminals!
- The demo is not optimized for surge, lightning, etc
- This reference board requires thermal management especially at very low line voltage. Use fan for excessive heat spreading
- Follow up power−up and power−down sequences

Power−up Sequence:

1. Connect AC Supply to the demoboard AC input
2. Connect Electronic Load at the output terminals with proper polarity – see figure Figure 30
3. Set AC Supply voltage in range 85 to 265V AC
4. Turn AC Supply on
5. Check output terminals voltage, approximately 19 V
6. Modify electronic load current to desired level while output voltage is monitored

Power−down sequence:

1. Turn AC Supply off
2. Discharge bulk capacitor for manipulating further

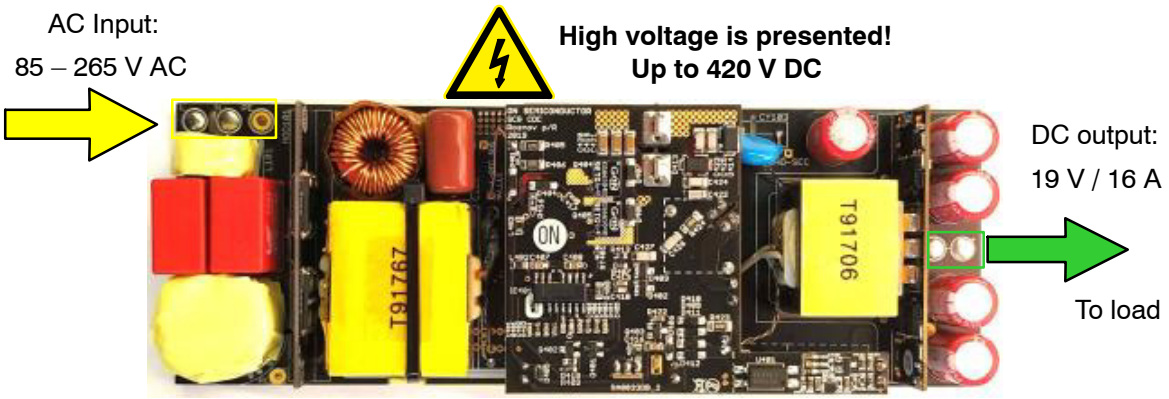


Figure 30. NCP4306 PCB Design Example

Measurements section

Table 3 provides summary information about system efficiency and no−load power consumption measured at several input voltage levels while synchronous PFC operation is enabled. Conduced EMI signatures offer Figure 32 and Figure 33 as well as thermal images whilst full load was applied in Figure 34, Figure 35, Figure 36 and Figure 37. Pictures from Figure 38 are demonstrating operating waveforms, which were captured at specified condition. It should be noted, that operating waveforms can slightly vary depending on actual demoboard as well as components values are altering due to their tolerance. Step load response and output voltage ripple showed from Figure 66 to Figure 73, were measured directly at output terminals without any additional decoupling or filtering. If lower ripple is required simple additional post filter can be implemented to reduce ripple to desired level.

Table 3. EFFICIENCY SUMMARY

LOAD		Consumption [mW] or Efficiency [%]	
		110 V AC 60 Hz	230 V AC 50 Hz
0 mW		< 150 mW	< 150 mW
120 mW		< 300 mW	< 300 mW
250 mW		< 450 mW	< 450 mW
500 mW		< 750 mW	< 750 mW
1000 mW		< 1300 mW	< 1300 mW
Load 1.0%	3 W	77.8	79.6
Load 2.5%	5 W	81.7	81.9
Load 5.0%	15 W	85.2	84.7
Load 10%	30 W	86.7	86.8
Load 20%	60 W	90.5	92.0
Load 25%	75 W	91.5	92.9
Load 50%	150 W	93.5	94.8
Load 75%	225 W	93.1	95.0
Load 100%	300 W	92.5	94.8
4 point AVG		92.7	94.4

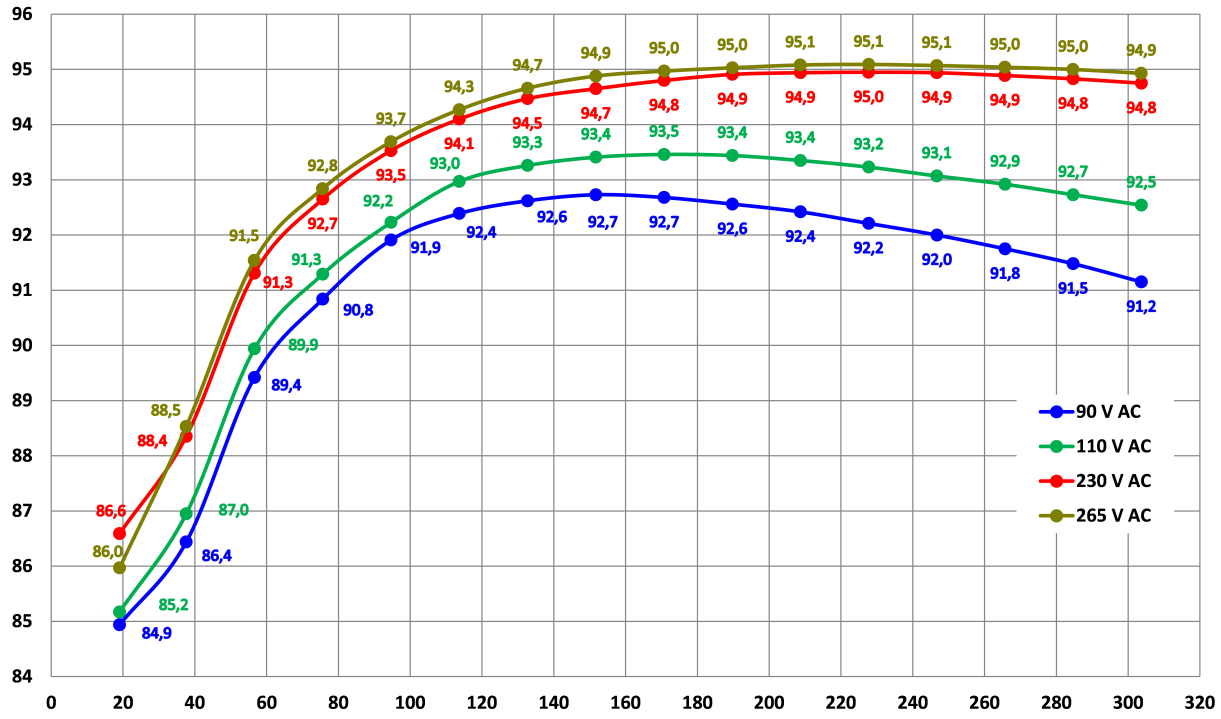


Figure 31. Adapter Total Efficiency vs. Loading Power

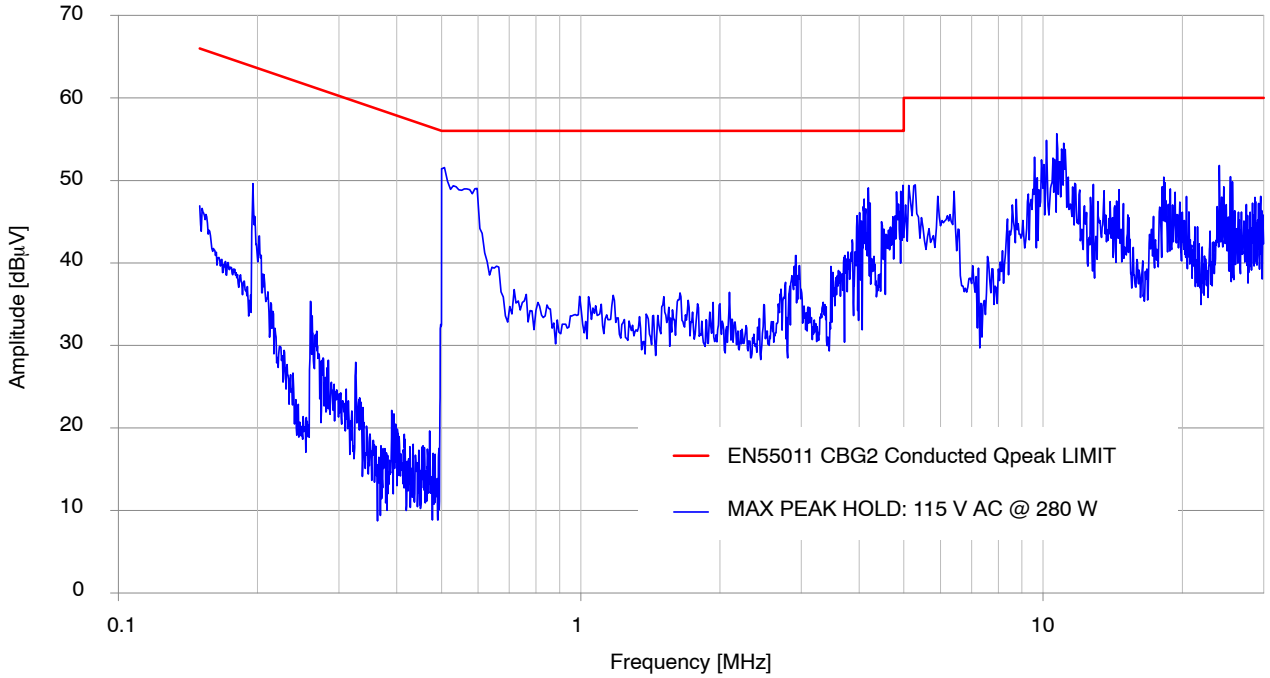


Figure 32. Conduced EMI Signature vs. Frequency at Input Voltage 115 V AC and 280 W Load

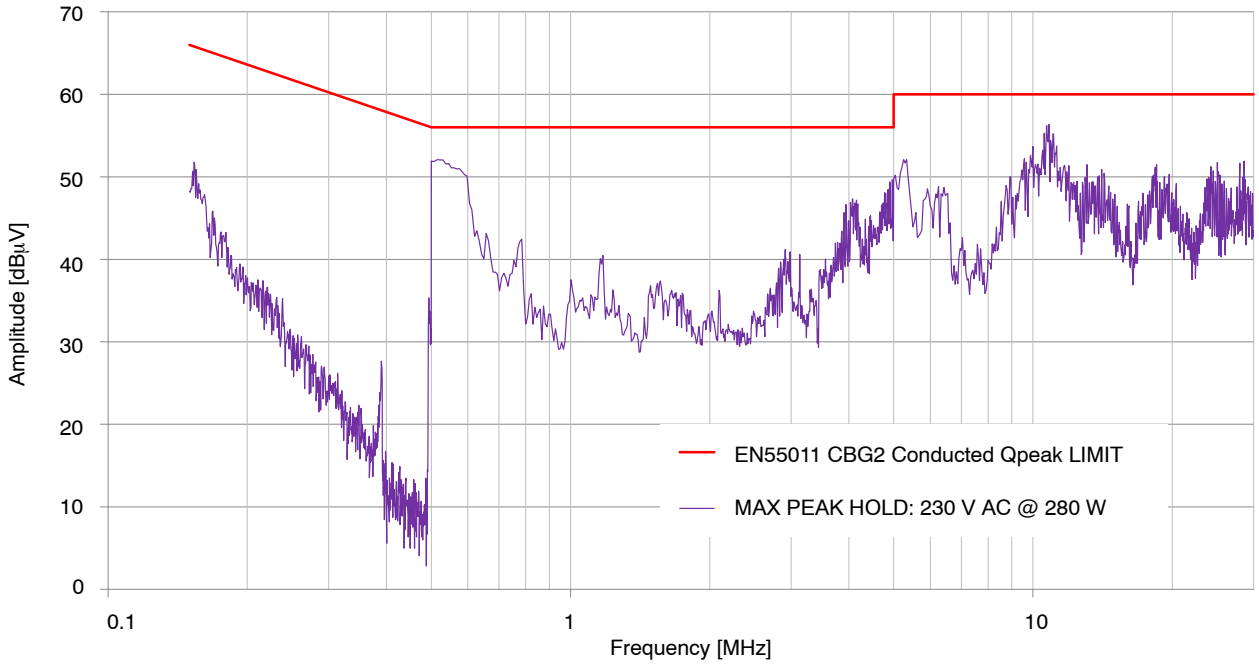


Figure 33. Conduced EMI Signature vs. Frequency at Input Voltage 230 V AC and 280 W Load

Spot 1 – 2	B201 – B204, BRIDGE RECTIFIER MODULE
Spot 3	Q404 High side GaN Switch, LLC STAGE MODULE
Spot 4	Q405 Low side GaN Switch, LLC STAGE MODULE
Spot 5	L404 resonant inductor, LLC STAGE MODULE
Spot 6	X501 LLC Transformer
Spot 7	Q503 & Q505, SR MODULE
Spot 8	Q502 & Q504, SR MODULE

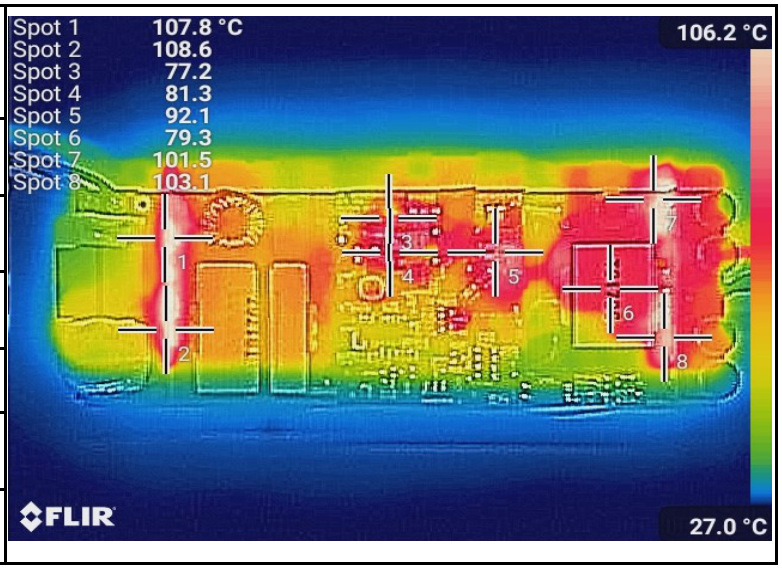


Figure 34. Thermal Image taken at Input Voltage 110 V AC and 300 W Load (Component Side)

Spot 1 – 2	BRIDGE RECTIFIER MODULE connection to MAIN BOARD
Spot 3	R121–R125–R128 PFC shunt, MAIN BOARD
Spot 4	Q106 PFC GaN Switch, MAIN BOARD
Spot 5	Q107 PFC GaN Switch, MAIN BOARD
Spot 6	Q107 PFC Synchronous GaN Switch, MAIN BOARD
Spot 7	X501 LLC Transformer
Spot 8	SR MODULE connection to MAIN BOARD

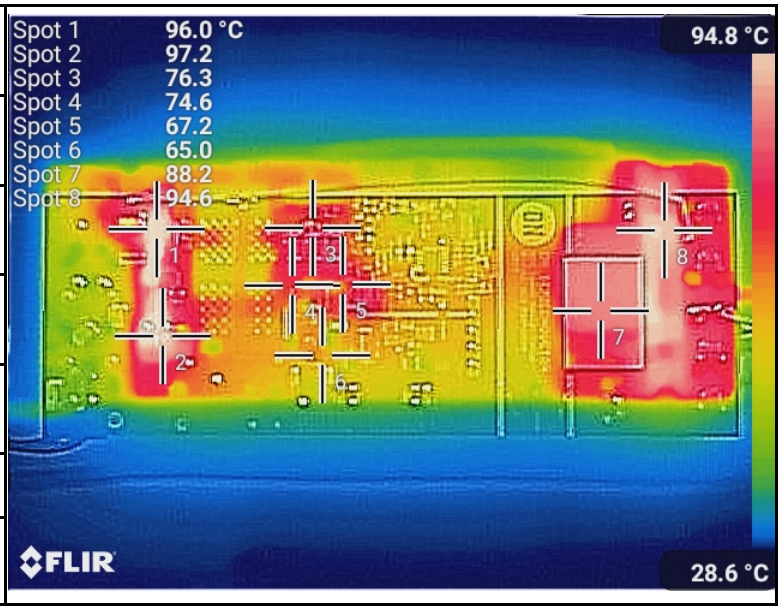


Figure 35. Thermal Image taken at Input Voltage 110 V AC and 300 W Load (Bottom Side)

Spot 1 – 2	B201 – B204, BRIDGE RECTIFIER MODULE
Spot 3	Q404 High side GaN Switch, LLC STAGE MODULE
Spot 4	Q405 Low side GaN Switch, LLC STAGE MODULE
Spot 5	L404 resonant inductor, LLC STAGE MODULE
Spot 6	X501 LLC Transformer
Spot 7	Q503 & Q505, SR MODULE
Spot 8	Q502 & Q504, SR MODULE

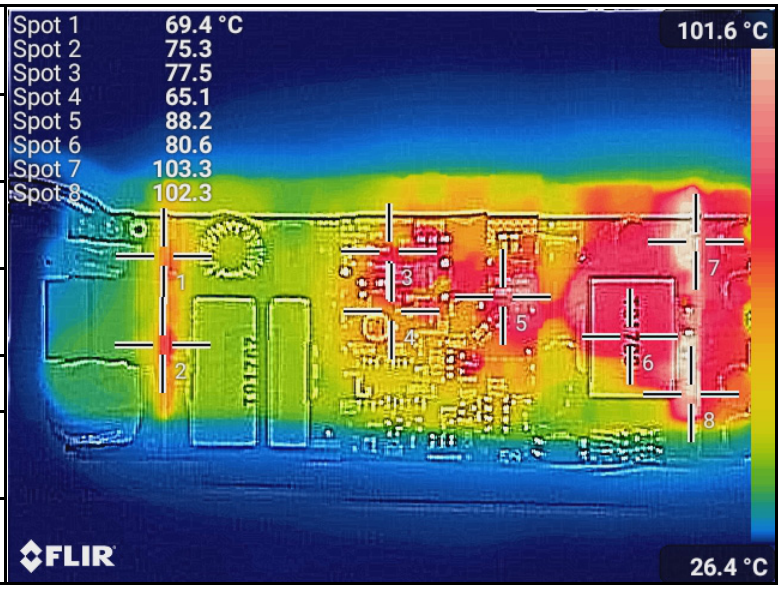


Figure 36. Thermal Image taken at Input Voltage 230 V AC and 300 W Load (Component Side)

Spot 1 – 2	BRIDGE RECTIFIER MODULE connection to MAIN BOARD
Spot 3	R121–R125–R128 PFC shunt, MAIN BOARD
Spot 4	Q106 PFC GaN Switch, MAIN BOARD
Spot 5	Q107 PFC GaN Switch, MAIN BOARD
Spot 6	Q107 PFC Synchronous GaN Switch, MAIN BOARD
Spot 7	X501 LLC Transformer
Spot 8	SR MODULE connection to MAIN BOARD

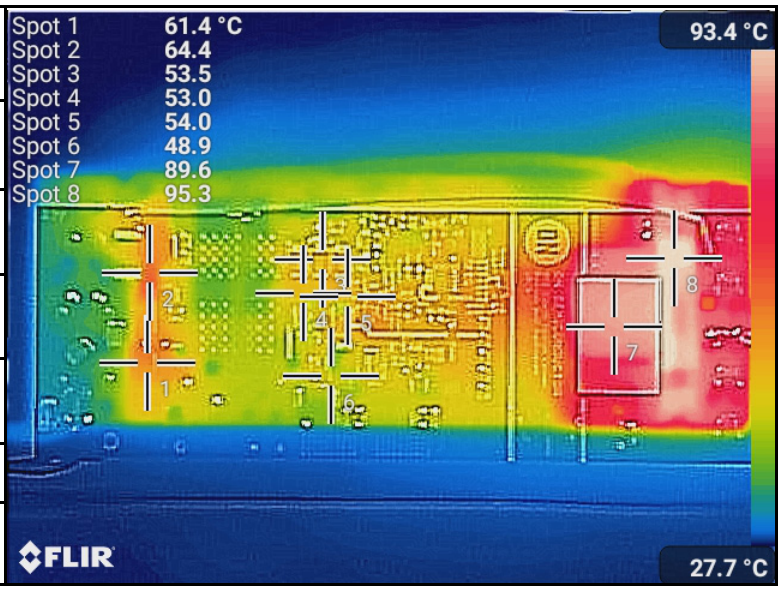


Figure 37. Thermal Image taken at Input Voltage 230 V AC and 300 W Load (Bottom Side)

Operating Waveforms during Burst

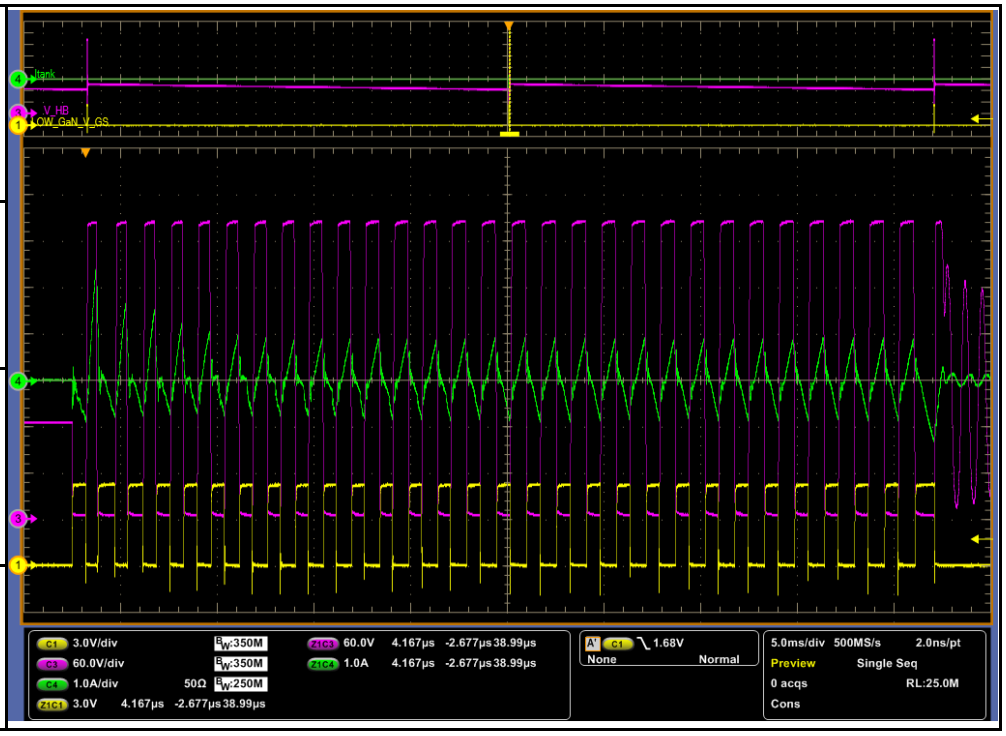
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 38. Primary Side, LLC Stage Burst Waveforms at Load 0 W (0 mA)

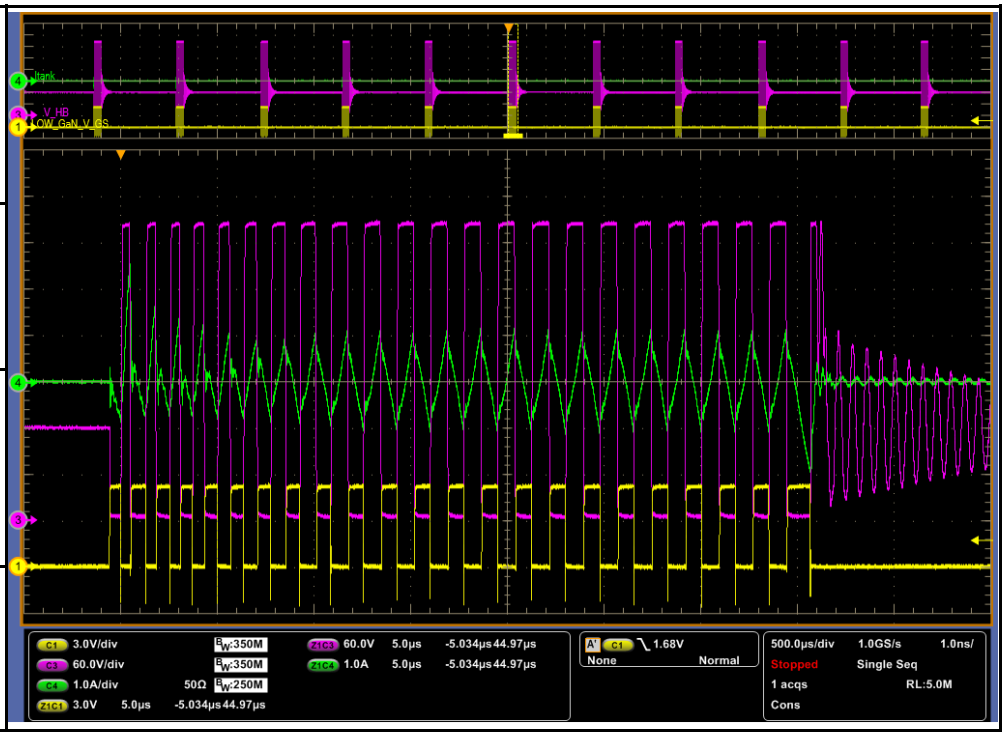
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 39. Primary Side, LLC Stage Burst Waveforms at Load 2 W (~ 100 mA)

Operating Waveforms during Burst

CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 40. Primary Side, LLC Stage Burst Waveforms at Load 7.7W (~ 400 mA)

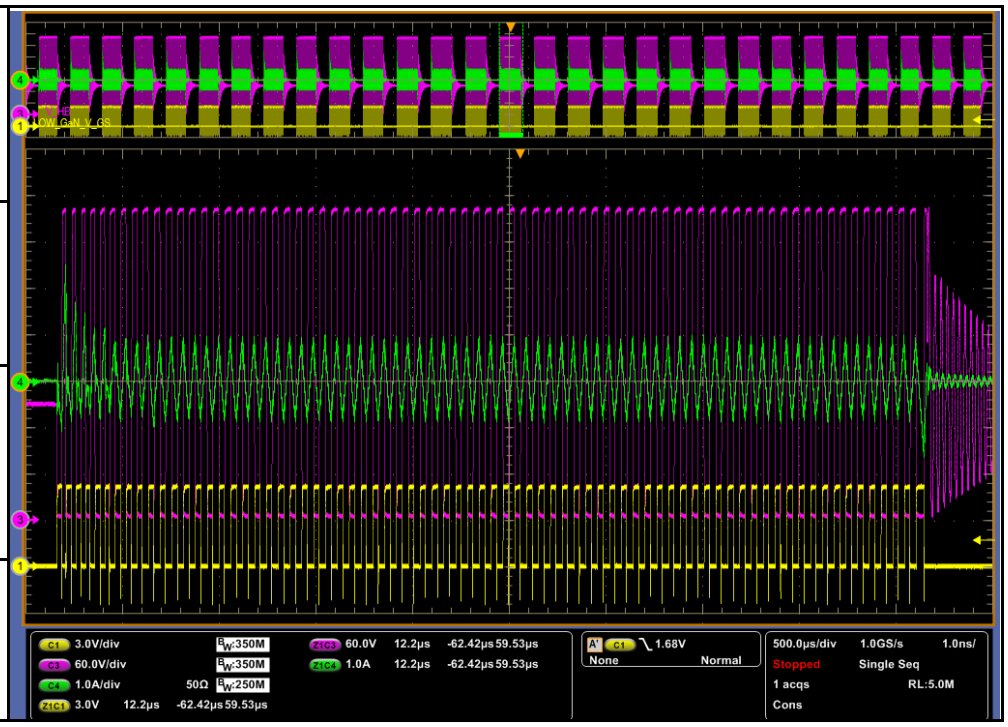
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 41. Primary Side, LLC Stage Burst Waveforms at Load 19 W (~ 1 A)

Operating Waveforms during Normal Mode at Loads: 30 and 100 W

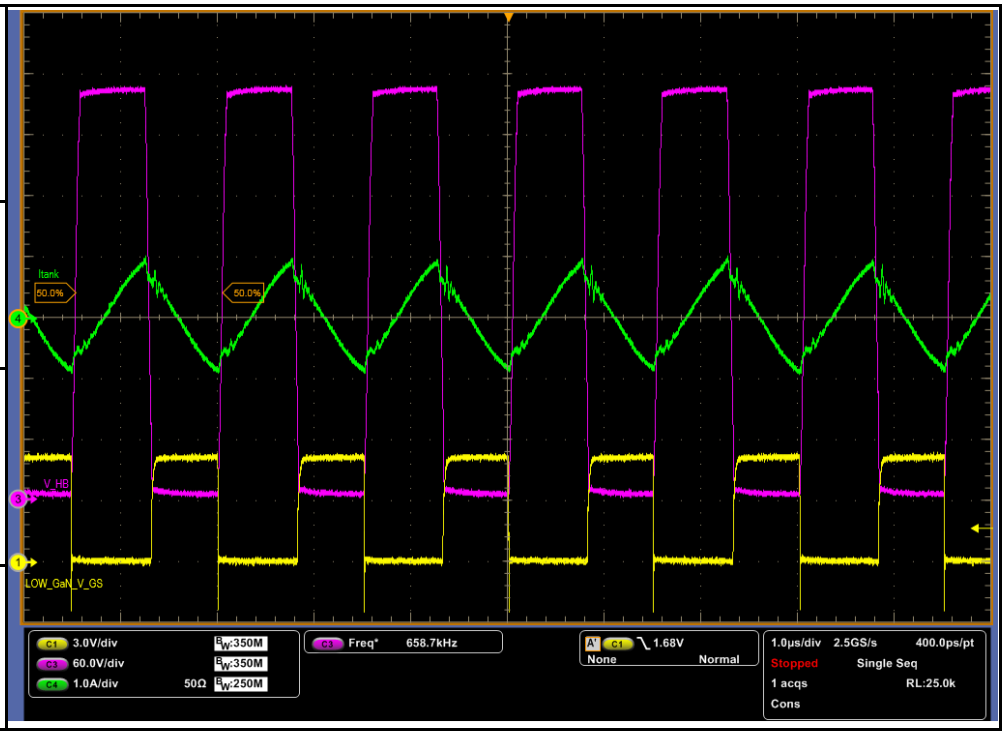
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 42. Primary Side, LLC Stage Normal Mode Waveforms at Load ~40 W (~ 2.0 A)

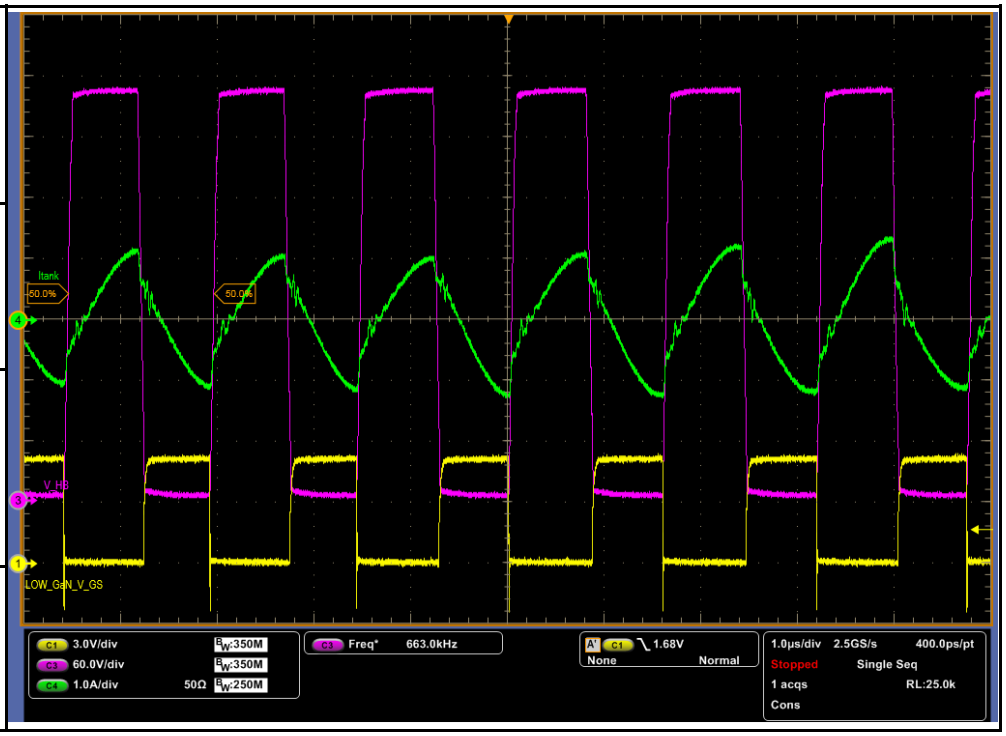
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 43. Primary Side, LLC Stage Normal Mode Waveforms at Load 100 W (~5 A)

Operating Waveforms During Normal Mode at Loads: 200 and 310 W

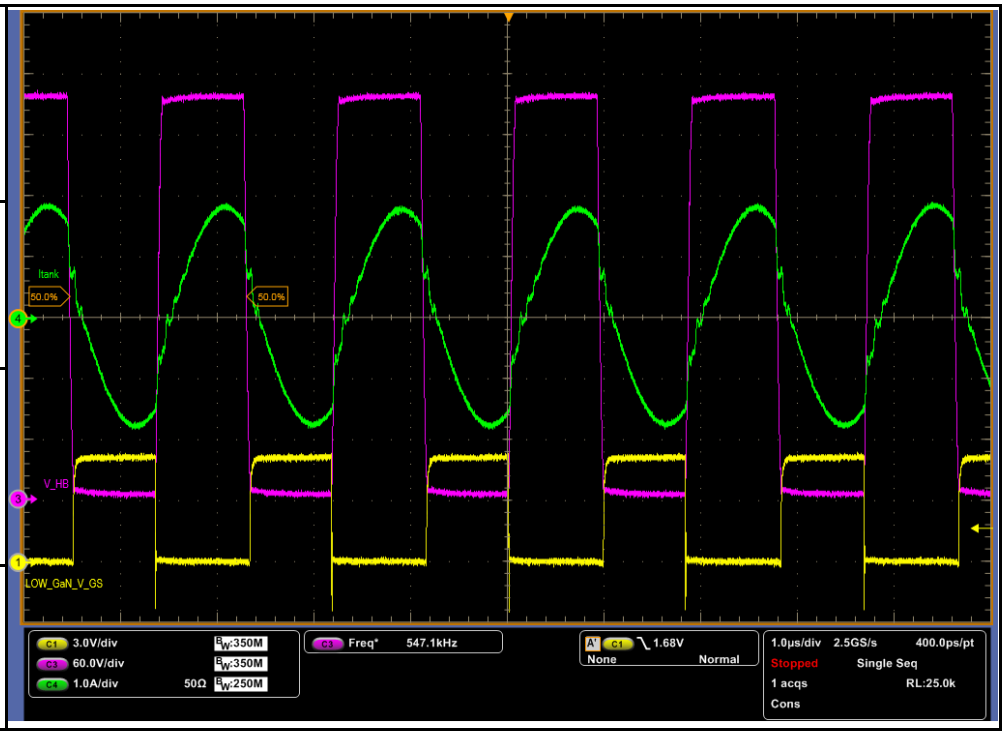
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 44. Primary Side, LLC Stage Normal Mode Waveforms at Load 190 W (~10 A)

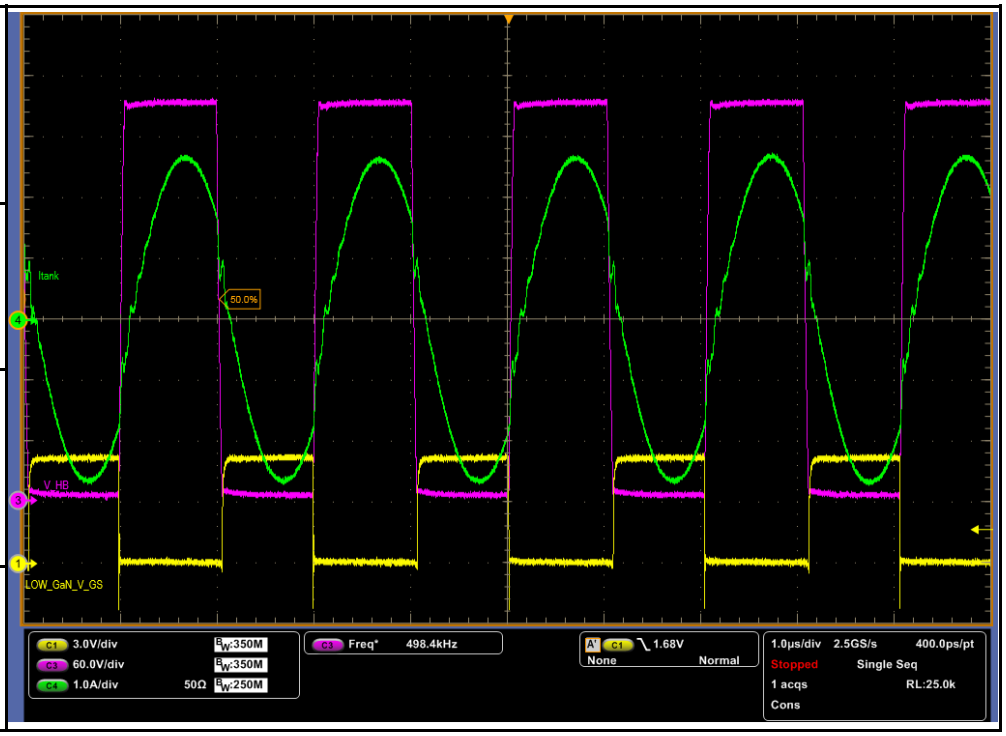
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 45. Primary Side, LLC Stage Normal Mode Waveforms at Load 310 W (~16 A)

Operating Waveforms during Normal Mode at Extreme Load: 350 W

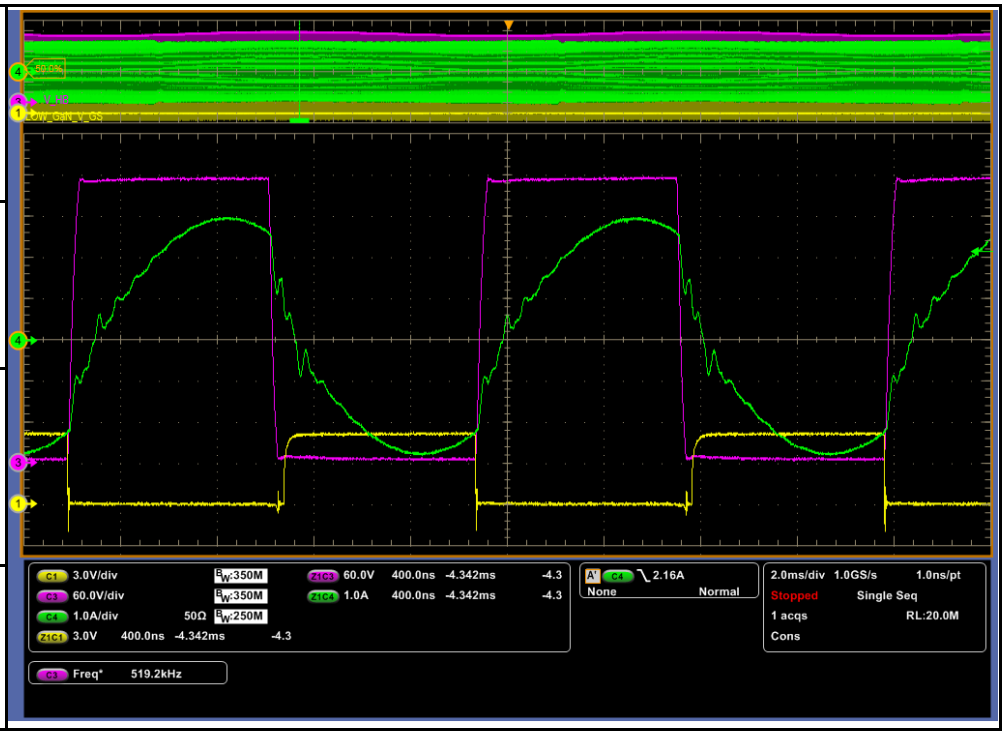
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 46. Primary Side, LLC Stage Normal Mode Waveforms at Load 350 W & Vbulk Max (~18 A)

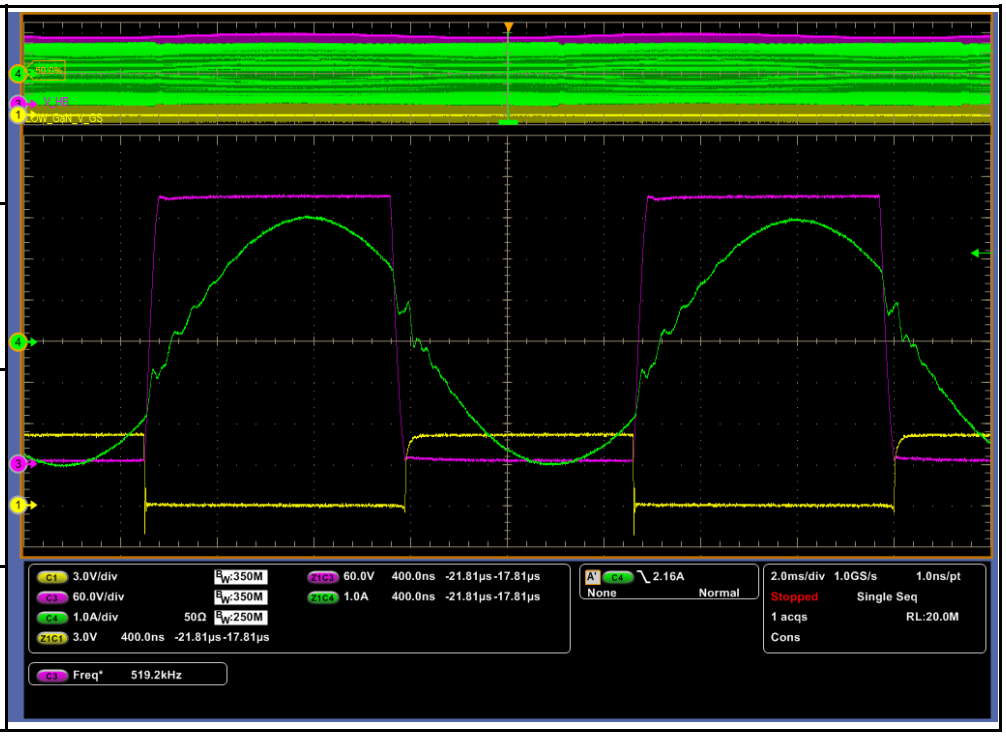
CH1: Q405 Gate drive voltage, 3 V/div	
CH2: N/A	
CH3: LLC HB node voltage, 60 V/div	
CH4: LLC resonant tank current, 1 A/div	

Figure 47. Primary Side, LLC Stage Normal Mode Waveforms at Load 380 W & Vbulk Min

Secondary Side Synchronous Rectifier Operating Waveforms during Burst

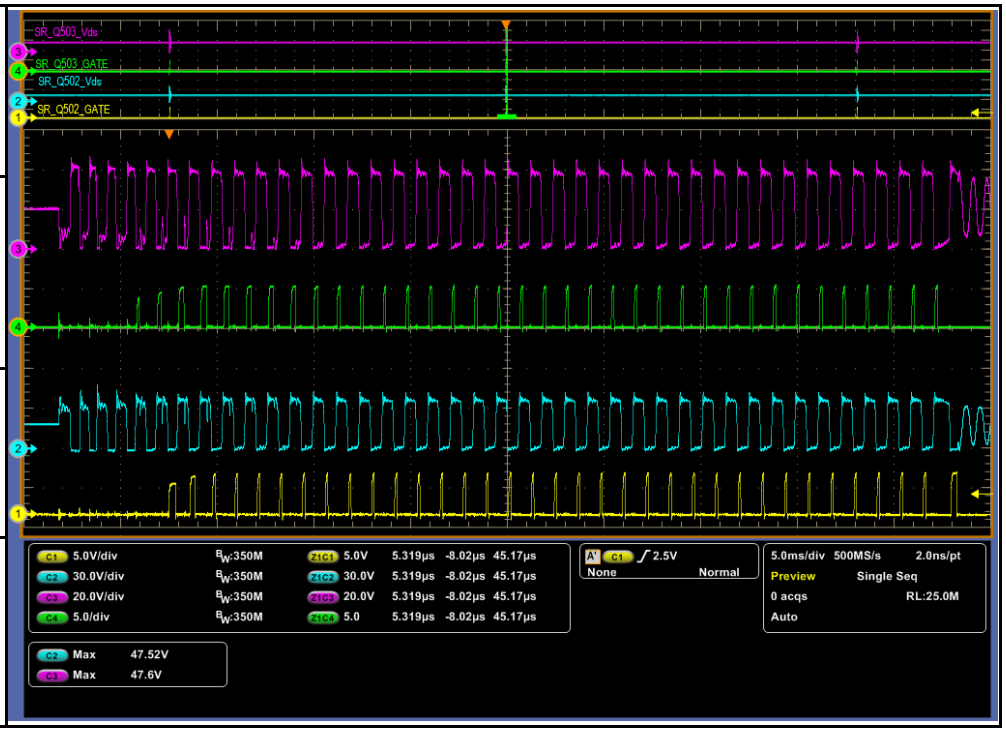
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 48. Secondary Side Synchronous Rectifier Driving Pulses at Load 0 W

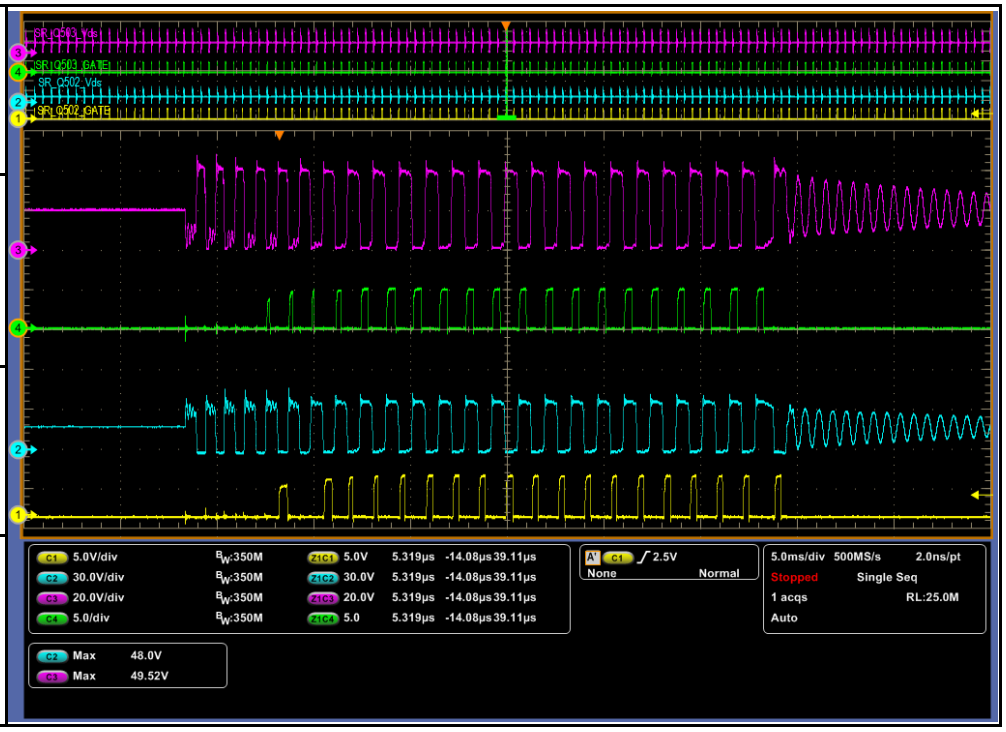
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 49. Secondary Side Synchronous Rectifier Driving Pulses at Load 2 W

Secondary Side Synchronous Rectifier Operating Waveforms during Burst

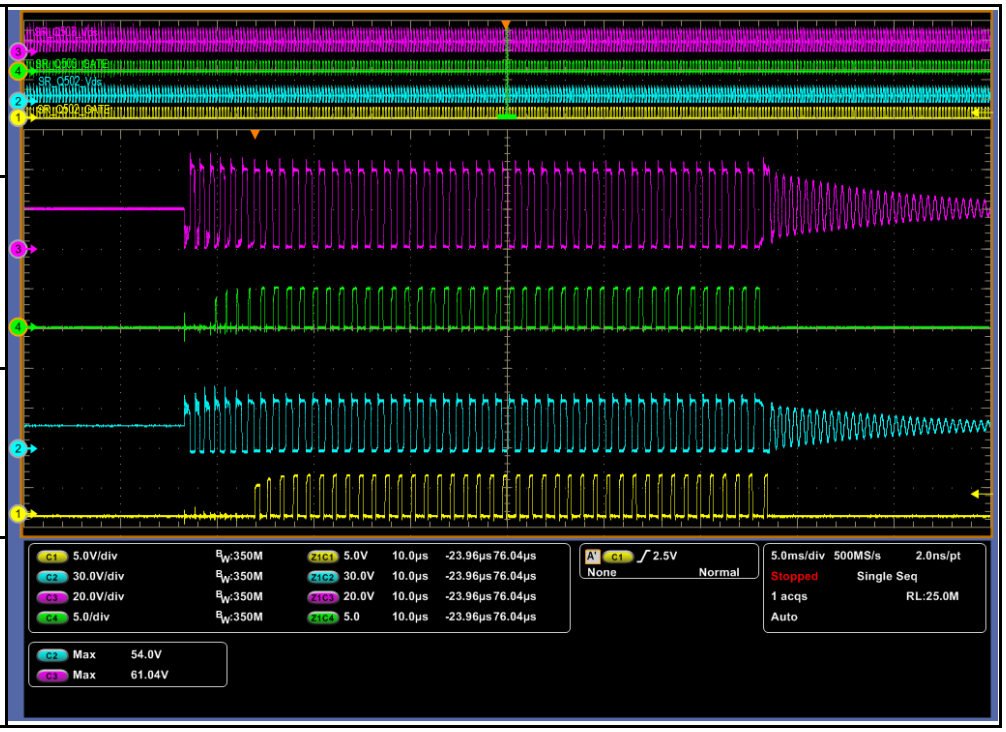
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 50. Secondary Side Synchronous Rectifier driving Pulses at Load 10 W (~ 500 mA)

CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 51. Secondary Side Synchronous Rectifier Driving Pulses at 19 W (1 A)

Secondary Side Synchronous Rectifier Operating Waveforms during Normal Mode at Loads: 60 and 100 W

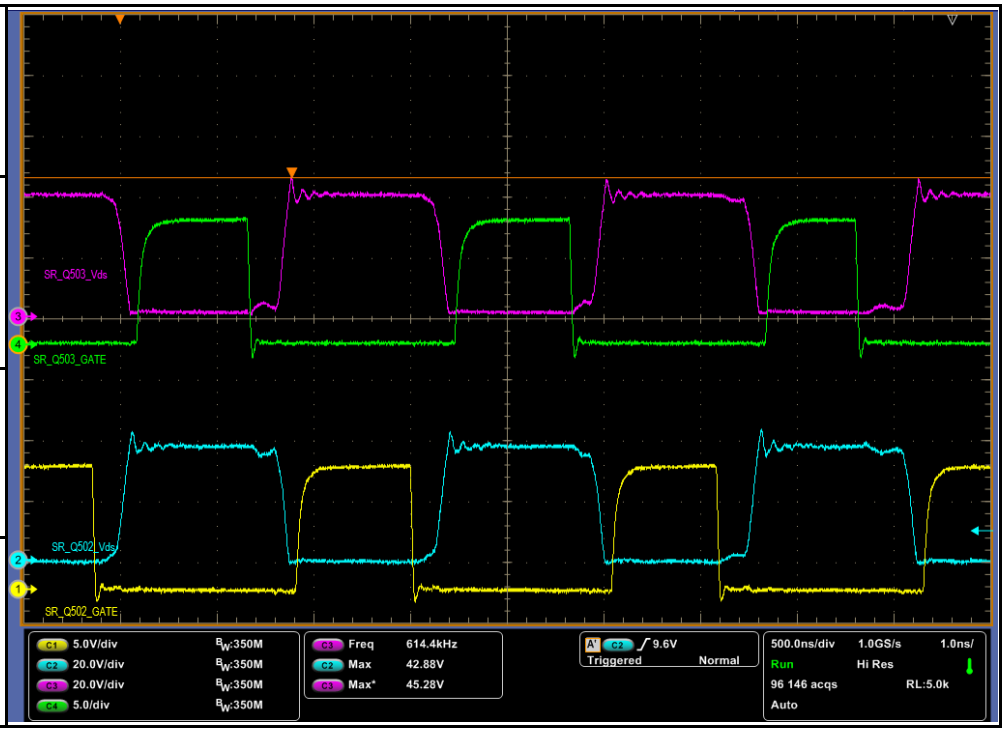
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 52. Secondary Side Synchronous Rectifier driving Pulses at Load 60 W

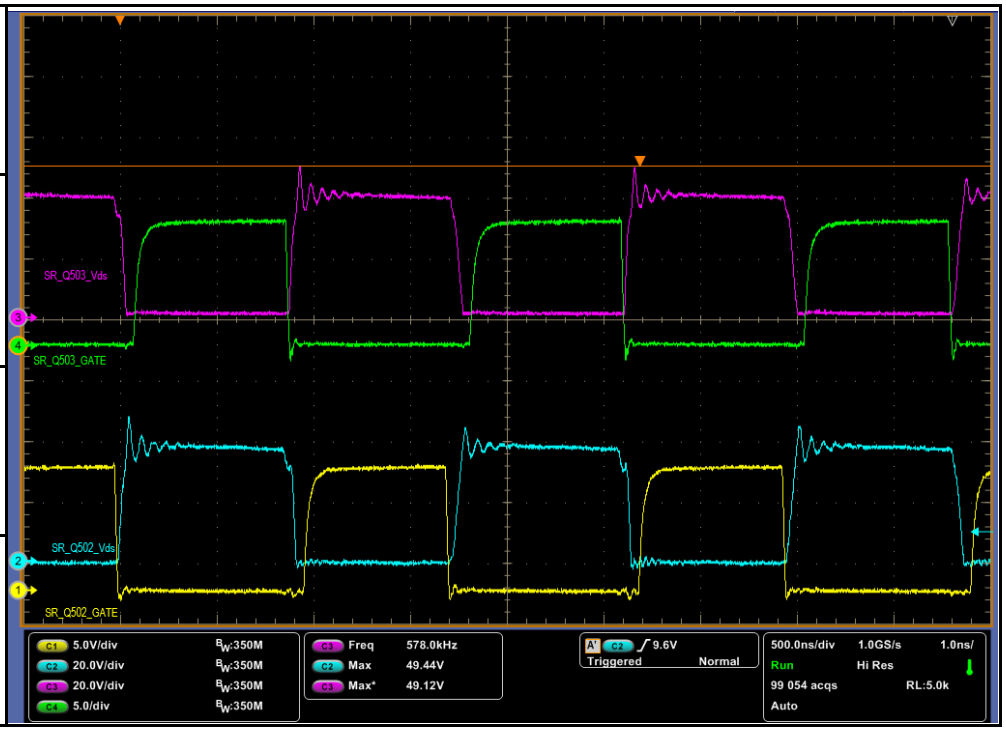
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 53. Secondary Side Synchronous Rectifier driving Pulses at Load 100 W

Secondary Side Synchronous Rectifier Operating Waveforms during Normal Mode at Loads: 200 and 310 W

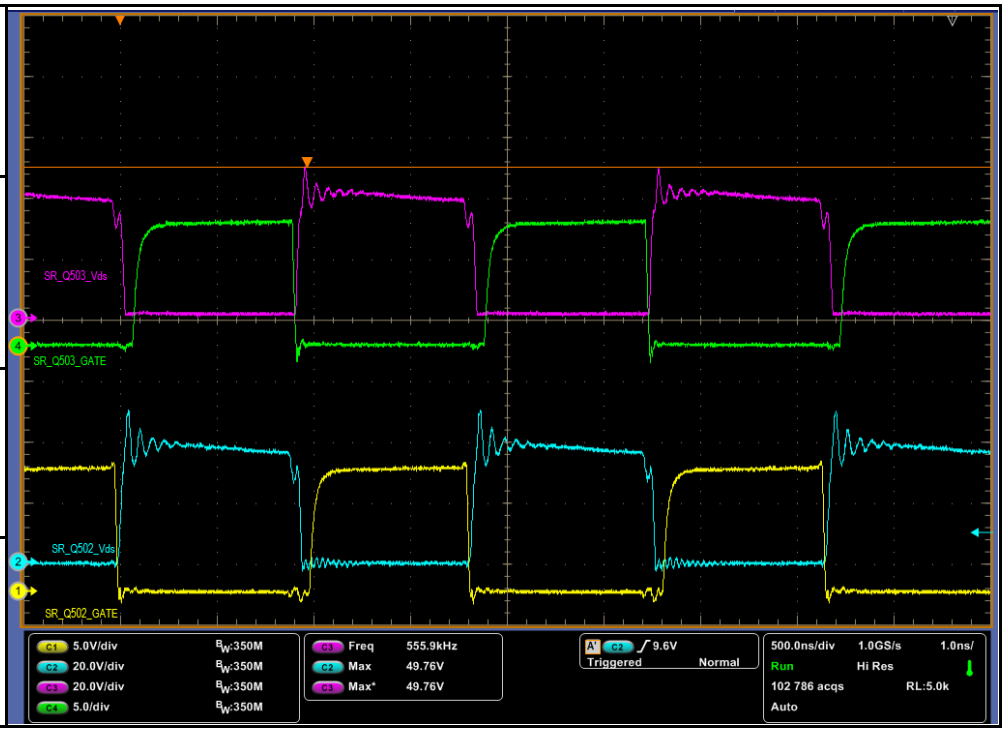
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 54. Secondary Side Synchronous Rectifier Driving Pulses at Load 200 W

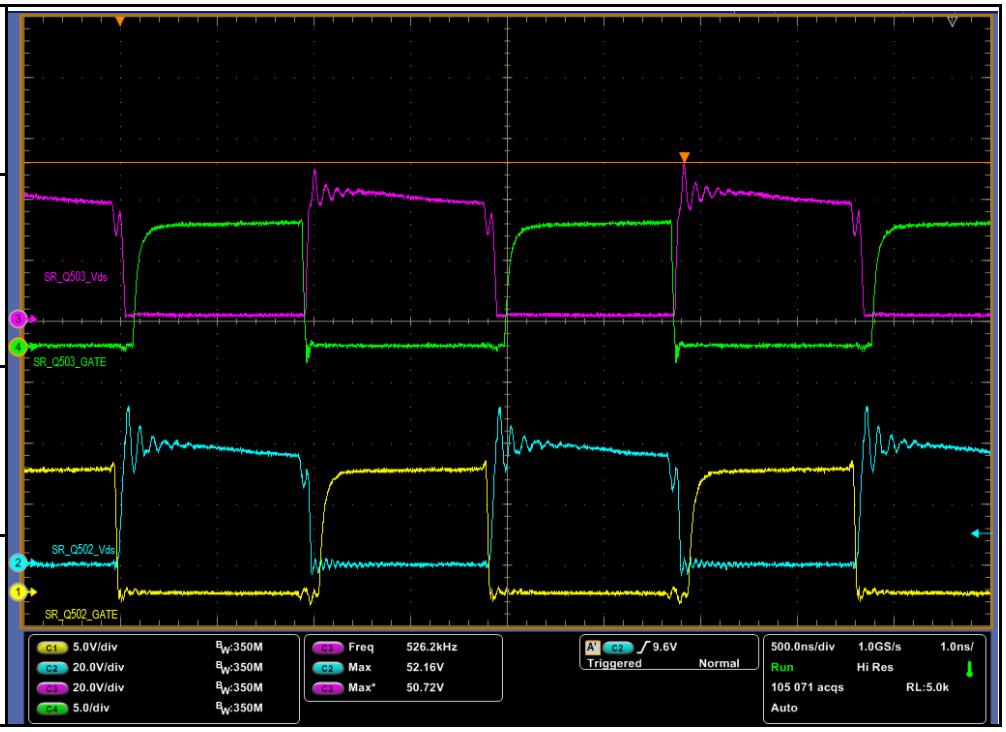
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 55. Secondary Side Synchronous Rectifier Driving Pulses at Load 310 W

Secondary Side Synchronous Rectifier Operating Waveforms during Normal Mode at Extreme Loads: 340 and 380 W

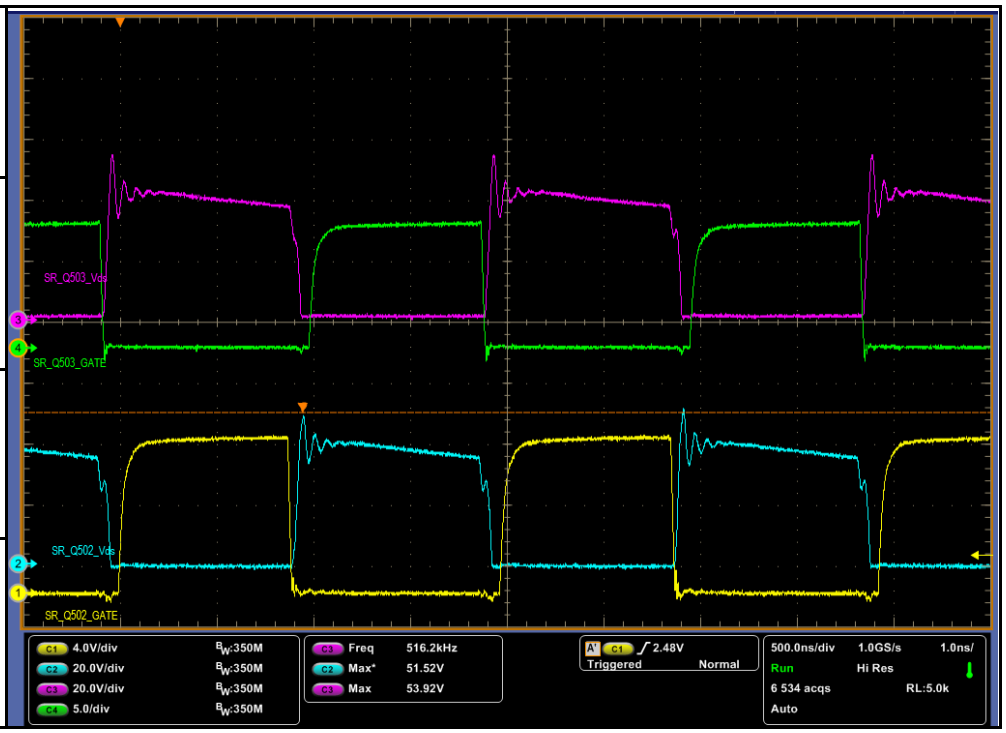
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 56. Secondary Side Synchronous Rectifier driving Pulses at Load 340 W

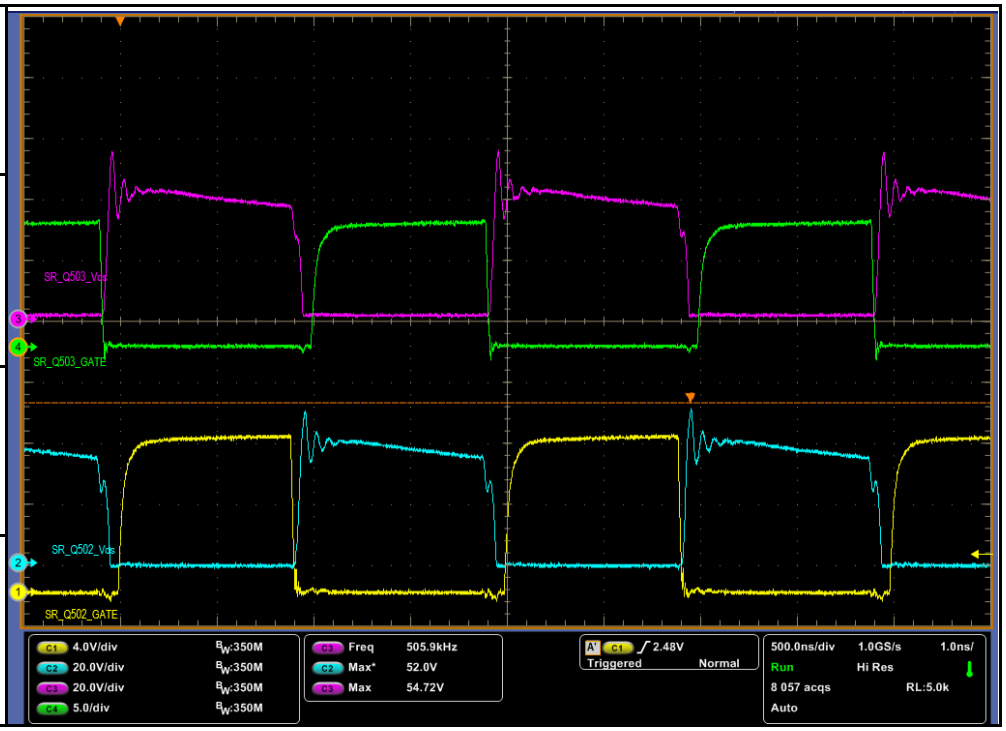
CH1: Q502−4 Gate drive voltage, 5 V/div	
CH2: Q502−4 Drain−source voltage, 20 V/div	
CH3: Q503−5 Gate drive voltage, 5 V/div	
CH4: Q502−4 Drain−source voltage, 20 V/div	

Figure 57. Secondary Side Synchronous Rectifier driving Pulses at Load 380 W

PFC Stage Operating Waveforms at Input Voltage 110 V C and Loads: 20 and 100 W

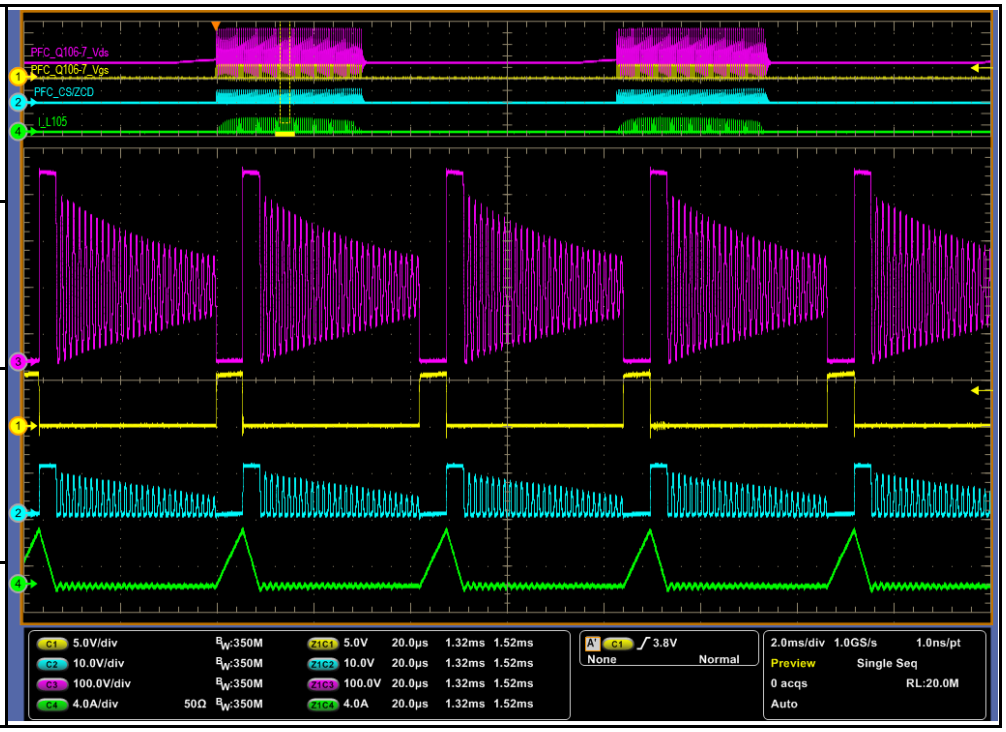
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 58. PFC Stage Skip Mode at 110 V AC and Load 20 W

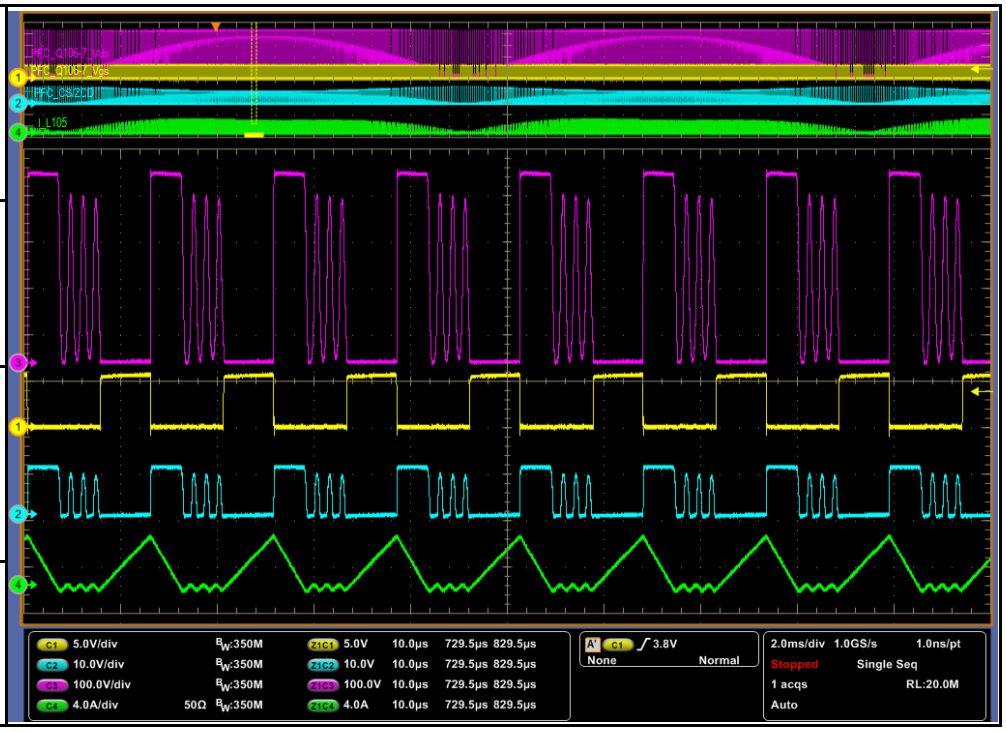
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 59. PFC Stage Normal Mode at 110 V AC and Load 100 W

PFC Stage Operating Waveforms at Input Voltage 110 V AC and loads: 20 and 100 W

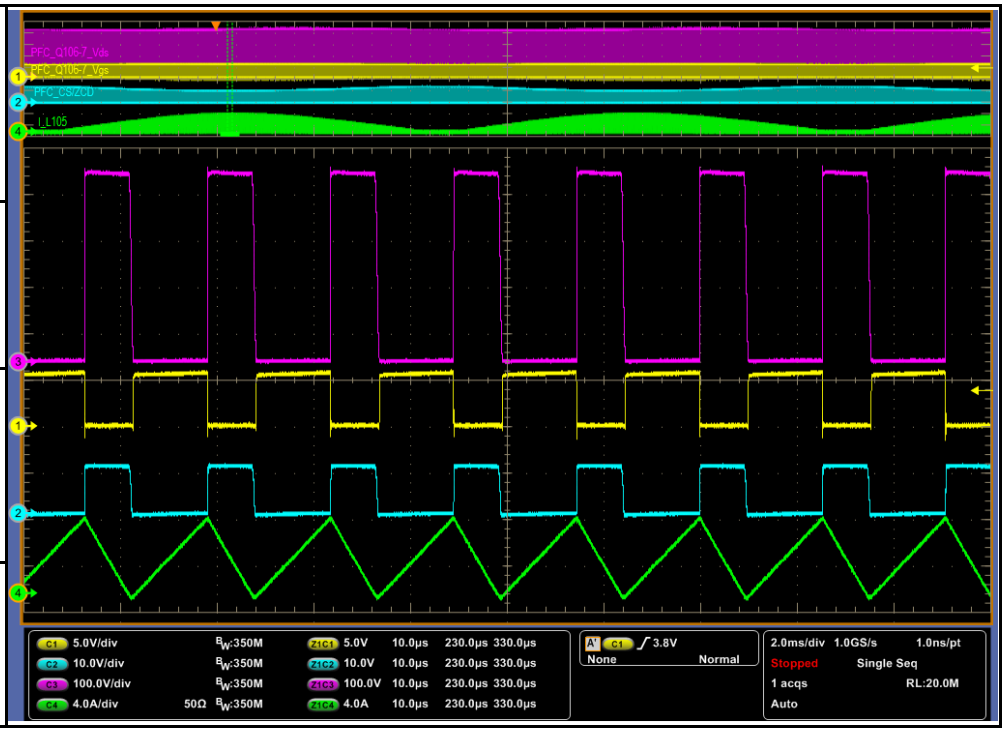
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 60. PFC Stage Normal Mode at 110 V AC and Load 200 W

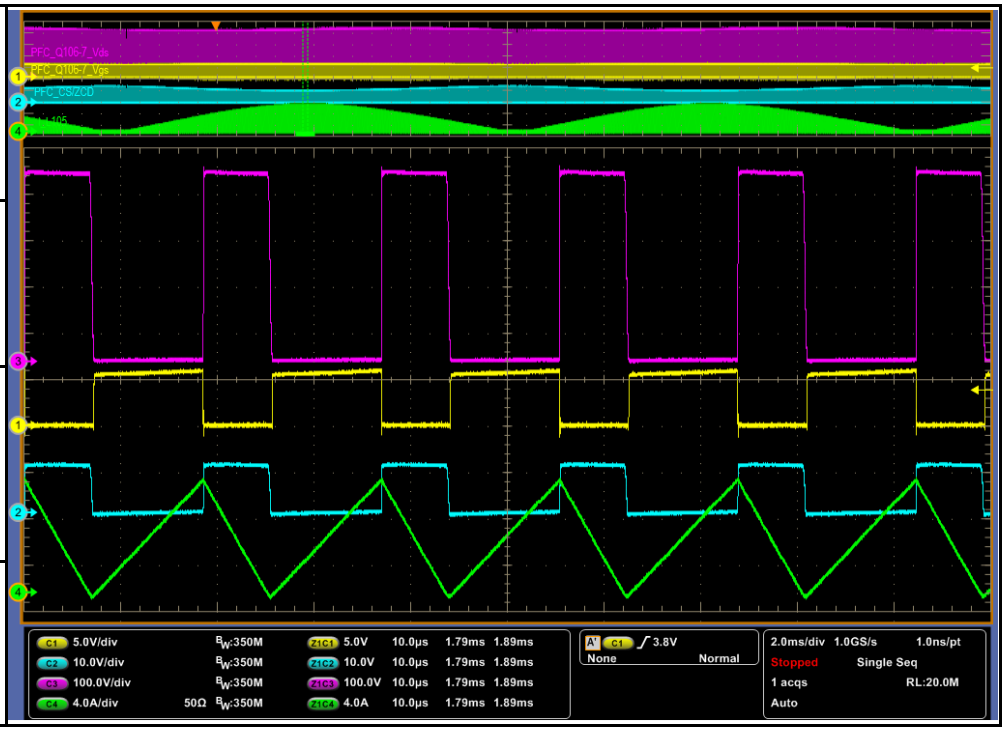
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 61. PFC Stage Normal Mode at 110 V AC and Load 310 W

PFC Stage Operating Waveforms at Input Voltage 230 V AC and Loads: 20 and 100 W

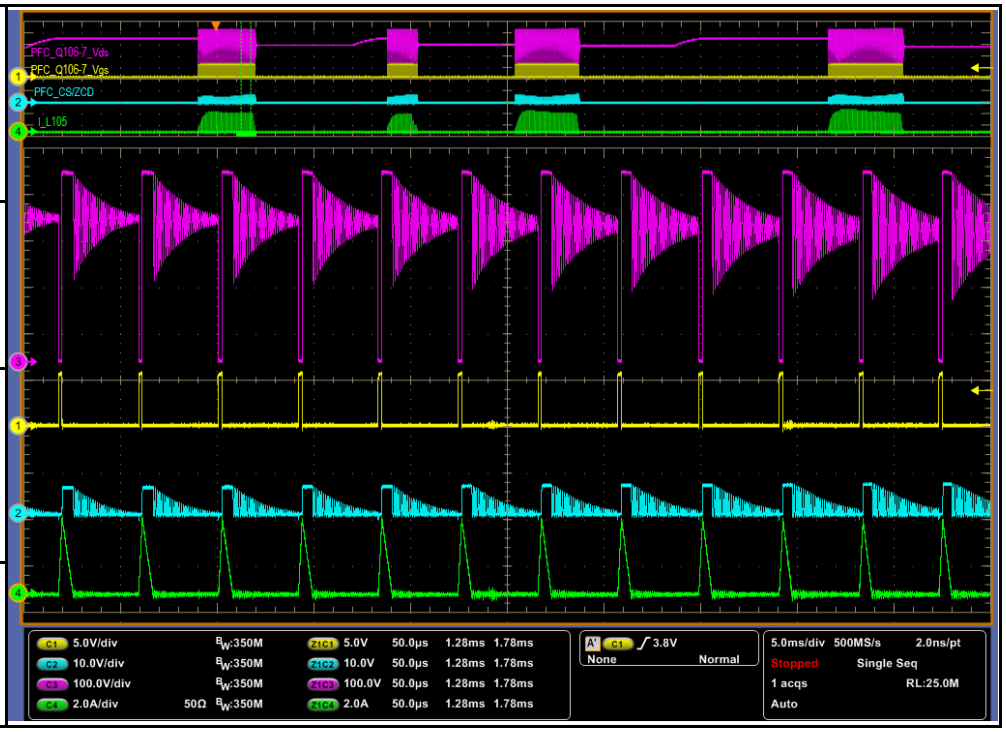
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 62. PFC Stage Skip Mode at 230 V AC and Load 20 W

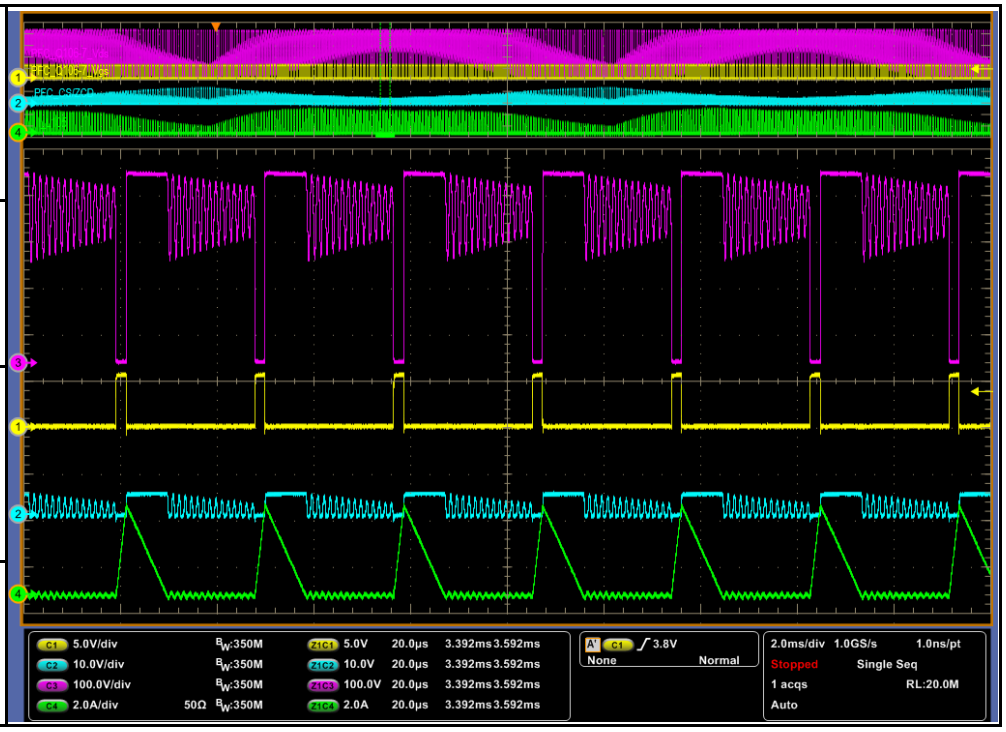
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 63. PFC Stage Normal Mode at 230 V AC and Load 100 W

PFC Stage Operating Waveforms at Input Voltage 230 V AC and Loads: 200 and 310 W

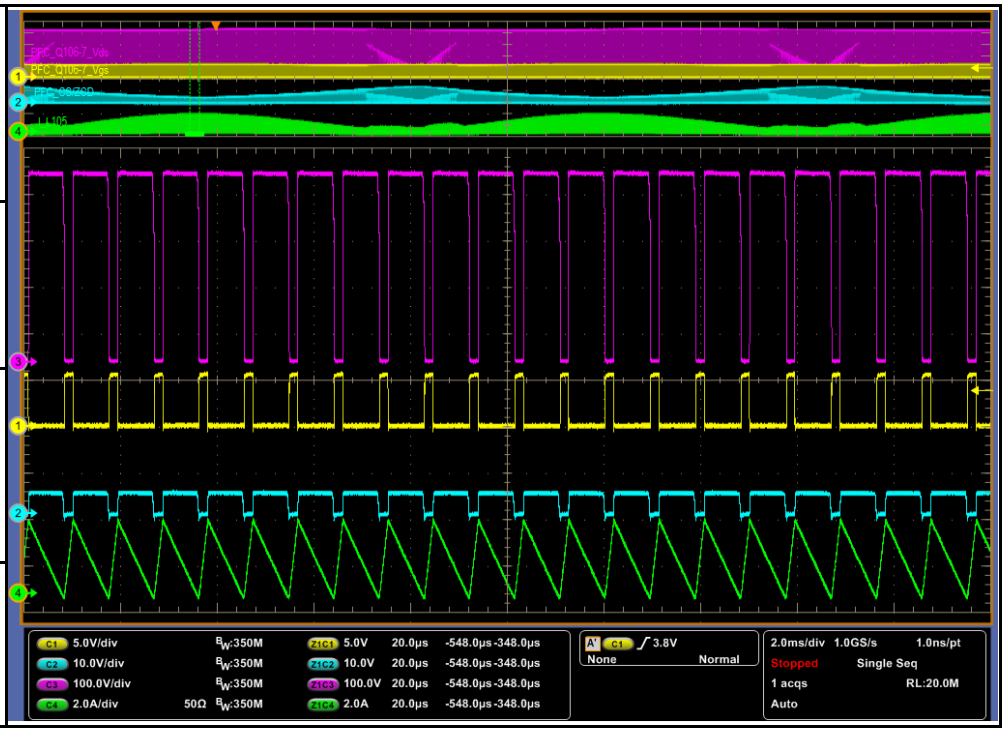
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 64. PFC Stage Normal Mode at 230 V AC and Load 200 W

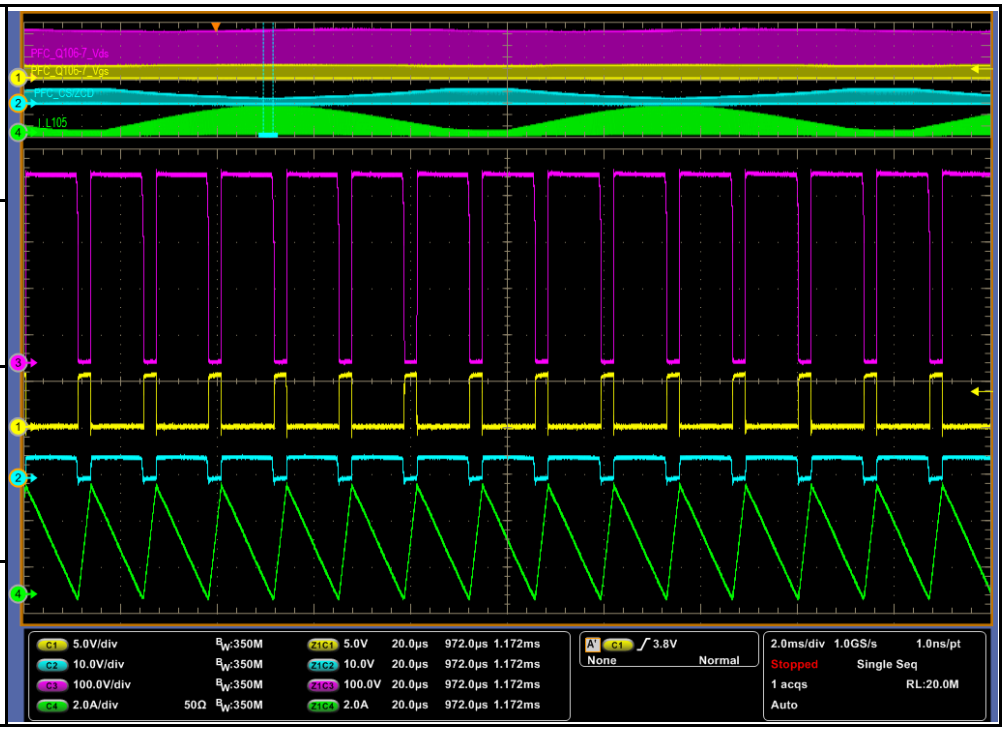
CH1: PFC GaN Q106−7 Gate drive voltage, 5 V/div	
CH2: PFC ZCD voltage 10 V/div	
CH3: PFC GaN Q106−7 Drain−source voltage, 100 V/div	
CH4: L105 − PFC inductor current, 4 A/div	

Figure 65. PFC Stage Normal Mode at 230 V AC and Load 310 W

Waveforms Captured during Applied Step Load. Measured at 110 V AC

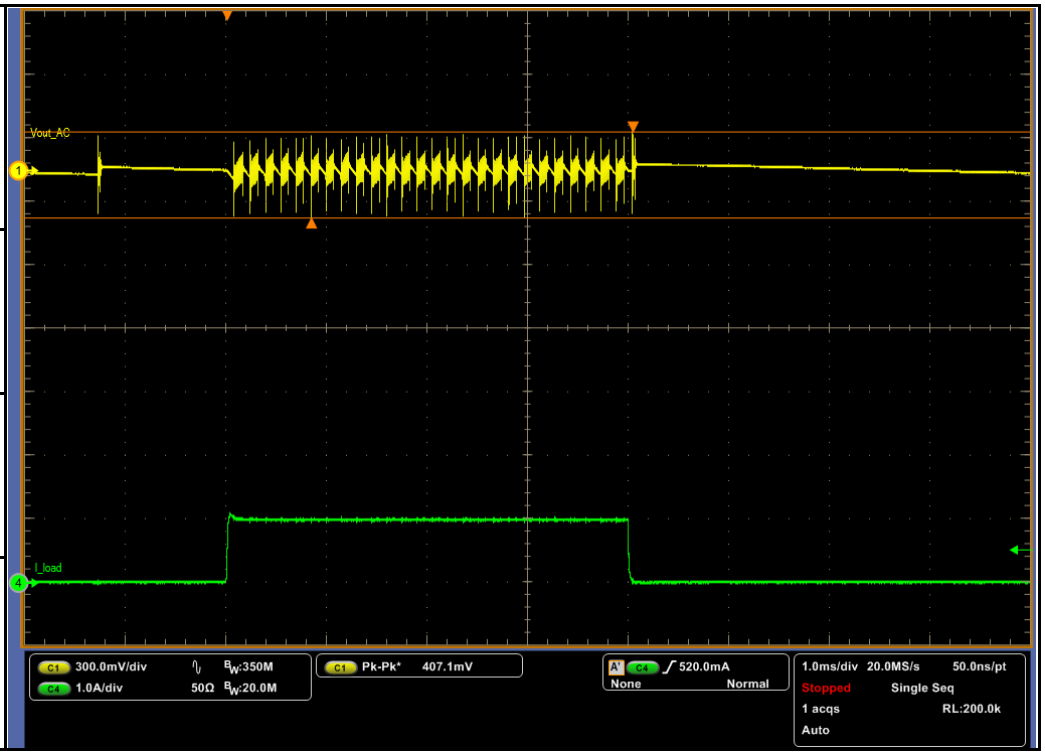
CH1: Output voltage, AC coupled 300 mV/div	
CH2: N/A	
CH3: N/A	
CH4: Output load current, 1 A/div	

Figure 66. Output Voltage Step Load Response: 0 to 1 A (19 W)

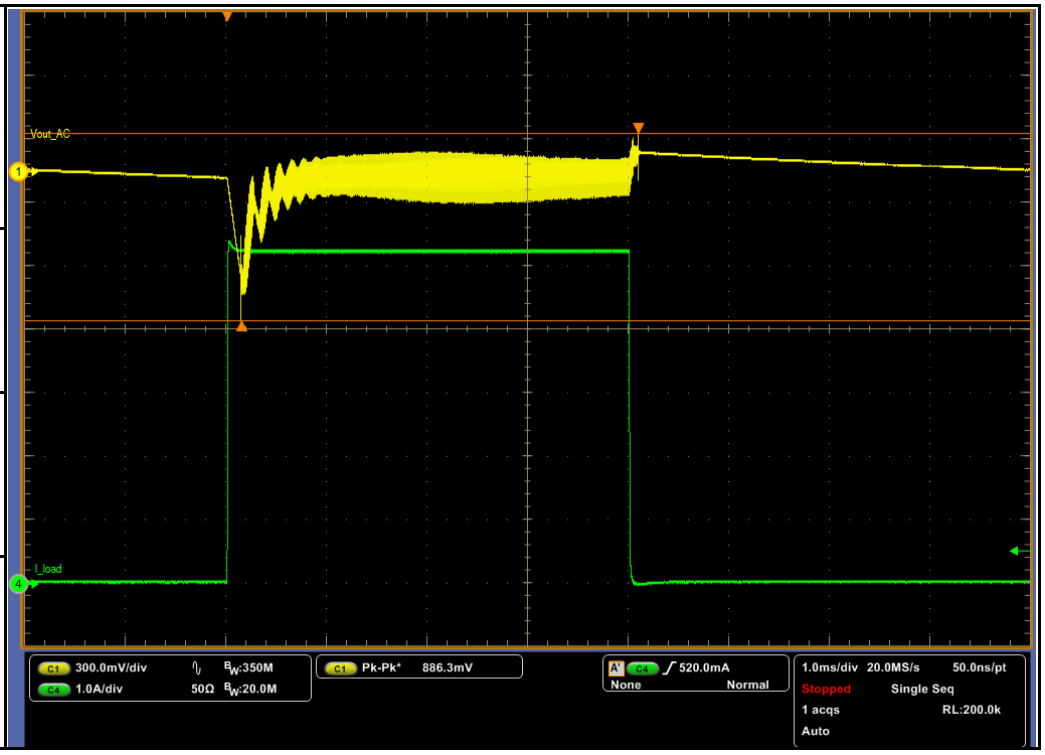
CH1: Output voltage, AC coupled 300 mV/div	
CH2: N/A	
CH3: N/A	
CH4: Output load current, 1 A/div	

Figure 67. Output Voltage Step Load Response: 0 to 5.25 A (100 W)

Waveforms Captured during Applied Step Load. Measured at 110 V AC

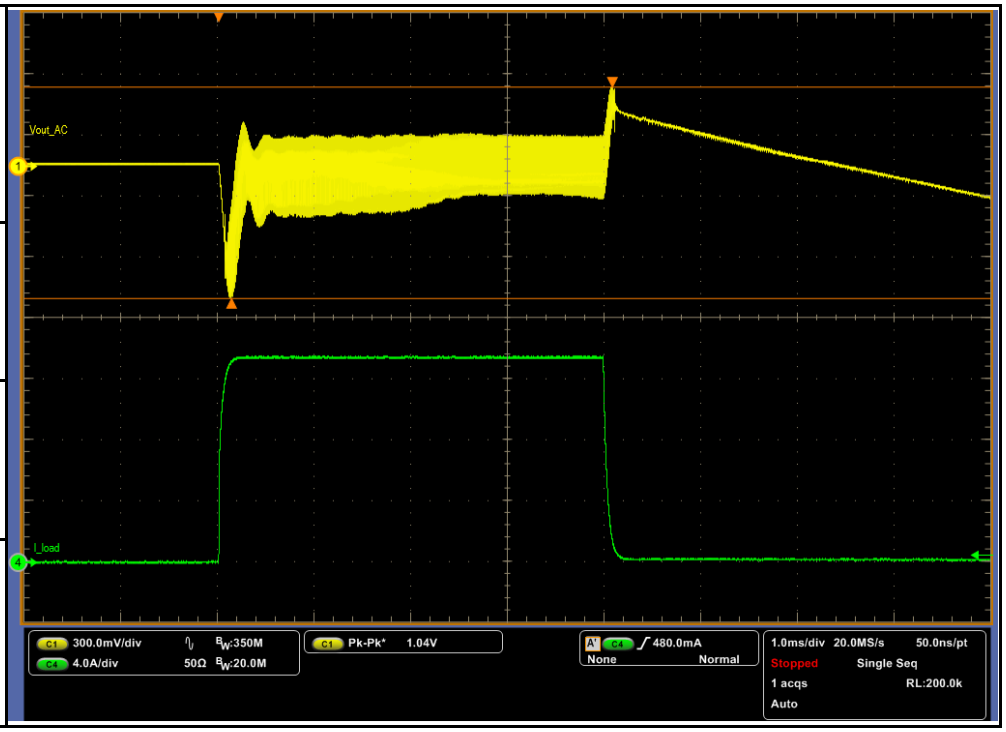
CH1: Output voltage, AC coupled 300 mV/div	
CH2: N/A	
CH3: N/A	
CH4: Output load current, 4 A/div	

Figure 68. Output Voltage Step Load Response: 0 to 13.2 A (200 W)

CH1: Output voltage, AC coupled 300 mV/div	
CH2: N/A	
CH3: N/A	
CH4: Output load current, 4 A/div	

Figure 69. Output Voltage Step Load Response: 0 to 16 A (300 W)

Waveforms Captured during Steady Load. Measured at 110 V AC

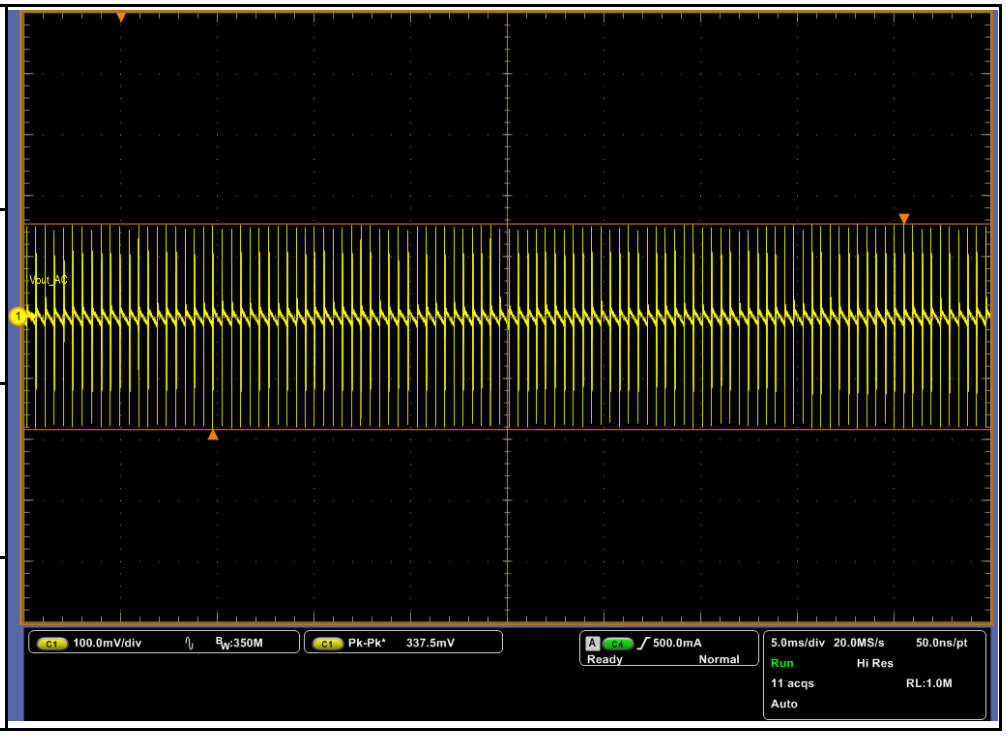
CH1: Output voltage, AC coupled 100 mV/div	
CH2: N/A	
CH2: N/A:	
CH2: N/A	

Figure 70. Output Voltage Ripple at Load 0.1 A

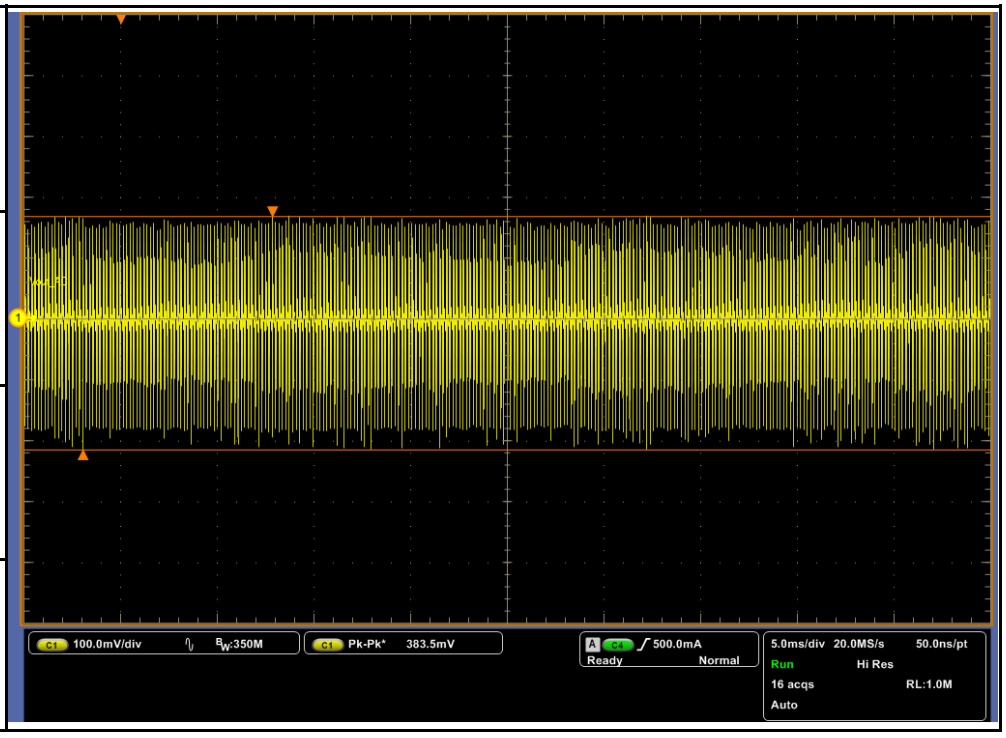
CH1: Output voltage, AC coupled 100 mV/div	
CH2: N/A	
CH2: N/A:	
CH2: N/A	

Figure 71. Output Voltage Ripple at Load 0.1 A

Waveforms Captured during Steady Load. Measured at 110 V AC

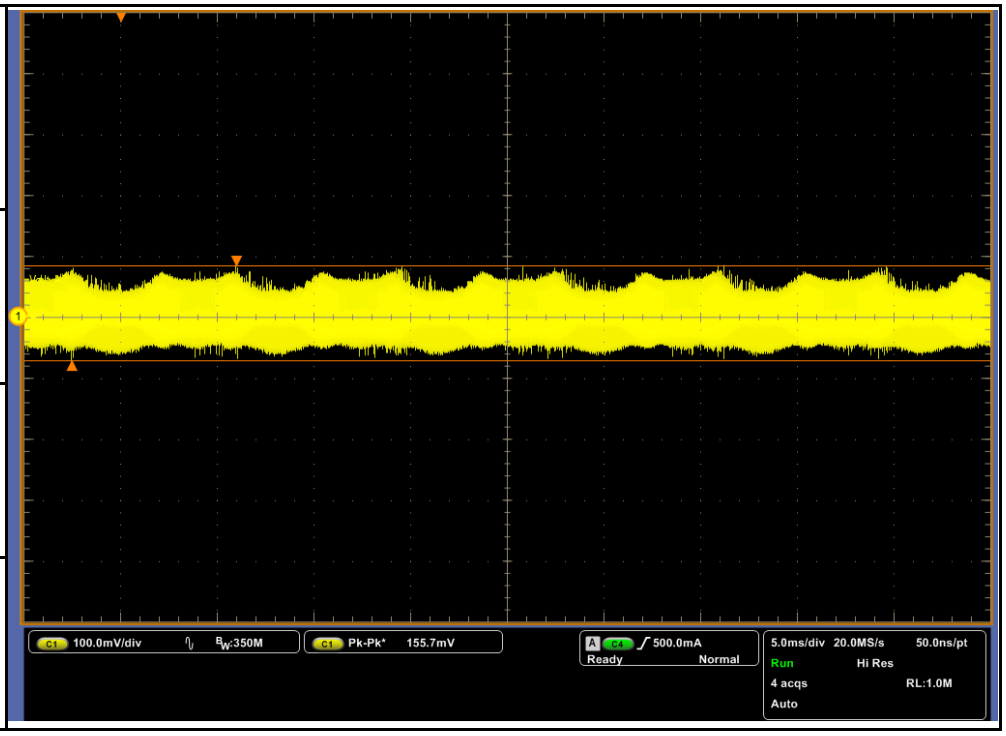
CH1: Output voltage, AC coupled 100 mV/div	
CH2: N/A	
CH2: N/A:	
CH2: N/A	

Figure 72. Output Voltage Ripple at Load 5.25 A (100 W)

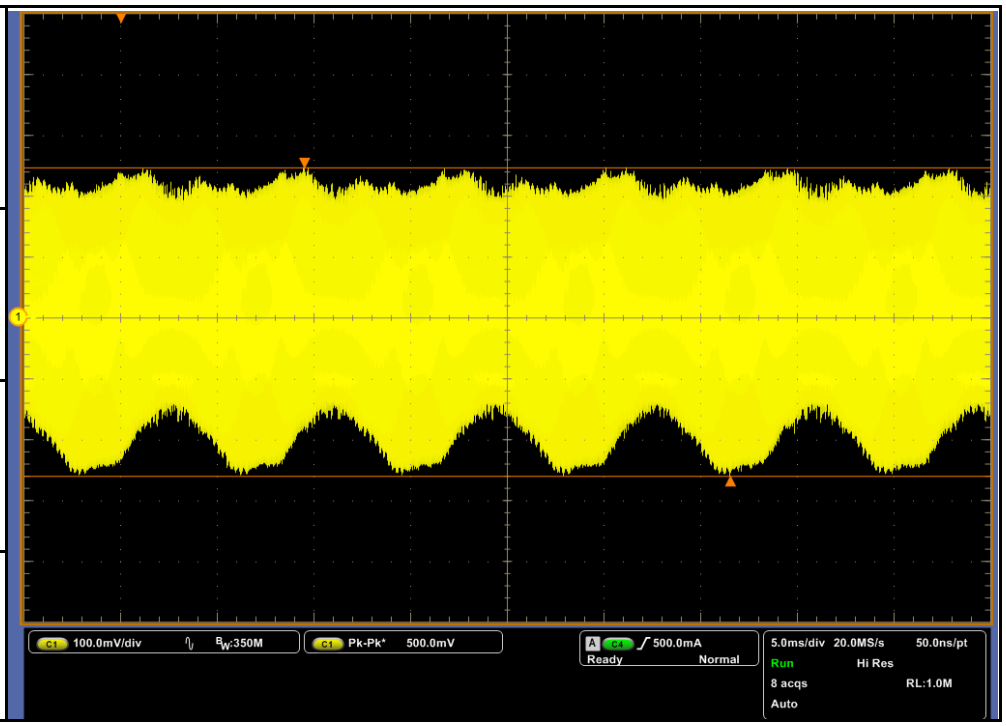
CH1: Output voltage, AC coupled 100 mV/div	
CH2: N/A	
CH2: N/A:	
CH2: N/A	

Figure 73. Output Voltage Ripple at Load 16 A (300 W)

Waveforms Captured during Start−up and Vout building at 110 V AC

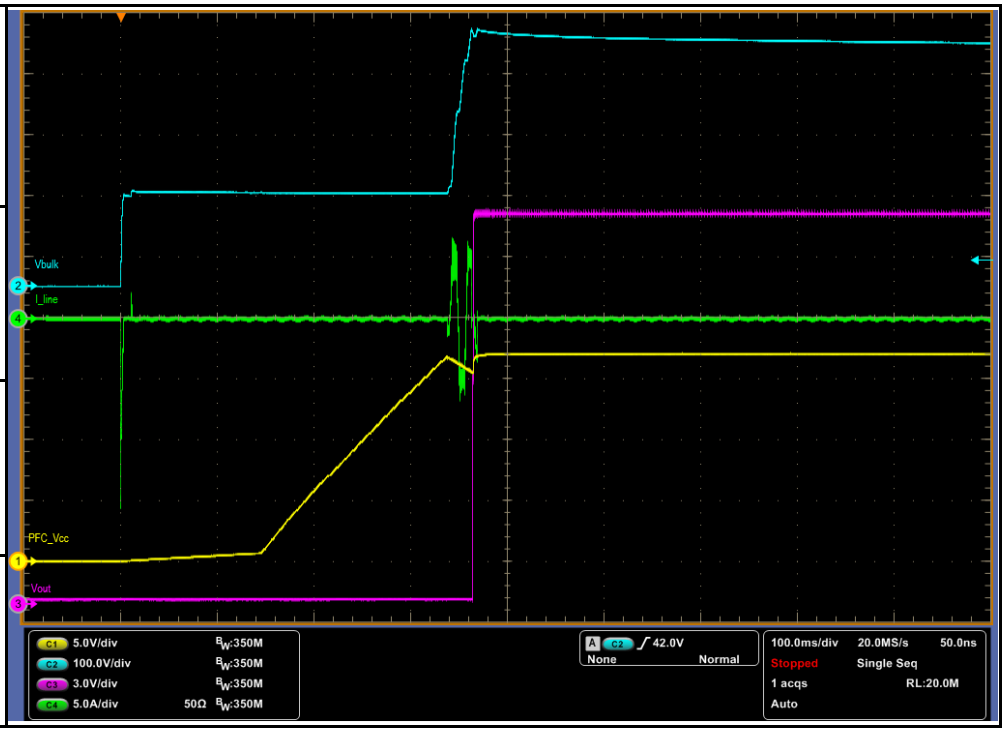
CH1: IC103 Vcc voltage, 5 V/div	
CH2: PFC Bulk capacitor voltage 100 V/div	
CH3: Output voltage, 3 V/div	
CH4: AC line current, 5 A/div	

Figure 74. Start−up Sequence without Loading (0 A)

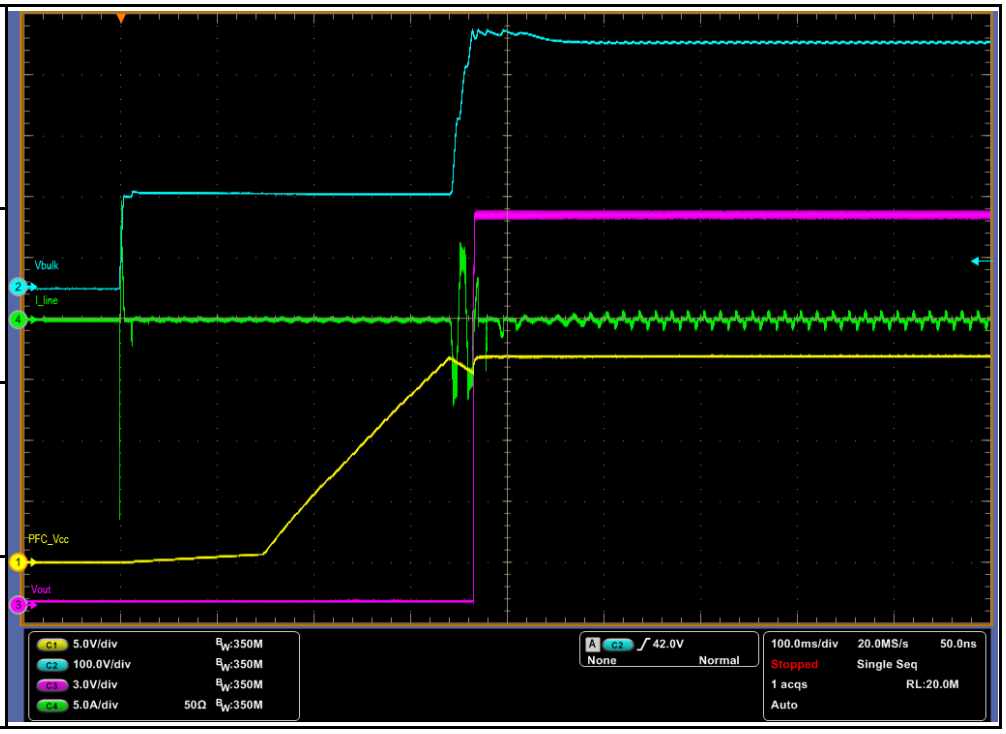
CH1: IC103 Vcc voltage, 5 V/div	
CH2: PFC Bulk capacitor voltage 100 V/div	
CH3: Output voltage, 3 V/div	
CH4: AC line current, 5 A/div	

Figure 75. Start−up Sequence into Constant Current Load 1 A / ≈ 19 W

Waveforms Captured during Start−up and Vout building at 110 V AC

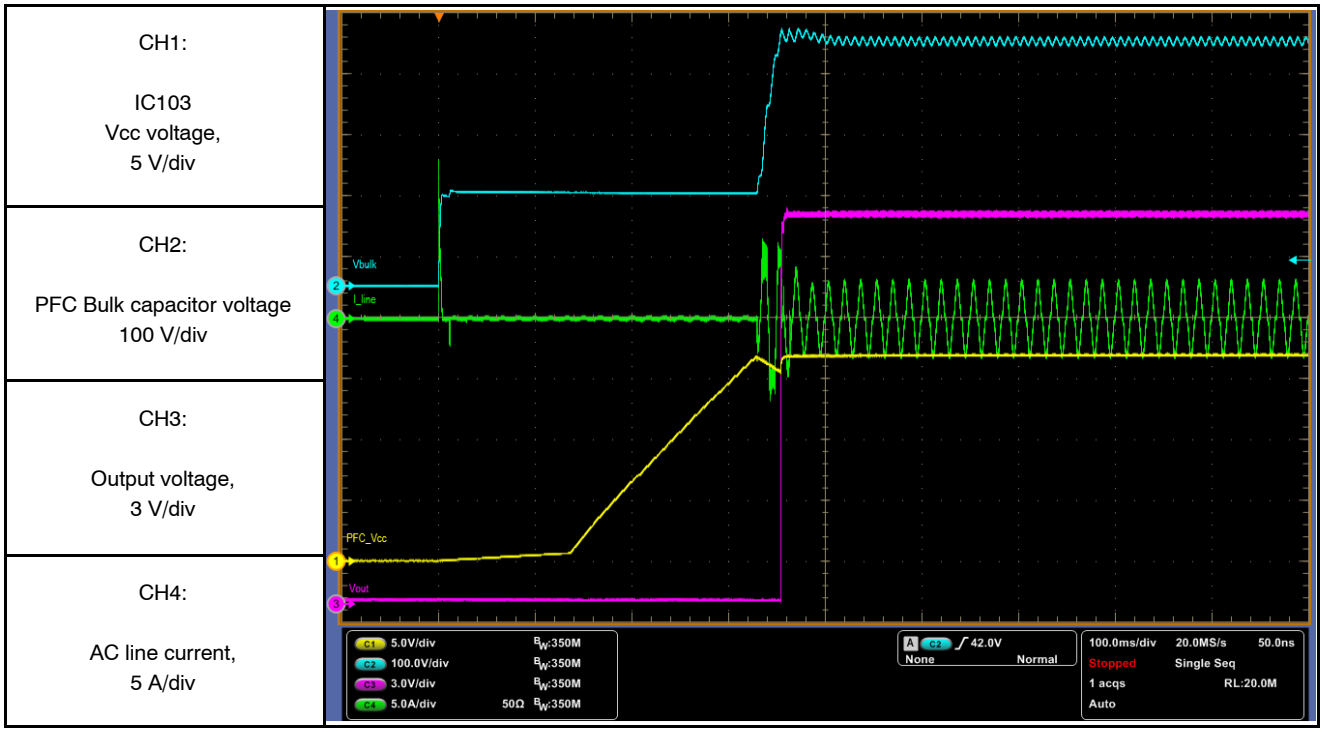


Figure 76. Start−up Sequence into Constant Current Load 5.25 A / ≈ 100 W

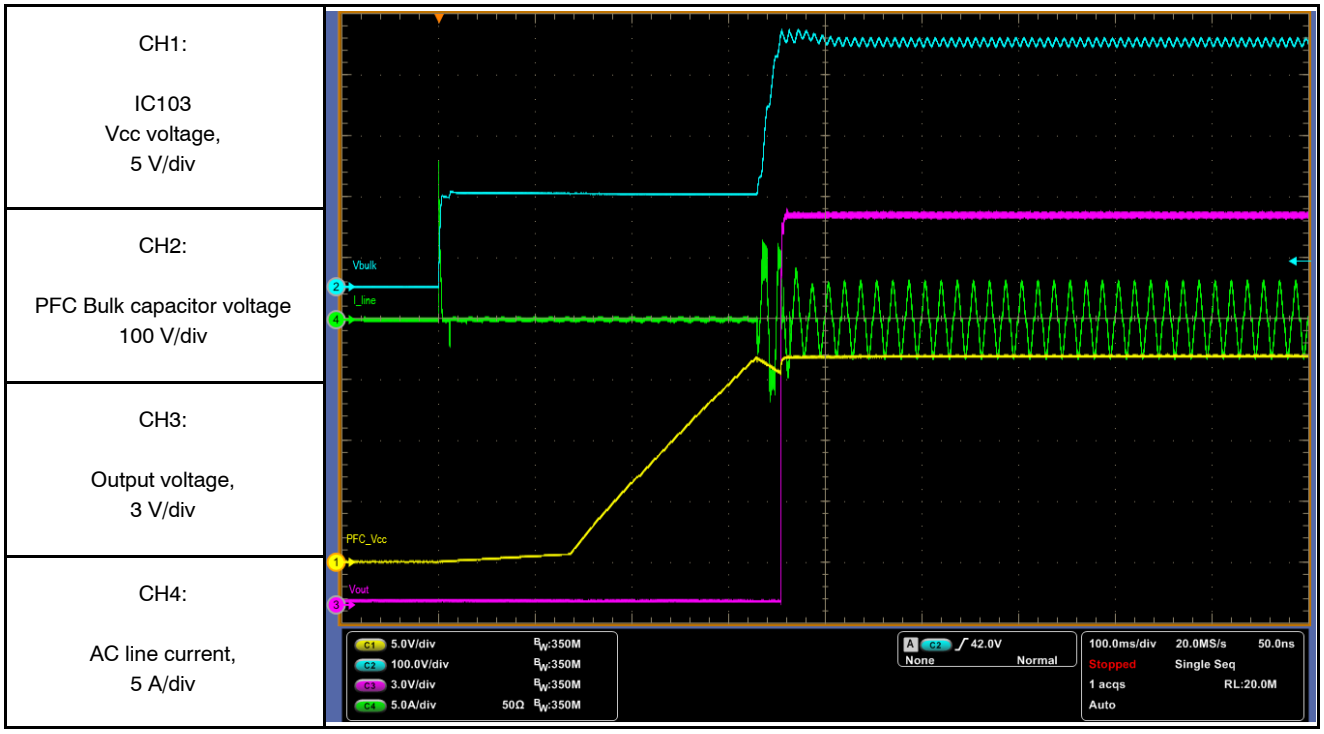


Figure 77. Start−up Sequence into Constant Current Load 10.5 A / ≈ 200 W

Waveforms Captured during Start−up and Vout building at 110 V AC

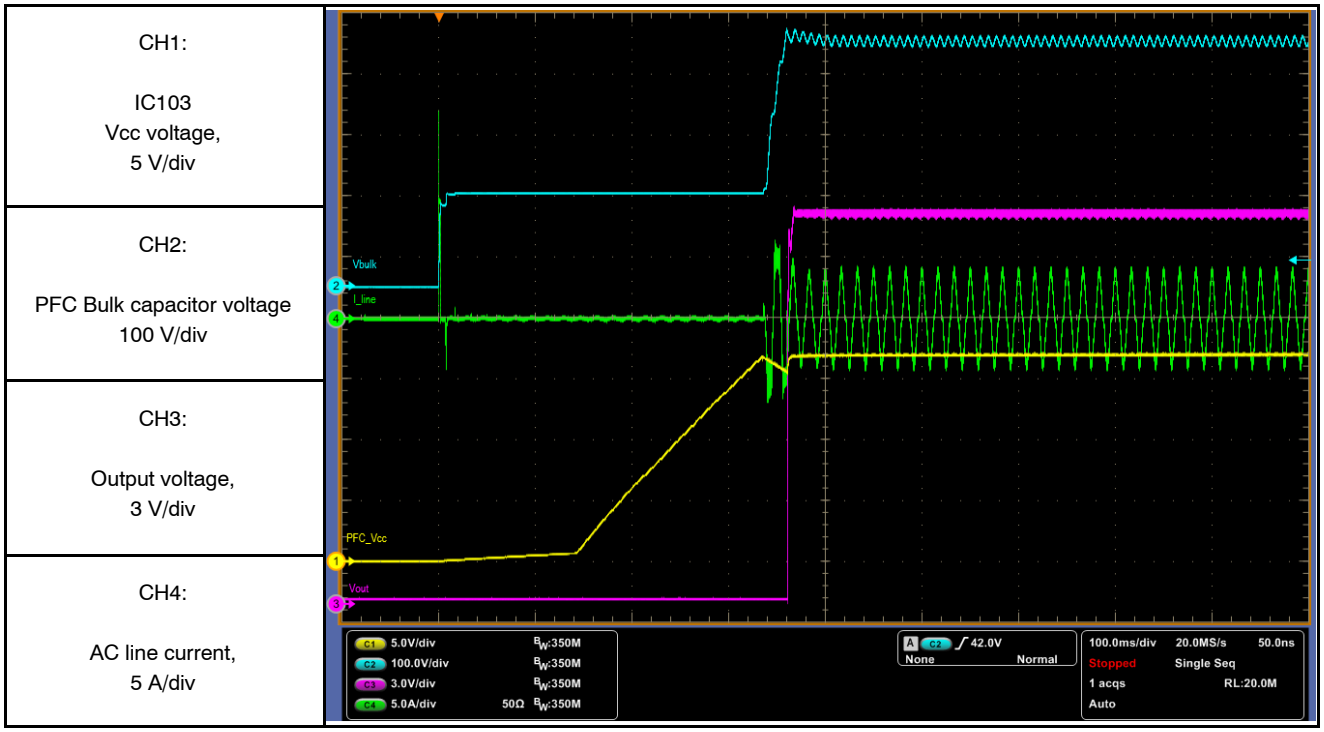


Figure 78. Start−up Sequence into Constant Current Load 13.2 A / ≈ 250 W

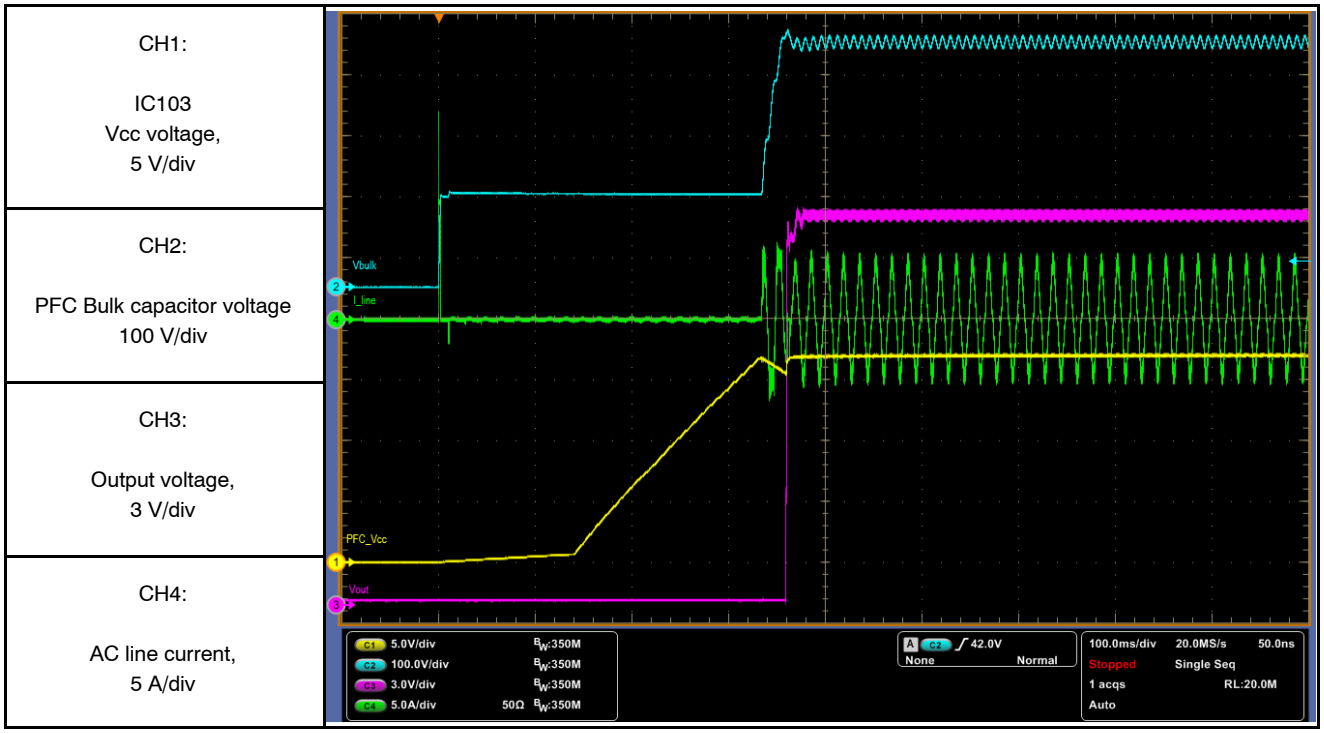


Figure 79. Start−up Sequence into Constant Current Load 16 A / ≈ 300 W

EMI INDUCTORS MODIFICATIONS

L101 is based on WURTH's 744823201 common mode inductors core. Follow up steps in Figure 80 and afore mentioned steps for desired tweaking of inductor.

1. Untouched inductor sample
2. Carefully remove plastic pin holder and both windings
3. Wound 9 turns on each core side. For both windings use insulated copper wire with diameter 0.7 mm

Initial parameters: 2x 1.0 mH, 2x 45 mΩ, I_R = 2 A
Final parameters: 2x 0.45 mH, 2x 8 mΩ, $I_R \geq 2$ A

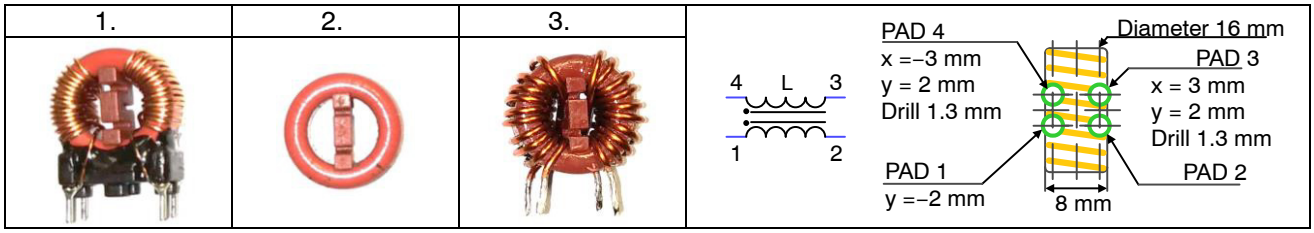


Figure 80. Common Mode Inductor L101 Modification Process

L102 is built from WURTH's 744823333 common mode inductors core. Use formula in Figure 81 and below mentioned steps for desired tweaking of inductor.

1. Untouched inductor sample
2. Carefully remove plastic pin holder and both windings
3. Wound 26 turns on each core side. For both windings use insulated copper wire with diameter 0.7 mm
4. Inductor is covered with Capton tape (KPT−238 – PPC222) to make insulation between windings and shielding
5. Use 19 mm Copper Foil Tape (3M 1181 19MM) to cover top side of the inductor
6. 12.7 mm Copper Foil Tape (3M 1181 12MM)is used to create encircled turn around core between inductor pins
7. Create a closed turn around core circumference with 12.7 mm Copper Foil Tape
8. Solder copper foils together at touching edges
9. Finally, inductor is taped out with 12 mm Insulation Tape (3M 1350 12MM) to make it safe.

Initial parameters: 2x 3.3 mH, 2x 60 mΩ, I_R = 2.5 A
Final parameters: 2x 6.3 mH, 2x 34 mΩ, $I_R \geq 2.5$ A

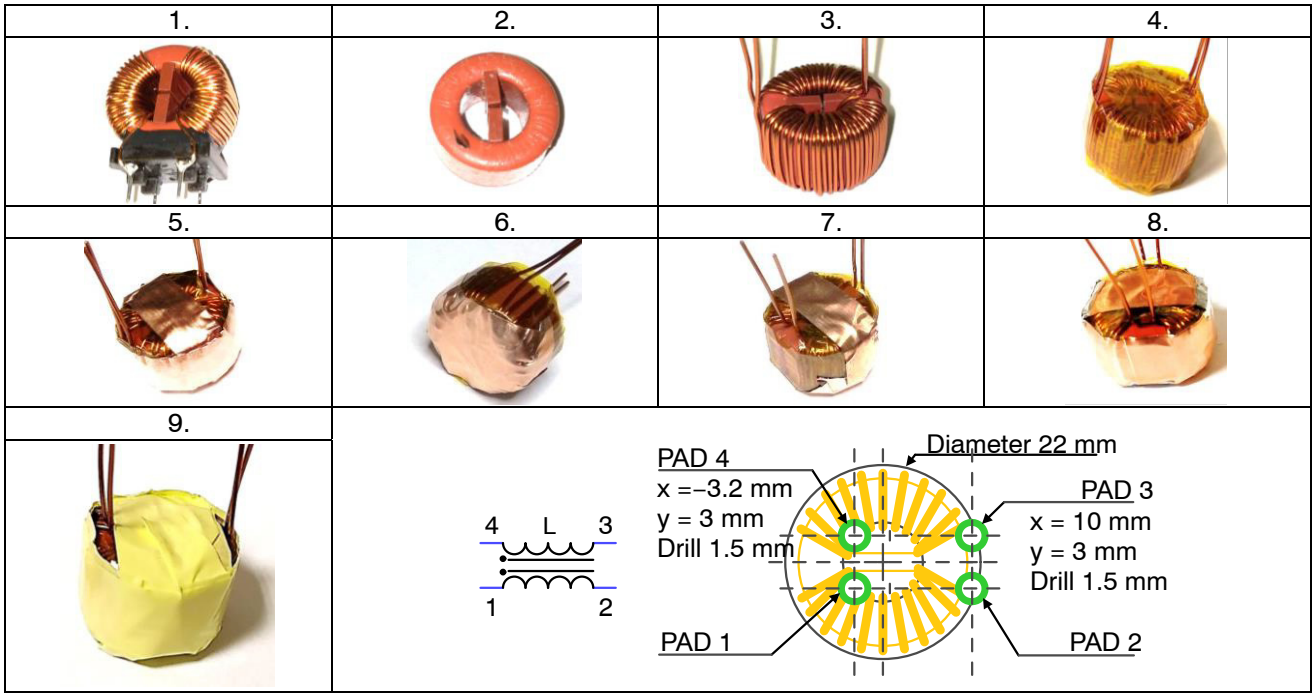


Figure 81. Common Mode Inductor L102 Modification Process

L104 is slightly upgraded differential mode inductor 7447013 manufactured by WURTH. Refer to procedure below in Figure 82 how to change inductor for this demo−board: Initial state of L104 = 90 μH, 40 mΩ, I_R = 4.6 A, WURTH 7447013.

1. Sample initial state
2. Wire terminal shaped in 90 degrees to initial state
3. Outside terminal is insulated with insulation sleeve
4. Inductor is covered with Capton tape (KPT−238 − PPC222) to make insulation between winding and shielding
5. Copper Foil Tape (1181 TAPE (1/4”X18YDS)) is used to create enclosed turn for shielding and short fringing flux
6. Extra pin is added and soldered to shielding turn. This pin is going to be connected to power GND
7. Finally, inductor is covered with Capton tape for safety reason

Initial parameters: 90 μH, 40 mΩ, I_R = 4.6 A.

Final parameters: 90 μH, 40 mΩ, I_R = 4.6 A, shielding with extra pin for grounding was added

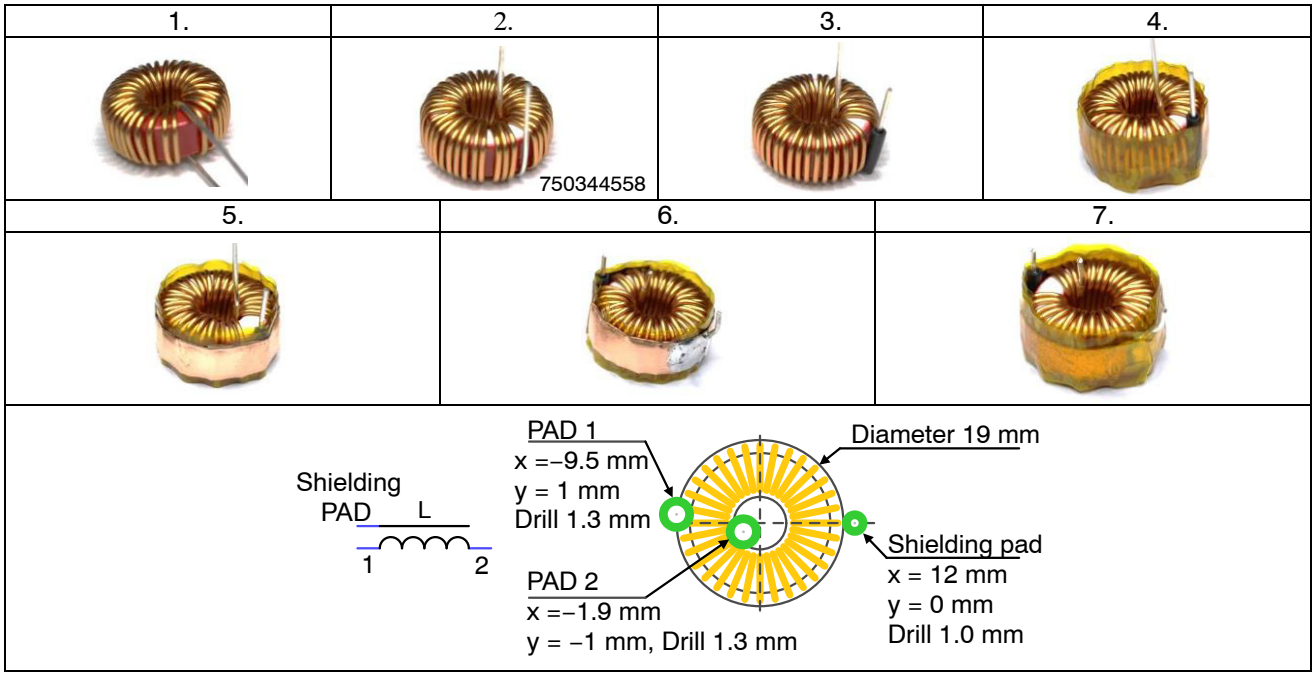


Figure 82. Differential Mode Inductor Shielding Upgrade Steps

Table 4. BILL OF MATERIAL

Parts	Qty	Value	Part Number	Package	Tolerance	Replacement	MANUFACTURER
C101, C102	2	680 nF, 275 V AC	WURTH, 890324025045	C150−100X180	± 10%	Not allowed	WURTH
C103	1	2.2 μF/ 450 V DC	Panasonic, ECW−FD2W225K	C150−072X183	± 10%	Allowed	Panasonic
C104	1	47 pF/ 25V	WURTH, 885012006036	C0603	± 5%	Allowed	WURTH
C105	1	100 μF/ 25V	WURTH, 860020473008	E2,5−7	± 20%	Allowed	WURTH
C106, C107	2	2.2 μF/ 25V	WURTH, 885012207079	C0805	± 20%	Allowed	WURTH
C108	1	1 μF/ 25V	WURTH, 885012206076	C0603	± 20%	Allowed	WURTH
C109	1	100 nF/ 25V	WURTH, 885012206071	C0603	± 20%	Allowed	WURTH
C110, C121	2	10 nF/ 25V	WURTH, 885012206065	C0603	± 10%	Allowed	WURTH
C111	1	NU	–	C0603	–	–	–
C112, C113	2	220 nF/ 25 V	WURTH, 885012206073	C0603	±10%	Allowed	WURTH
C114, C118	2	100 nF/ 450 V	TDK, C3216X7T2W104K160AA	C1206	± 10%	Allowed	TDK
C115	1	2.2 μF/ 16 V	WURTH, 885012106018	C0603	± 10%	Allowed	WURTH
C116, C120	2	NU	–	C1206	–	–	–
C117	1	220 nF/ 50 V	WURTH, 885012206073	C0603	± 10%	Allowed	WURTH
C119	1	1 nF/ 50 V	WURTH, 885012006063	C0603	± 5%	Allowed	WURTH
C122, C124, C126, C128, C130	5	330 μF/ 25 V	WURTH, 870025575009	E5−10,5	± 20%	Allowed	WURTH
C123, C125, C127, C129, C131	5	2.2 μF/ 25V	WURTH, 885012208066	C1206	± 20%	Allowed	WURTH
CY101, CY102	2	1 nF/ 250 V AC	WURTH, 885352211003	C1812	± 10%	Not allowed	WURTH
CY103	1	3.3 nF/ CY	Vishay, WKP332MCPEJ0KR	YC10B5	± 20%	Not allowed	Vishay
D101, D102	2	S1JFL	S1JFL	SOD123	–	Not allowed	ON Semiconductor
D103	1	MM3Z7V5	MM3Z7V5T1G	SOD323	–	Not allowed	ON Semiconductor
D104	1	ES1JFL	ES1JFL	SOD123	–	Not allowed	ON Semiconductor
D105	1	NU	–	SOD323	–	–	–
D106, D109	2	BAS16HT	BAS16HT1G	SOD323	–	Not allowed	ON Semiconductor
D107	1	MM3Z18V	MM3Z18VT1G	SOD323	–	Not allowed	ON Semiconductor
D108	1	S3M	S3M	SMC	–	Not allowed	ON Semiconductor
D110, D112	2	BAT54H	BAT54HT1G	SOD323	–	Not allowed	ON Semiconductor
D111	1	ES3J	ES3J	SMC	–	Not allowed	ON Semiconductor
F101	1	T5A	Littelfuse, 0476005.MR	LF15	–	Allowed	Littelfuse
IC101	1	NCP4306DBAZZAA	NCP4306DBAZZAA	TSOP6	–	Not allowed	ON Semiconductor
IC102	1	FAN3180TSX	FAN3180TSX	SOT23−5	–	Not allowed	ON Semiconductor
IC103	1	NCP1616A	NCP1616A2DR2G	SO10	–	Not allowed	ON Semiconductor
L101	1	MODIFICATED: 744821201	WURTH, 750344558 Sumida, 04291T318	–	± 20%	Not allowed	WURTH / Sumida
L102	1	MODIFICATED: 744823333	WURTH, 750344559 Sumida, 04291T319	–	± 20%	Not allowed	WURTH / Sumida
L103	1	1 μH	WURTH, 74479775210A	L0805	± 20%	Not allowed	WURTH
L104	1	MODIFICATED: 7447013	WURTH, 750344560 Sumida, 04291T320	–	± 20%	Not allowed	WURTH / Sumida
L105	1	180 μH/ T91767	SUMIDA, T91767	–	± 20%	Not allowed	Sumida
Q101, Q108	2	BSS138L	BSS138LT1G	SOT23	–	Not allowed	ON Semiconductor
Q102	1	NU	–	SOT23	–	–	–
Q103	1	NU	–	SOT23	–	–	–
Q104	1	BSS127S−7	Diodes, BSS127S−7	SOT23	–	Not allowed	Diodes

Table 4. BILL OF MATERIAL

Parts	Qty	Value	Part Number	Package	Tolerance	Replacement	MANUFACTURER
Q105, Q106, Q107	3	GS66504B	GaN Systems, GS66504B	GS66504B	–	Not allowed	GaN System
R101	1	VAR 275 V AC, 250 A, 50 pF	Littelfuse, VARV430CH8S	–	–	Allowed	Littelfuse
R102	1	47 kΩ	Various	R0603	± 1%	Allowed	Various
R103, R105, R108	3	330 Ω	Various	R0805	± 1%	Allowed	Various
R104, R110, R113, R139	4	NU	–	R0603	–	–	–
R106	1	10 Ω	Various	R0805	± 1%	Allowed	Various
R107, R112	2	NU	–	R0805	–	–	–
R109	1	6.2 kΩ	Various	R1206	± 1%	Allowed	Various
R111, R141	2	2.2 kΩ	Various	R0603	± 1%	Allowed	Various
R114	1	10 Ω	WURTH, 560050316012	R0603	± 1%	Allowed	WURTH
R115, R123	2	20 kΩ	Various	R0603	± 1%	Allowed	Various
R116	1	1.5 kΩ	Various	R0603	± 1%	Allowed	Various
R117, R120, R124	3	5.1 Ω	Various	R0603	± 1%	Allowed	Various
R118	1	0 Ω	Various	R0603	± 1%	Allowed	Various
R119	1	3.9 kΩ	Various	R1206	± 1%	Allowed	Various
R121, R125, R128	3	0.15 Ω	BB, CRL2512−JW−R150ELF	R6332	± 5%	Allowed	Various
R122	1	470 kΩ	Various	R0603	± 1%	Allowed	Various
R126	1	470 kΩ/ NTC	TDK, B57371V2474J060	R0603	± 5%	Allowed	Various
R127	1	75 kΩ	Various	R0603	± 1%	Allowed	Various
R129	1	150 kΩ	Various	R0603	± 1%	Allowed	Various
R130	1	51 kΩ	Various	R0603	± 1%	Allowed	Various
R131	1	30 kΩ	Various	R0603	± 1%	Allowed	Various
R132, R133, R134, R135	4	1.8 MΩ	Various	R0805	± 1%	Allowed	Various
R136	1	91 kΩ	Various	R0805	± 1%	Allowed	Various
R137	1	24 kΩ	Various	R0603	± 1%	Allowed	Various
R138	1	22 kΩ	Various	R0603	± 1%	Allowed	Various
R140	1	82 kΩ	Various	R0603	± 1%	Allowed	Various
B201,B201, B203, B204	4	800 V / 4 A	Z4DGP408L−HF	Z4−D	–	Not allowed	Compchip
C301, C302, C303, C304	4	22 μF / 400 V	WURTH, 860021375012	E5−10,5x25	± 20%	Allowed	WURTH
C305, C306, C307	3	10 μF / 400 V	WURTH, 860021375011	E5−10,5x13	± 20%	Allowed	WURTH
C401, C402, C404, C405	4	10 nF / 25 V	WURTH, 885012206065	C0603	± 10%	Allowed	WURTH
C403	1	470 pF / 50 V	WURTH, 885012006061	C0603	± 5%	Allowed	WURTH
C406	1	33 pF / 50 V	WURTH, 885012006054	C0603	± 5%	Allowed	WURTH
C407, C414, C415	3	100 nF / 25 V	WURTH, 885012207072	C0805	± 10%	Allowed	WURTH
C408, C416	1	1 μF / 25 V	WURTH, 885012207078	C0805	± 10%	Allowed	WURTH
C409	1	100 μF / 25 V	WURTH, 860020473008	E2,5−7	± 20%	Allowed	WURTH
C410	1	1 nF / 50 V	WURTH, 885012006063	C0603	± 5%	Allowed	WURTH
C411	1	470 nF / 25 V	WURTH, 885012208062	C1206	± 10%	Allowed	WURTH
C412	1	1 nF / 50 V	WURTH, 885012006063	C0603	± 5%	Allowed	WURTH
C413	1	12 nF / 50 V	various	C0603	± 5%	Allowed	Various
C417	1	220 nF / 25 V	WURTH, 885012206073	C0603	± 20%	Allowed	WURTH

Table 4. BILL OF MATERIAL

Parts	Qty	Value	Part Number	Package	Tolerance	Replacement	MANUFACTURER
C418	1	47 μF/ 50 V	WURTH, 860020673013	E2,5−7	± 5%	Allowed	WURTH
C419, C420, C421	3	100 nF/ 450V	TDK, C3216X7T2W104K160AA	C1206	± 10%	Allowed	TDK
C422, C423, C424, C425	4	2.7 nF / 630 V C0G	TDK, CGA5L4C0G2J272J160AA	C1206	± 5%	Not allowed	TDK
C426, C427	2	100 pF / 1 kV C0G	Murata, GRM31A5C3A101JW01D	C1206	± 5%	Not allowed	Murata
C428, C429, C431	3	NU	–	C0603	± 10%	–	–
C430	1	2.2 nF / 50 V	WURTH, 885012206085	C0603	± 10%	Allowed	WURTH
D401	1	S1JFL	S1JFL	SOD123	–	Not allowed	ON Semiconductor
D402, D403	2	BZX84C2V4LT1G	BZX84C2V4LT1G	SOT23	–	Not allowed	ON Semiconductor
D404, D407, D408	3	ES1JFL	ES1JFL	SOD123	–	Not allowed	ON Semiconductor
D405	1	BAT54HT1G	BAT54HT1G	SOD323	–	Not allowed	ON Semiconductor
D406	1	MM3Z18VT1G	MM3Z18VT1G	SOD323	–	Not allowed	ON Semiconductor
D409, D410, D411, D412	4	MBR2H100SFT3G	MBR2H100SFT3G	SOD123	–	Not allowed	ON Semiconductor
D413, D414	2	MURA160	MURA160T3G	SMA2	–	Not allowed	ON Semiconductor
IC401	1	NCP13992	NCP13992	SO16	–	Not allowed	ON Semiconductor
IC402	1	NCP51820	NCP51820A	DFN	–	Not allowed	ON Semiconductor
IC403	1	NCP431BCSNT1G	NCP431BCSNT1G	SOT23	–	Not allowed	ON Semiconductor
L401, L402, L403	3	1 μH	WURTH, 74479775210A	L0805	± 20%	Not allowed	WURTH
L404	1	8 μH	Sumida, T91760	RM510	–	Not allowed	Sumida
Q401, Q402, Q403	3	BSS138LT1G	BSS138LT1G	SOT23	–	Not allowed	ON Semiconductor
Q404, Q405	2	GS66504B	GaN Systems, GS66504B	GS66504B	–	Not allowed	GaN System
R401	1	20 kΩ	various	R0603	± 1%	Allowed	Various
R402	1	4.3 kΩ	various	R0603	± 1%	Allowed	Various
R403	1	15 kΩ	various	R0603	± 1%	Allowed	Various
R404	1	10 kΩ	various	R0603	± 1%	Allowed	Various
R405, R406	2	1.2 kΩ	various	R1206	± 1%	Allowed	Various
R408	1	100 Ω	various	R0805	± 5%	Allowed	Various
R409, R433	2	11 k	various	R0603	± 1%	Allowed	Various
R410, R427, R428, R431	4	NU	–	R0603	± 1%	–	–
R413	1	2.2 kΩ	various	R0603	± 1%	Allowed	Various
R414	1	1 kΩ	various	R0603	± 1%	Allowed	Various
R415	1	110 kΩ	various	R0603	± 1%	Allowed	Various
R416	1	10 Ω	various	R0805	± 5%	Allowed	Various
R418, R420	2	33 Ω	various	R0603	± 1%	Allowed	Various
R419, R421	2	2.2 Ω	various	R0603	± 5%	Allowed	Various
R422	1	22 kΩ	various	R0603	± 1%	Allowed	Various
R423	1	2.2 Ω	various	R1206	± 5%	Allowed	Various
R424	1	1 Ω	various	R1206	± 5%	Allowed	Various
R425	1	820 Ω	various	R0603	± 1%	Allowed	Various
R430, R434	2	68 kΩ	various	R0603	± 1%	Allowed	Various
R432	1	47 kΩ	various	R0603	± 1%	Allowed	Various
R435	1	150 kΩ	various	R0603	± 1%	Allowed	Various

Table 4. BILL OF MATERIAL

Parts	Qty	Value	Part Number	Package	Tolerance	Replacement	MANUFACTURER
RT101	1	NU	NOTE: Recommended – NTC 470k, B57371V2474J060	R0603	–	–	–
U401	1	TCLT1008	Vishay, TCLT1008	SOP−4	–	Not allowed	Vishay
C501, C502	2	470 pF / 100 V	WURTH, 885012006083	C0603	± 5%	Allowed	WURTH
C503, C504, C507, C508	4	4.7 uF / 25 V	WURTH, 885012107018	C0805	± 20%	Allowed	WURTH
C505, C506	2	2.2 μF / 25 V	various	C0603	± 20%	Allowed	Various
C509, C510	2	1 nF / 25 V	WURTH, 885012006044	C0603	± 5%	Allowed	WURTH
D501	1	NU	–	SOD323	–	–	–
IC501, IC502	2	NCP4306	NCP4306ABAZZZA	DFN−8	–	Not allowed	ON Semiconductor
Q501	1	NU	–	SOIC8/ SO8FL	–	–	–
Q502, Q503, Q504, Q505	4	NTMFS5C645	NTMFS5C645NLT1G	SO8FL	–	Not allowed	ON Semiconductor
R501, R502, R503, R505	4	16 Ω	various	R0805	± 1%	Allowed	Various
R504	1	NU	various	R0603	–	–	–
R506	1	0 Ω	various	R0603	± 1%	Allowed	Various
R507, R514	2	27 kΩ	various	R0603	± 1%	Allowed	Various
R508, R513	2	1.1 kΩ	various	R0603	± 1%	Allowed	Various
R509, R512	2	6.8 kΩ	various	R0603	± 1%	Allowed	Various
R510, R511	2	5.1 Ω	various	R0603	± 5%	Allowed	Various
X501	1	N = 10:1:1:1:1	SUMIDA, T91706	–	–	Not allowed	Sumida

NOTES: All parts are Pb−free.

LITERATURE

High Performance Current Mode Resonant Controller with Integrated High Voltage Drivers:
NCP13992: http://www.onsemi.com/PowerSolutions/product.do?id=NCP13992

Power Factor Controller, High Voltage Active X2:
NCP1616: http://www.onsemi.com/PowerSolutions/product.do?id=NCP1616

Secondary Side Synchronous Rectifier Controllers:
NCP4306: http://www.onsemi.com/PowerSolutions/product.do?id=NCP4306

Voltage Reference, Programmable Shunt Regulator
NCP431: http://www.onsemi.com/PowerSolutions/product.do?id=NCP431

High Performance, 650 V Half Bridge Gate Driver for GaN Power Switches
NCP51820: http://www.onsemi.com/PowerSolutions/product.do?id=NCP51820

NCP51820 GaN Driver, PCB Design and Layout Application Note
https://www.onsemi.com/pub/Collateral/AND9932−D.PDF

High−speed low−side gate driver with a 3.3 V output LDO
FAN3180: http://www.onsemi.com/PowerSolutions/product.do?id=FAN3180

Single N−Channel Power MOSFET 60 V, 100 A, 4.0 mΩ
NTMFS5C645NLT1G: http://www.onsemi.com/PowerSolutions/product.do?id= NTMFS5C645NLT1G

GaN Systems 650V Enhancement Mode GaN Transistor
GS66504B https://gansystems.com/wp−content/uploads/2019/07/GS66504B−DS−Rev−190717.pdf

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Additional information

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