EVBUM2694/D

QHS860-DC4-GEVK Evaluation Board User's Manual

Introduction

QHS860−DC4−GEVK is the single RGMII hardware reference module for Quantenna® QT3840BC chipset. This module can be integrated with different Residential GW SoCs to provide up to 1.7 Gbps PHY/Data Link Speed in 80 MHz mode. It consists of one 11ac digital baseband chip, one 4 chain 5 GHz RFIC with Skyworks SKY85717 FEM and one 2 chain 2.4 GHz Realtek RTL8192FR module.

Description

The QT3840BC chipset supports the 802.11ac/n/a standards. QHS860−DC4−GEVK has one RGMII port, which supports 1 Gbps/100 Mbps/10 Mbps. QHS860−DC4−GEVK supports 4x4 5 GHz and 2x2 2.4 GHz MU−MIMO.

I/O Interfaces and Features

- Explicit and Implicit Digital Transmit Beamforming
- Advanced MIMO Features STBC and Channel State Aware Link Management for Sustained Link Robustness
- Two ARC−based Network Processors with Hardware Assist to Manage Multiple Simultaneous
- 802.11a/n/ac Connections
- DSP Engine to Hardware Accelerate Aggregation, De−aggregation, and Packet Re−ordering
- MU−MIMO Support
- SuperDFS Support
- Expanded Support for 128 Users
- LDPC Support
- Works with Quantenna 4x4 5 GHz RFIC (QT2518B)
- DDR2/DDR3 Memory Support
- PCIe Gen2.0 with Embedded DMA
- Standards:
  - ◆ 802.11ac/n/a
  - ◆ 802.11i (WEP, WPA/WPA2, RADIUS)
  - ◆ 802.11d
  - ◆ 802.11e (WMM, WMM−PS)
  - ◆ 802.11w
  - ◆ 802.11h
  - ◆ 802.11k
- Operating Frequencies: 4.9−5.85 GHz/2.4 GHz
- Maximum Data Rate (per Stream) − Rates are for 256 QAM Operation
  - ◆ 80 MHz: 1.7 Gbps (433.33 Mbps)
  - ◆ 40 MHz: 800 Mbps (200 Mbps)
  - ◆ 20 MHz: 346.8 Mbps (86.7 Mbps)
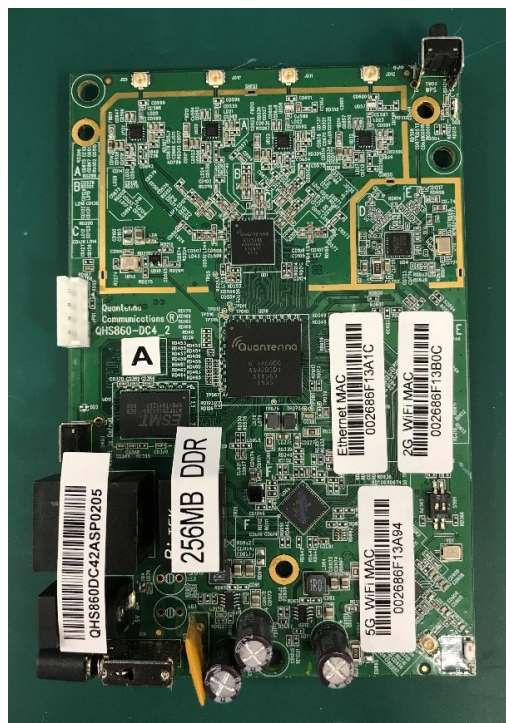
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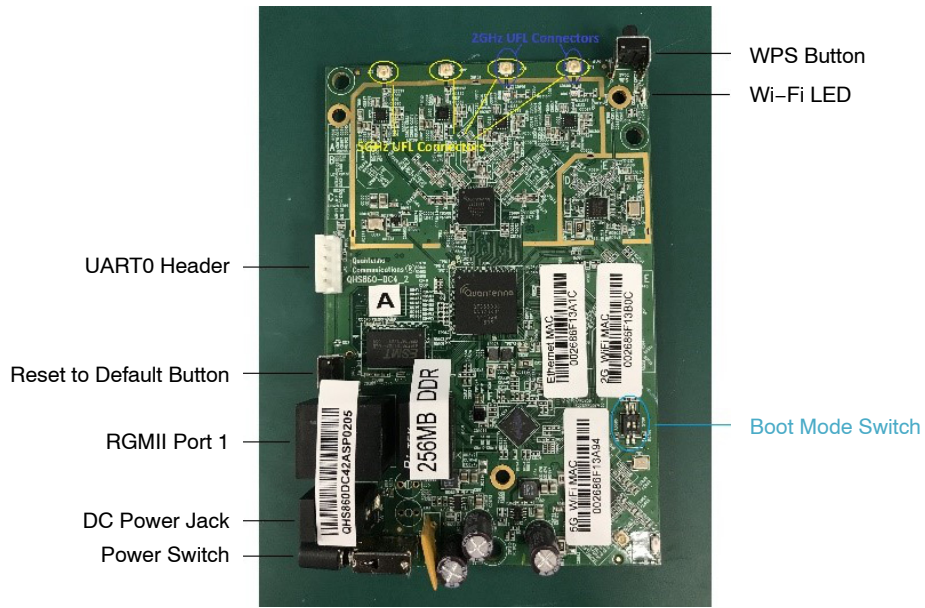**Figure 1. QHS860−DC4−GEVK Photo**

Figure 2. QHS860−DC4−GEVK Description

APPLICATIONS INFORMATION

Power Configuration

QHS860−DC4−GEVK is designed to be powered externally. The external power supply should be 5 V DC. When the board is powered on, the power LED will be steady green.

Reset to Default Button

Reserved (Reset to Default Button).

WPS Button

Reserved (WPS Button).

RGMII Port

RGMII supports 1 Gbps/100 Mbps/10 Mbps UTP speed.

UART Header

The UART header is used to connect serial port for debug purpose.

Table 1. SERIAL PORT SETTING

Baud Rate	115200
Data	8 bit
Parity	None
Stop	1 bit
Flow Control	None

Boot Mode Switch

Boot mode switch controls serial port mode.

Table 2. BOOT MODE SWITCH DEFINITION

State	Definition
00	bootm
10	SPI−0 (Default)
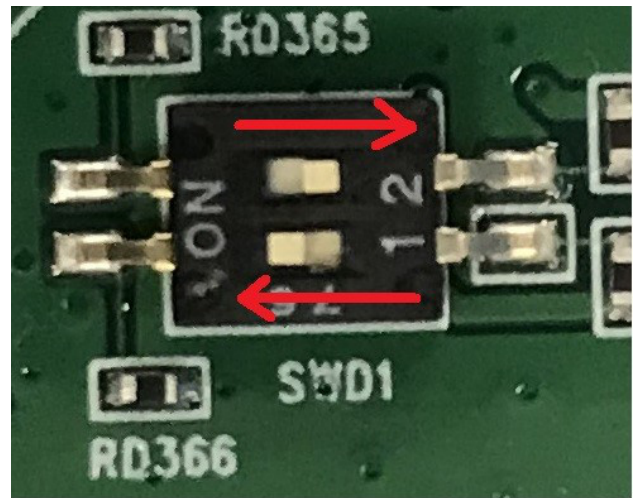
Figure 3. Default Setting (SPI−0)
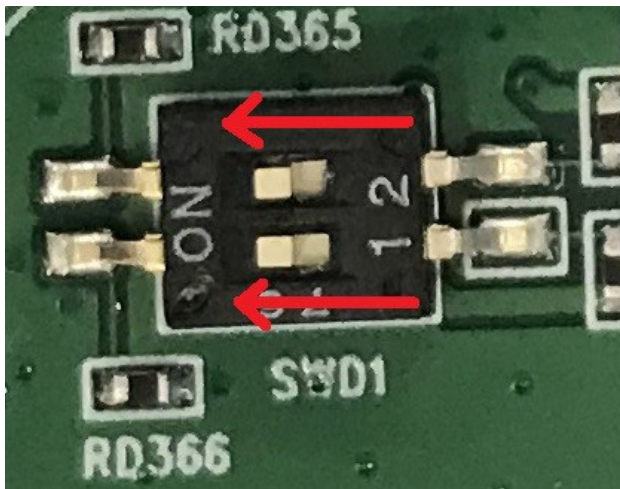
Figure 4. Bootm Setting

BOARD POWER UP

LED Indication When QHS860−DC4−GEVK Powers Up
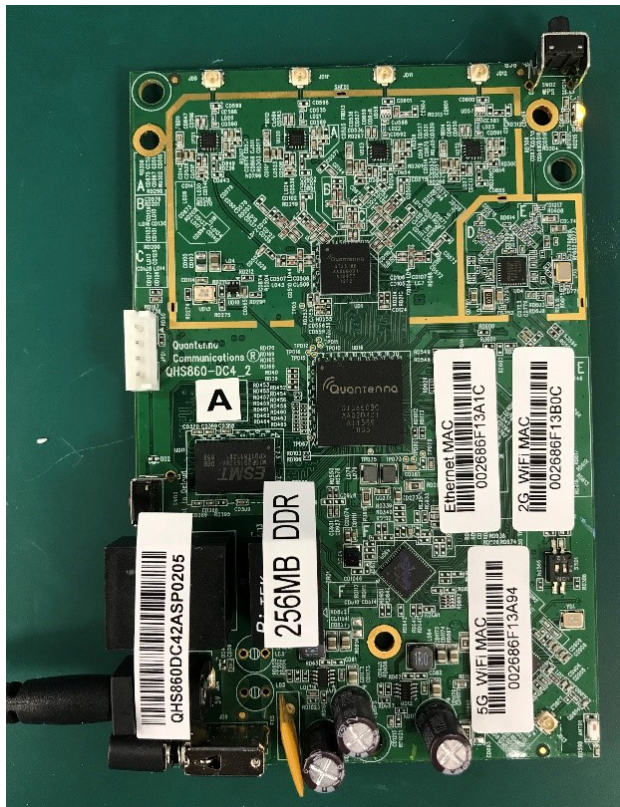
Figure 5. LED Indication When QHS860−DC4−GEVK Powers Up

Console Display When QHS860−DC4−GEVK Successfully Boots Up

When QHS860−DC4−GEVK successfully boots up, it will show "quantenna #".

Figure 6. QHS860−DC4−GEVK Successfully Boots Up

Web GUI

QHS860−DC4−GEVK default IP address is 192.168.1.200.

Figure 7. Default IP Address
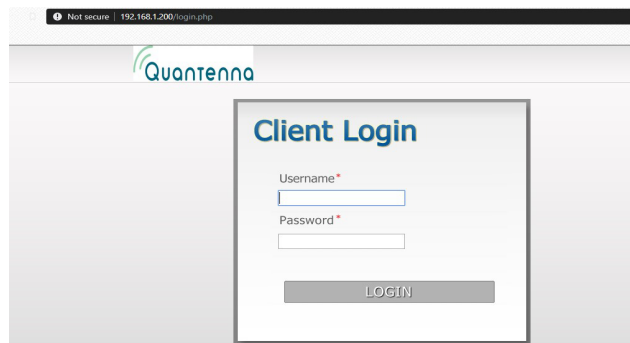
Web GUI   username: super
                    password: super

Figure 8. Web GUI Username and Password

Telnet

QHS860−DC4−GEVK could also be accessed through telnet. Use board IP address and the login username is "root".
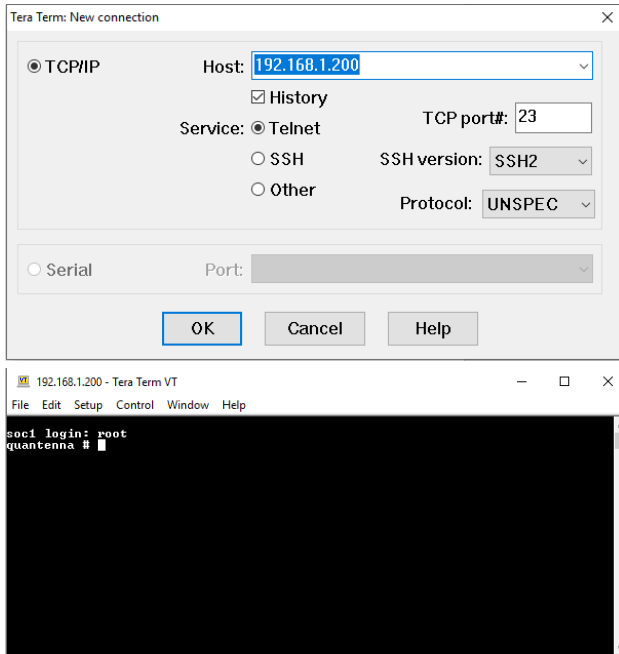
Figure 9. Access Through Telnet

ADDITIONAL INFORMATION

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Technical Library: www.onsemi.com/design/resources/technical–documentation
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ONLINE SUPPORT: www.onsemi.com/support
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