# VCSEL Driver with Buck PWM Controller Evaluation Board User's Manual

## NCL30105G1EVB

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

### Overview

This manual covers the specification, theory of operation, testing and construction of the NCL30105G1EVB evaluation board. This evaluation board uses NCL30105 as a high pulse current low duty cycle VCSEL driver. The expected duty cycle is less than 5% in typical applications. The NCL30105 is an inverted buck converter design with constant off time control.

### Features

The key features of this evaluation board include:

- High Peak Current
- Small Size
- Fast Rise/Fall Time
- PWM Control

### SPECIFICATIONS

| | | |
|---|---|---|
| Input voltage | 8.8 V dc – 22 V dc | Nom. |
| Output Voltage | 3 V dc | Nom. |
| Output Current | 4 A | Peak |
| Output Ripple | ± 6.5% | |
| Output Rise/Fall Time | 8 μs / 36 μs | |
| Switching Frequency | 146 kHz | @12 V |
| Dimming Interface | PWM | SMA connector |
| PCB Size | 25 mm × 55 mm | |

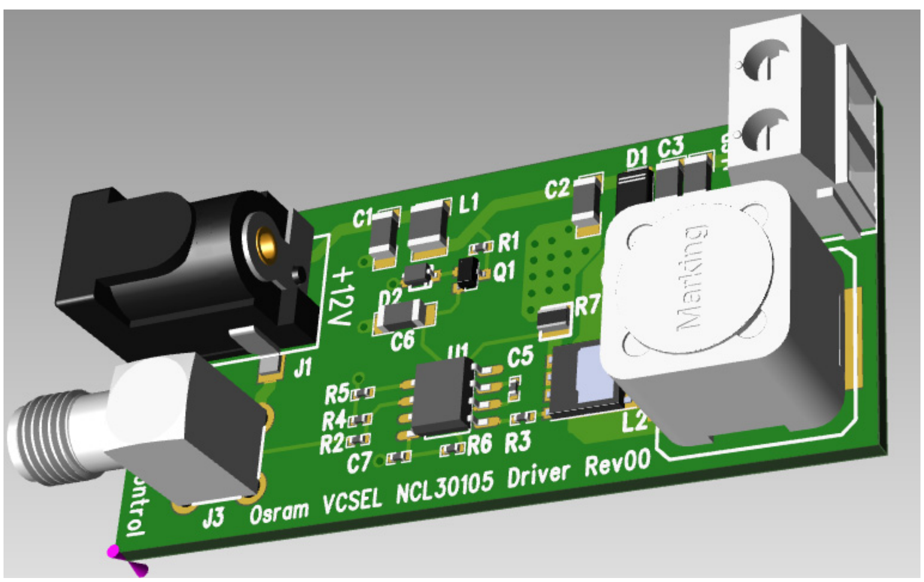


**Figure 1. Evaluation Board**

## THEORY OF OPERATION

### Overview

The NCL30105G1EVB drives a low voltage high current VCSEL for camera illumination for the automotive market.

### Current Control

The NCL30105 is a peak current mode control with constant off time. Peak current control provides accurate current regulation. The value of R7 sets the peak current as follows:

$$I_{peak} = \frac{1.01\ V}{R7}$$

The soft start pin controls the peak current at turn on. A capacitor on this pin is charged up by a 20 μA internal current source. For PWM operation this capacitor is very small to allow for fast rise times. Analog dimming can be done by programming the voltage on the soft start pin. The connection for this option is not brought out on this demo board although this control method is still available.

The off time is held constant in operation. R5 programs the off time. Constant off time control eliminates sub harmonic oscillation in buck converters where the duty cycle exceeds 50%. The on time is determined by the input voltage, the output voltage, and the inductor value. Consequently, the switching frequency will vary over line and load conditions even though the off time is constant. The NCL30105 has a maximum on time ~34 μs which is set internally.

### Vcc

Q1 is an emitter follower that limits Vcc to ~14 V. The NCL30105 has an upper Vcc limit of 22 V. Some automotive applications exceed the 22 V limit especially in the case of load dump.

### Current Sense

The current sense pin has a Leading Edge Blanking (LEB) function to avoid false triggering of the current sense comparator. The LEB is ~500 ns.

### Dimming

The demo board is set up for PWM dimming through J3 (SMA). A 0−5 V square wave signal will provide PWM dimming. The absence of a signal to J3, the output defaults to off.

The output current (green trace) follows the PWM input signal (yellow trace). The output filter affects the rise and fall times.

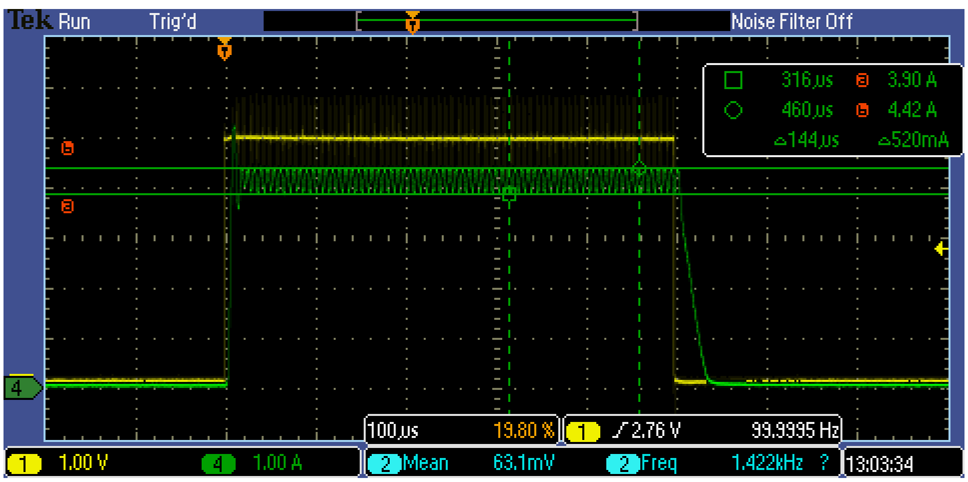


**Figure 2. Dimming Signal vs. $I_{OUT}$**

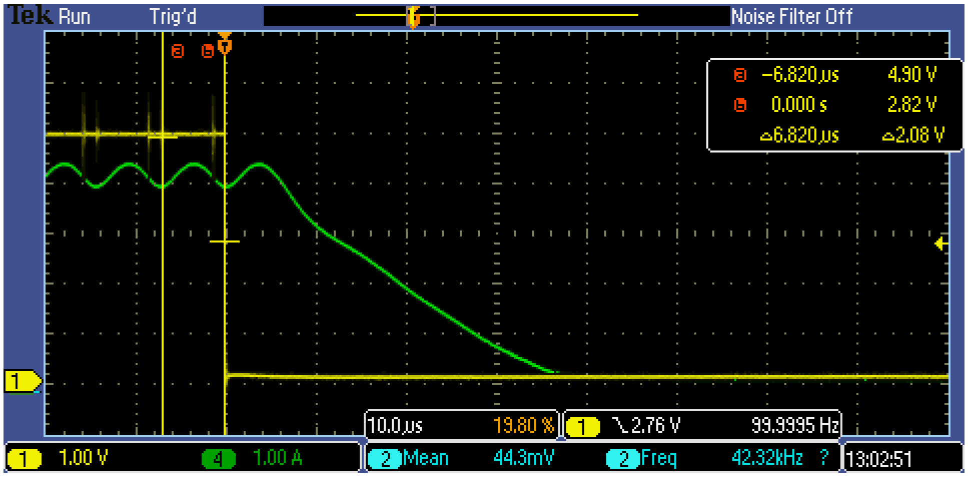


**Figure 3. Fall Time vs. Input Signal**

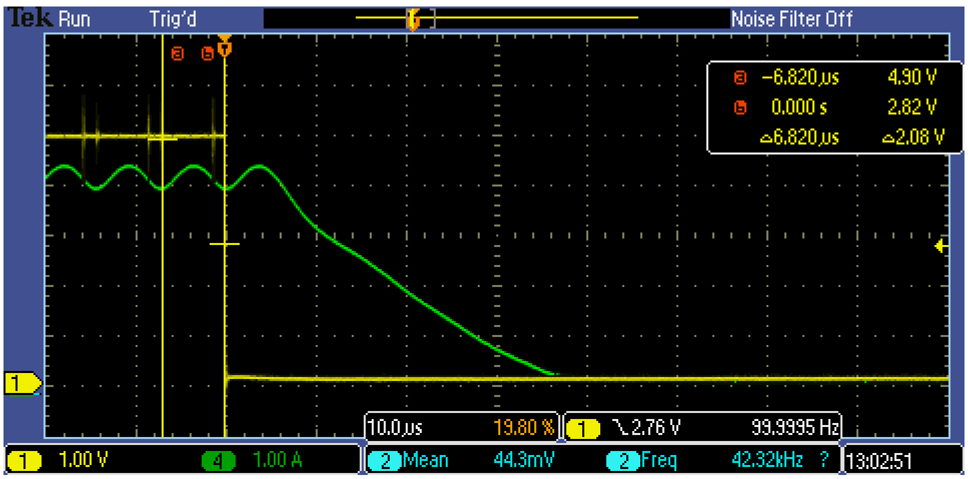


**Figure 4. Rise Time vs. Input Signal**

The rise and fall times are affected by the output filter values. Raising the Fsw will reduce the size requirement for the output capacitor which reduces rise and fall times. Reducing the off time will increase the switching frequency and reduce current ripple for a given output inductor.

## SCHEMATIC

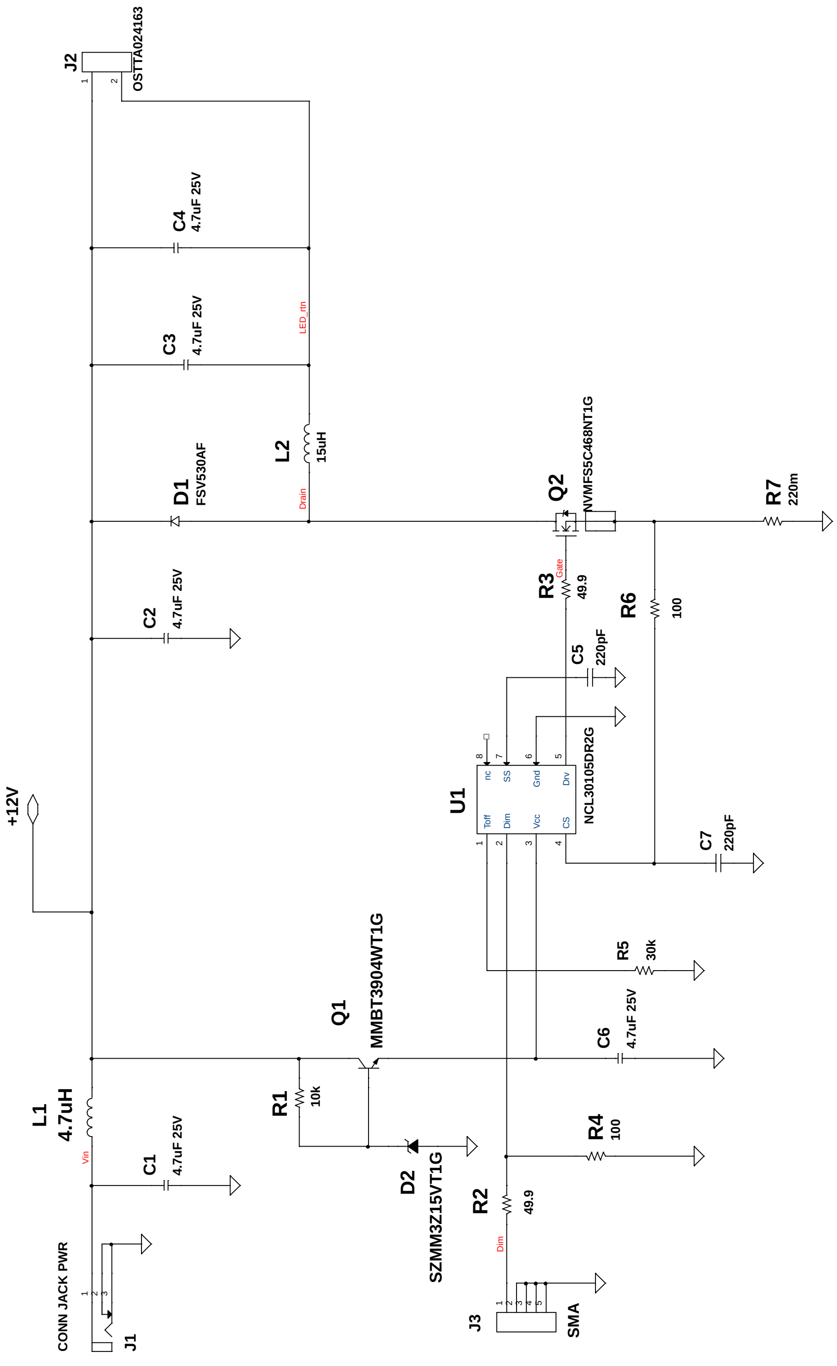


Figure 5. Schematic

## BILL OF MATERIAL

### BILL OF MATERIAL

| Qty | Reference | Part | Distributor | Dist. P/N | Manufacturer | Mfr_PN | Insert | Safety Controlled |
|---|---|---|---|---|---|---|---|---|
| 5 | C1, C2, C3, C4, C6 | 4.7 μF 25 V | Digikey | 1276−3178−1−ND | Samsung | CL31B475KAHN NWE | Yes | No |
| 2 | C5, C7 | 220 pF | Digikey | 311−1416−1−ND | Yageo | CC0402JRNPO9 BN221 | Yes | No |
| 1 | D1 | FSV530AF | ON Semiconductor | FSV530AFCT−ND | ON Semiconductor | FSV530AF | Yes | No |
| 1 | D2 | SZMM3Z15V T1G | ON Semiconductor | SZMM3Z15VT1GOS CT−ND | ON Semiconductor | SZMM3Z15VT1G | Yes | No |
| 1 | J1 | CONN JACK PWR | Digikey | 732−5929−1−ND | Wurth | 694106106102 | Yes | No |
| 1 | J2 | OSTTA024163 | Digikey | ED2580−ND | On Shore | OSTTA024163 | Yes | No |
| 1 | J3 | SMA | Digikey | WM5525−ND | Molex | 731000114 | Yes | No |
| 1 | L1 | 4.7 μH | Digikey | 587−1624−1−ND | Taiyo Yuden | CBC3225T4R7MR | Yes | No |
| 1 | L2 | 15 μH | Digikey | 732−1242−1−ND | Wurth | 7447709150 | Yes | No |
| 1 | Q1 | MMBT3904W T1G | ON Semiconductor | MMBT3904WT1G | ON Semiconductor | MMBT3904WT1G | Yes | No |
| 1 | Q2 | NVMFS5C46 8NT1G | ON Semiconductor | NVMFS5C468NT1G OSCT−ND | ON Semiconductor | NVMFS5C468NT 1G | Yes | No |
| 1 | R1 | 10k | Digikey | 311−10.0KLRCT−ND | Yaego | RC0402FR−0710 KL | Yes | No |
| 2 | R2, R3 | 49.9 | Digikey | 311−49.9LRCT−ND | Yaego | RC0402FR−0749 R9L | Yes | No |
| 2 | R4, R6 | 100 | Digikey | 311−100LRCT−ND | Yaego | RC0402FR−0710 0RL | Yes | No |
| 1 | R5 | 30k | Digikey | 311−30.0KLRCT−ND | Yaego | RC0402FR−0730 KL | Yes | No |
| 1 | R7 | 220m | Digikey | 408−1608−1−ND | Susumu | KRL2012E−M−R2 20−F−T5 | Yes | No |
| 1 | U1 | NCL30105DR 2G | ON Semiconductor | NCL30105DR2GOS CT−ND | ON Semiconductor | NCL30105DR2G | Yes | No |

## TEST PROCEDURE

1. Require Equipment
   a. DC Power Supply 12 V @ 2 A
   b. Function Generator
   c. LED Load similar to Luminus CBT−90−B−L11−J101 (observe the correct polarity)
2. Connector the LED Load to J2
3. Apply 12 V to J1 (2.1 x 5.5 Power Connector)
4. Connect a function generator and set as follows:
   a. Frequency – 100 Hz
   b. Duty Cycle – 5%
   c. Vin – 0−5 V (into a 50 Ω load)
5. Observe that the output current transitions from 0 to ~4 A in sync with the function generator output.

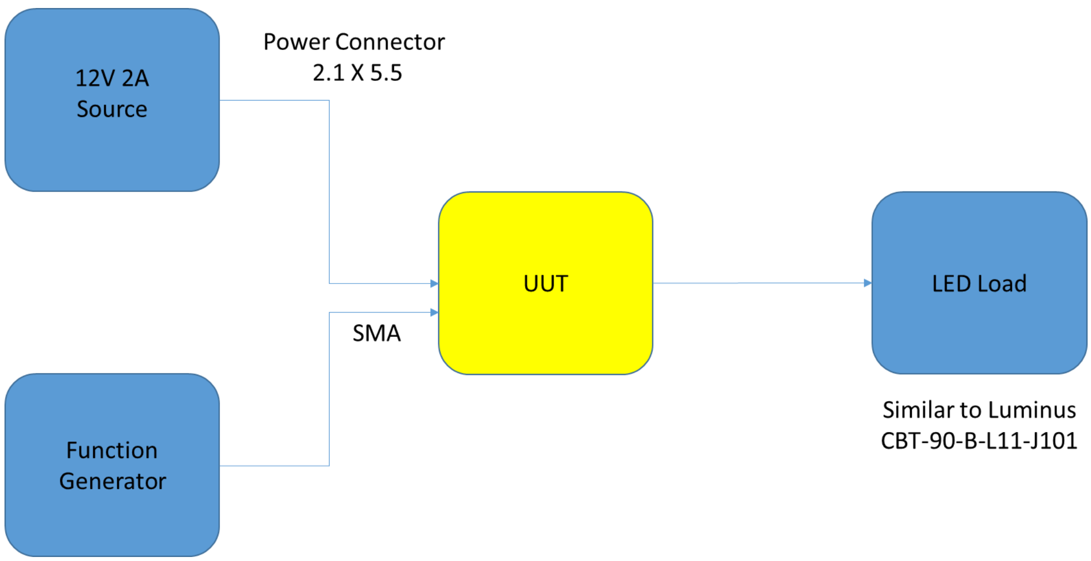


**Figure 6. Test Setup**

## ADDITIONAL INFORMATION

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**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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