

Combo JFET SSCB Evaluation Board User's Manual

EVBUM2926/D

General Information

This document provides descriptions and instructions for the onsemi Solid State Circuit Breaker (SSCB) application with Silicon Carbide (SiC) Combo JFET device in TOLL package. Included is schematics, PCB layout, interface definition, test procedure and bill of material.

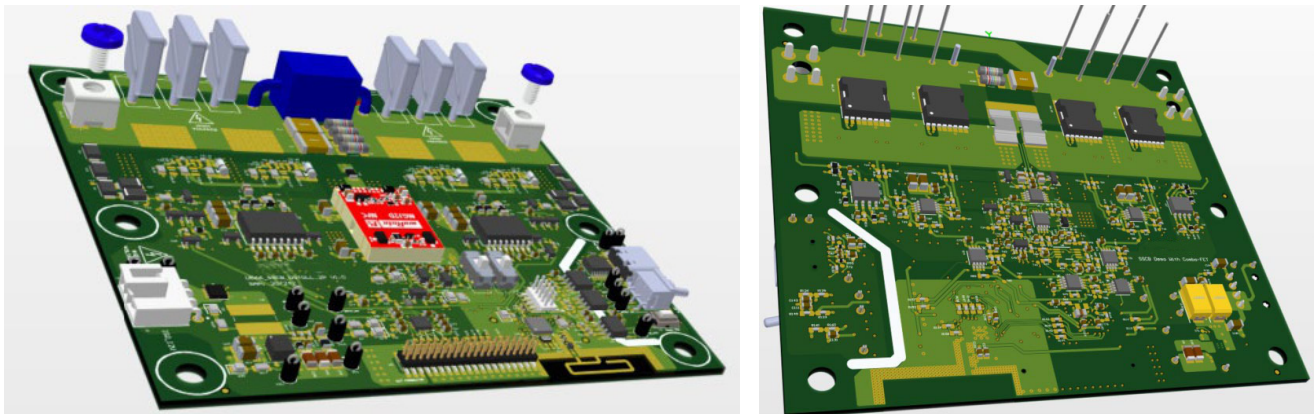


Figure 1. Picture of the Evaluation Board Design

Referenced Documents

The reference documents below take precedence over the contents of this user's manual and should always be consulted for the latest information.

- [1] Website page: UG4SC075005L8S
- [2] Combo JFET Technical Overview: AND90336/D
- [3] JFET Primer: AND90329/D
- [4] JFET User Guide: UM70113/D

Introduction

SiC Combo JFETs are composite devices consisting of a low-voltage Si MOSFET and a high-voltage SiC normally on JFET. Figure 2 shows the circuit schematic of the Combo JFET. The source of SiC JFET connects with drain of low voltage silicon MOSFET, both gates of SiC JFET and silicone MOSFET are accessible. Compared with standard cascode structure, the SiC Combo JFET has advantages of lower $R_{DS(on)}$ by over-drive, full switching speed control and junction temperature sensing, thanks to the accessibility of the gate of JFET. At the same time, with simple external configuration, the Combo JFET has normally off feature same as the standard cascode.

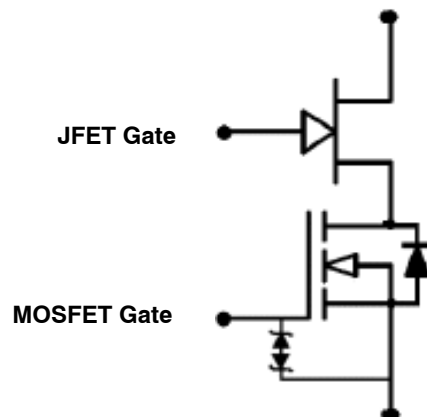


Figure 2. Circuit Schematic of the Combo JFET

The evaluation board demonstrates the design of solid state circuit breaker with onsemi Combo JFET device UG4SC075005L8S and Qorvo smart communication controller QPG6105.

EVBUM2926/D



Figure 3. UG4SC075005L8S, not scaled

Functional Blocks

There are seven functional blocks on this evaluation board:

- Power channel: includes power cells, snubbers and gate drivers
- Current sensing: current sensing conditioning and over current protection
- JFET junction temperature sensing: measure the JFET gate to source voltage drop
- Vds sensing: measure the drain to source voltage drop of power FET
- ADC: analog to digital conversion
- MCU: micro-computer unit and interfaces
- Auxiliary power supply: auxiliary power input and control power converter

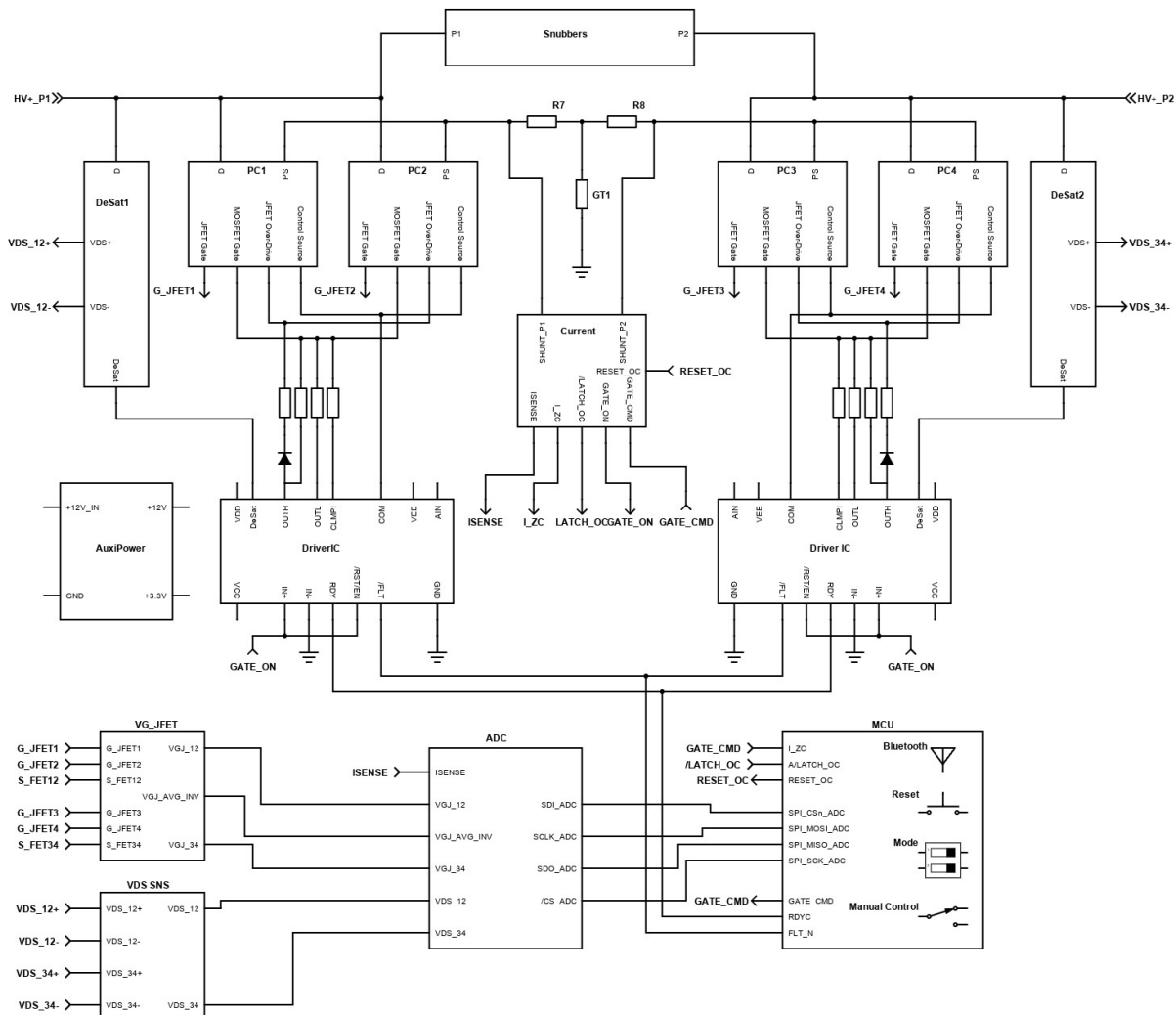


Figure 4. Evaluation Board Functional Diagram

Power Channel

The power stage of this solid-state circuit breaker evaluation board is bidirectional blocking and constructed by the Combo JFET with two in parallel and common source series configuration. Two shunt resistors are inserted into

common source for current sensing. RC snubber, TVS and MOVs are for absorbing the energy stored in parasitic inductors to clamp the voltage during Combo JFET switching off.

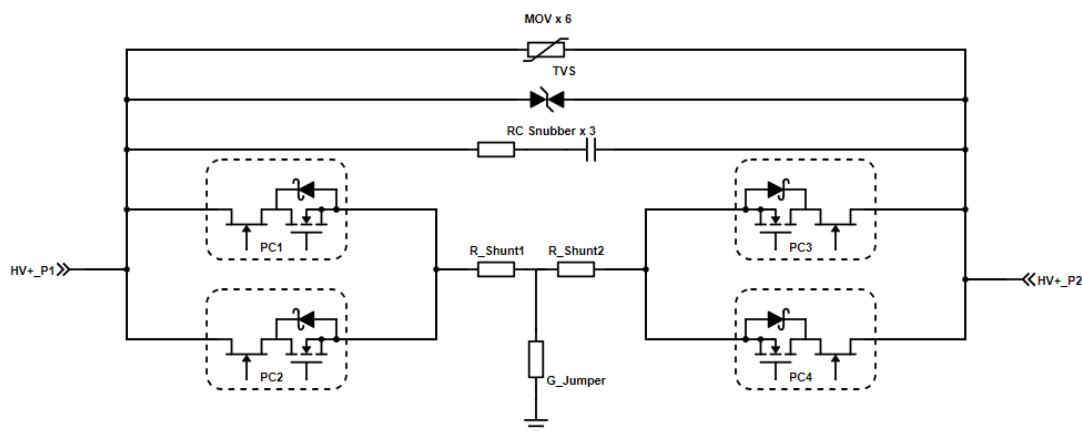


Figure 5. Power Channel Diagram

There are four identical power cells (PC1–PC4), the gate circuit configuration for each power cell is shown below. R1 and R2 are pull down resistors for the MOSFET and JFET respectively. R3 is JFET gate resistor to tune the switching

speed. D1 is to block the over-drive voltage of JFET gate, R4 and R6 are the gate and control source resistors to isolate the loop current between two Combo JFETs in parallel.

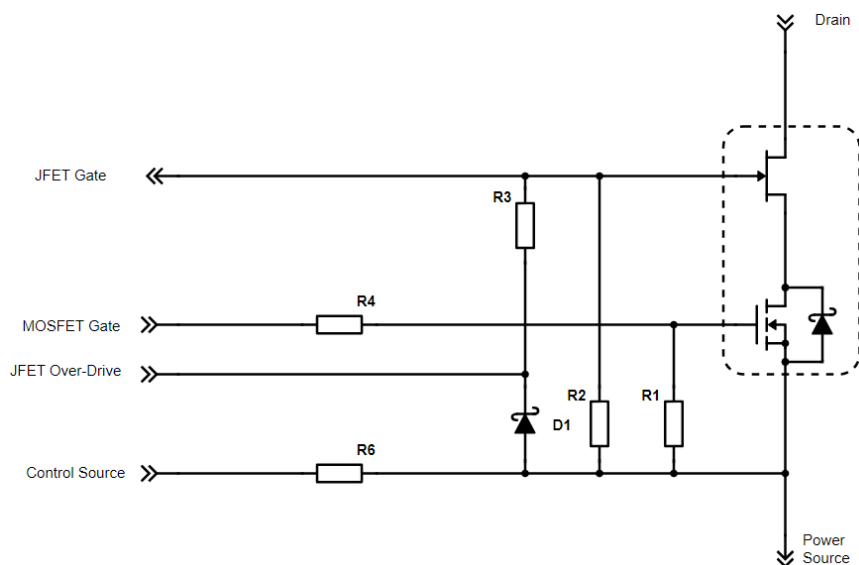


Figure 6. Power Cell Diagram

Current Sensing

The current is measured by shunt resistors and analog conditioning circuits, the hardware over current threshold

can be changed by resistor value and over current state is latched until it is reset manually or by software through GUI.

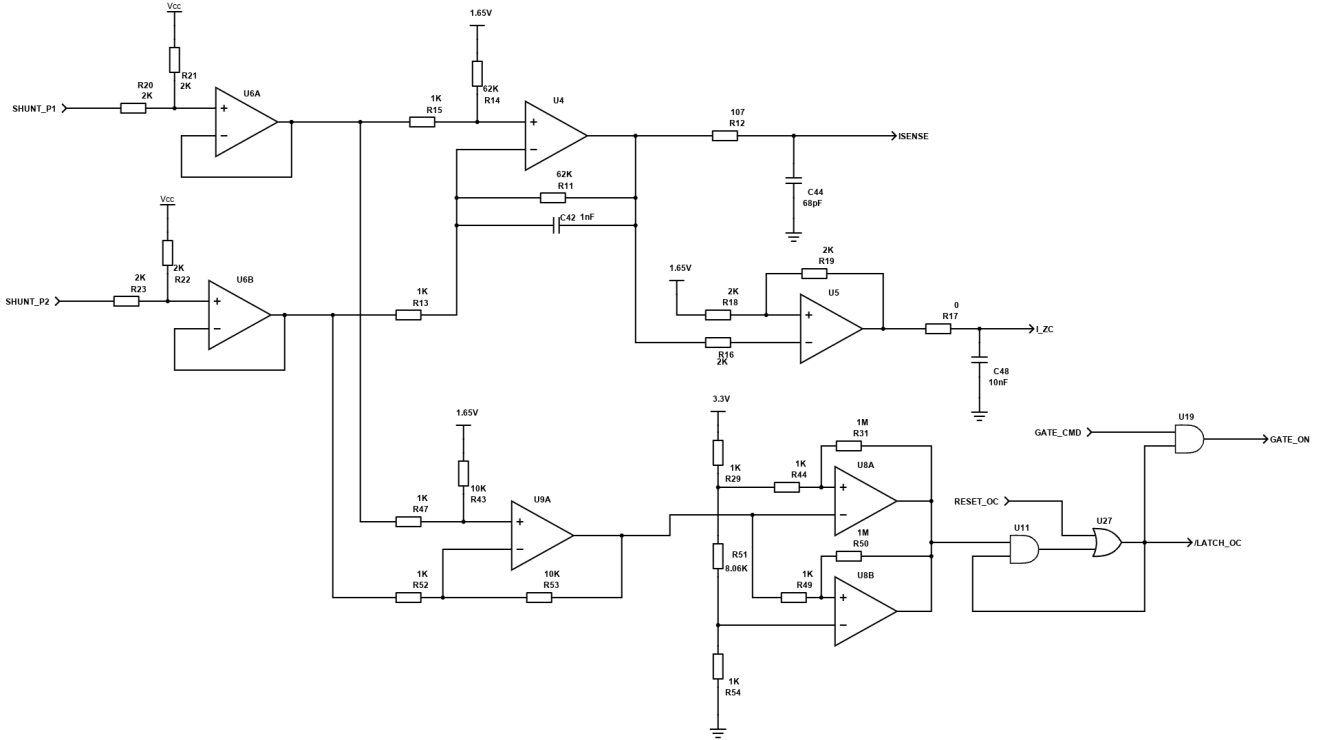
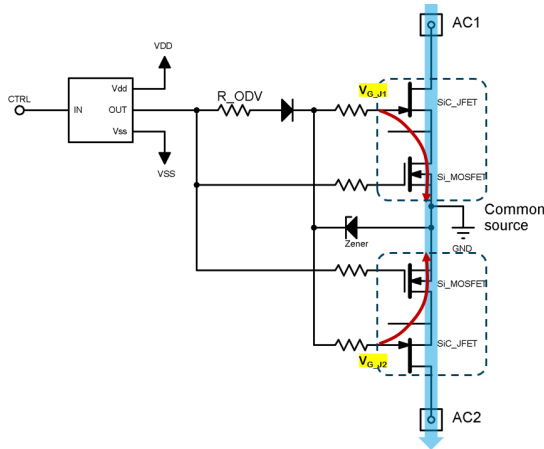


Figure 7. Current Sensing and Over Current Protection

JFET Junction Temperature Sensing

The JFET junction temperature is detected by measuring of JFET gate to source voltage. For Combo JFET, there is no access to the source of JFET, so the measurement of JFET

gate voltage includes drain to source voltage drop of low voltage MOSFET cascoded with JFET. To get rid of voltage offset of low voltage MOSFET drain to source, a hardware sum circuit be developed.



$$V_{G_J1} = V_{GS_J1} + V_{DS_MOSFET1}$$

$$V_{G_J2} = V_{GS_J2} + V_{DS_MOSFET2}$$

$$\frac{V_{G_J1} + V_{G_J2}}{2} = \frac{(V_{GS_J1} + V_{GS_J2} + V_{DS_MOSFET1} + V_{DS_MOSFET2})}{2}$$

$$\text{Any current direction: } V_{DS_MOSFET1} = -V_{DS_MOSFET2}$$

$$\frac{V_{G_J1} + V_{G_J2}}{2} = \frac{V_{GS_J1} + V_{GS_J2}}{2}$$

Figure 8. Method of Extracting JFET Gate to Source Voltage for Combo JFET Device

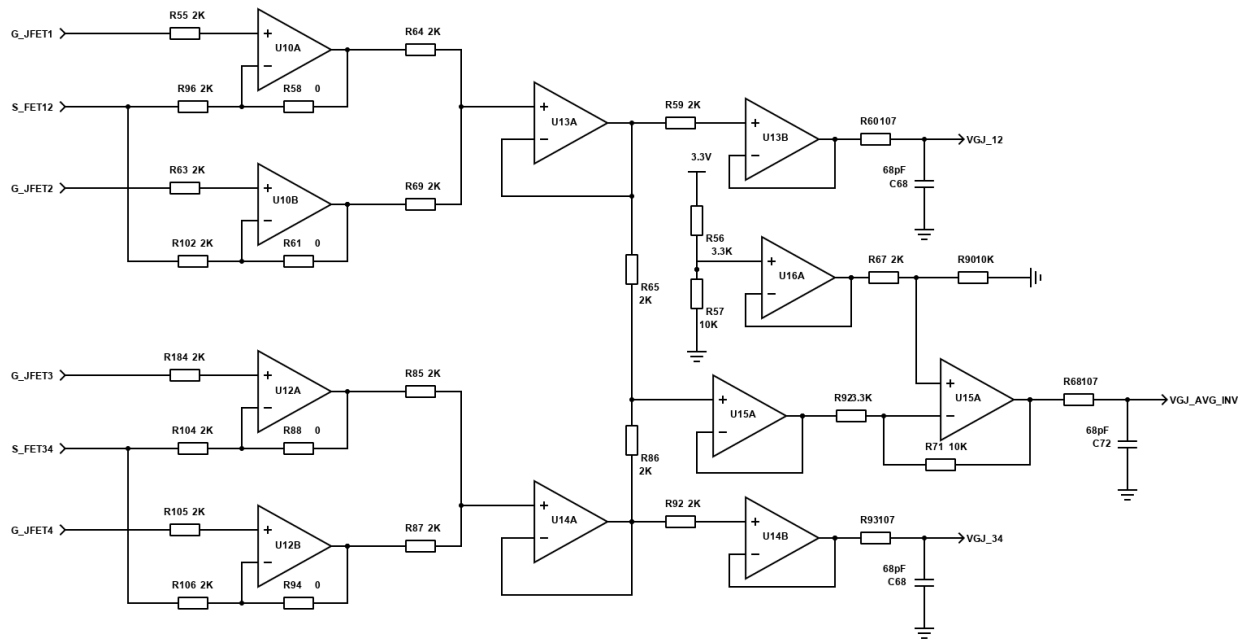


Figure 9. JFET Junction Temperature Sensing by JFET Gate Voltage Measurement

VDS Sensing

Combo JFET drain to source voltage drop is measured by utilizing desaturation circuit. The D11 and D13 (D12 and D14) are for blocking high voltage when power devices are off to protect other circuits. D4 and D6 (D3 and D5) are

series with D11 and D13 (D12 and D14) to mirror the voltage drop of D11 and D13 (D12 and D14), so the conditioning circuit can subtract the voltage drop of D11 and D13 (D12 and D14) from the measurement to have the drain to source voltage drop of the devices.

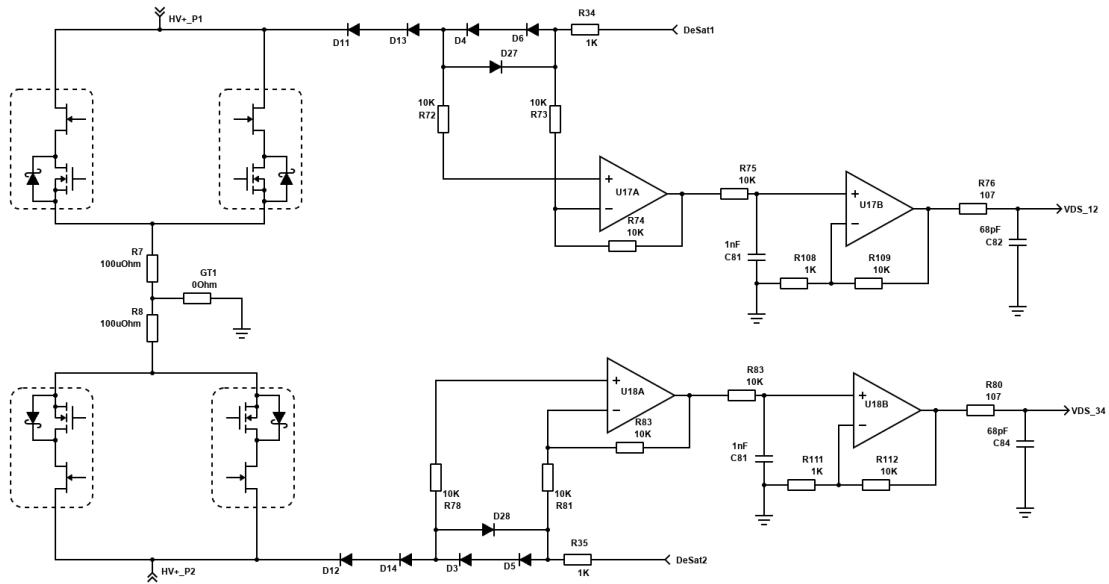


Figure 10. VDS Sensing Circuit

Analog to Digital Converter

This evaluation board uses 8-channel 16-bits analog to digital converter to read the analog signals, it can be controlled by MCU through SPI communication.

Micro-Controller Unit

QPG6105 is a low power communications controller implementing Zigbee®, Thread, Matter, Bluetooth® Low Energy and Bluetooth Mesh protocols. It features the hardware based ConcurrentConnect technology enabling multiple protocols to operate simultaneously, delivering improved capacity and enhanced interoperability with the leading low power standards.

The QPG6105 SoC and its software is Zigbee and Bluetooth Low Energy certified and a candidate for Matter v1.0 certification. The QPG6105 development kit is a one-stop shop for boards, software and documentation for easy product development. Additionally, a connected lighting reference design is available to reduce time to market for customers.

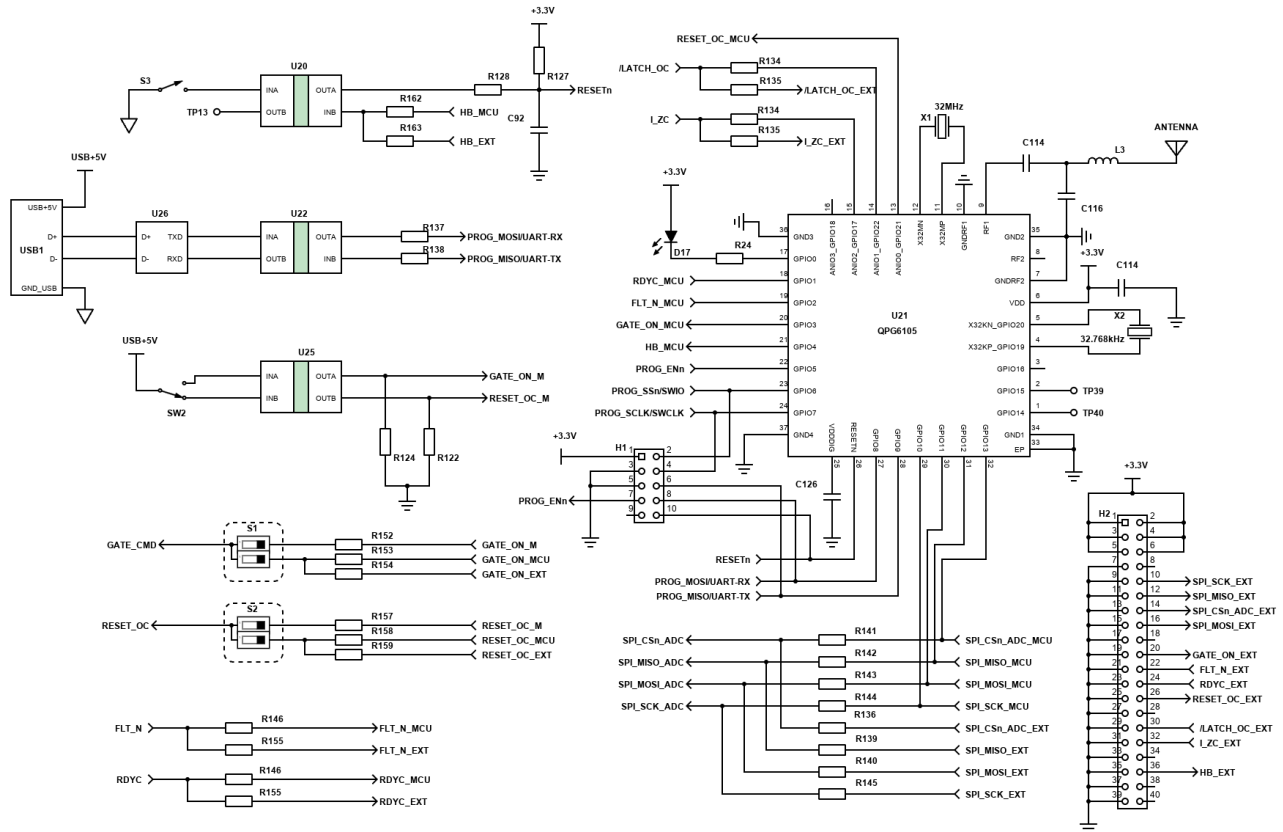


Figure 11. Control Unit Diagram

Auxiliary Power

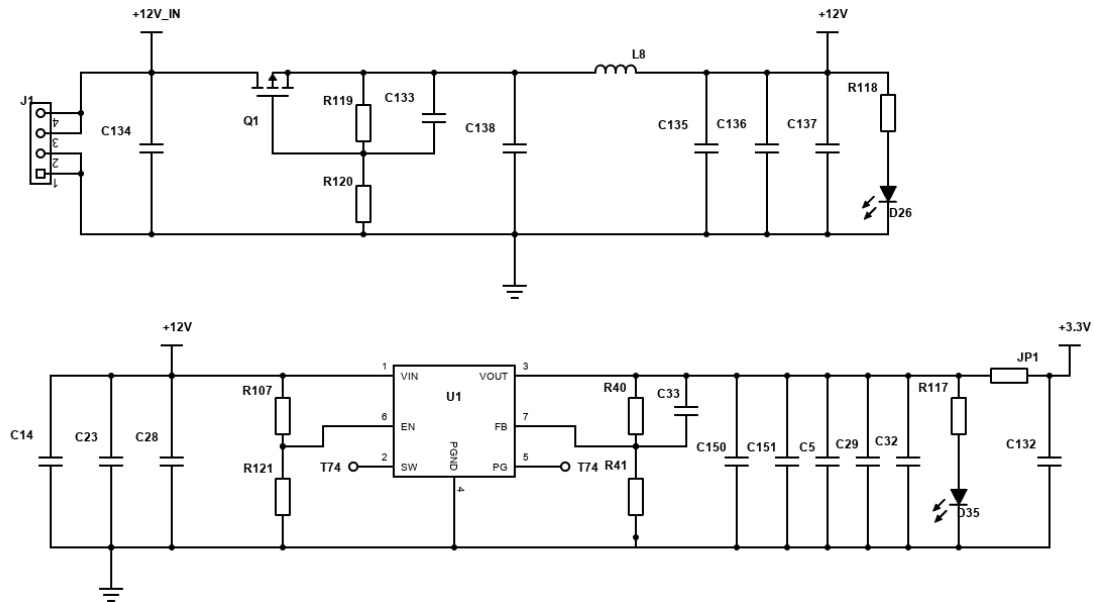


Figure 12. Auxiliary Power Diagram

Interfaces

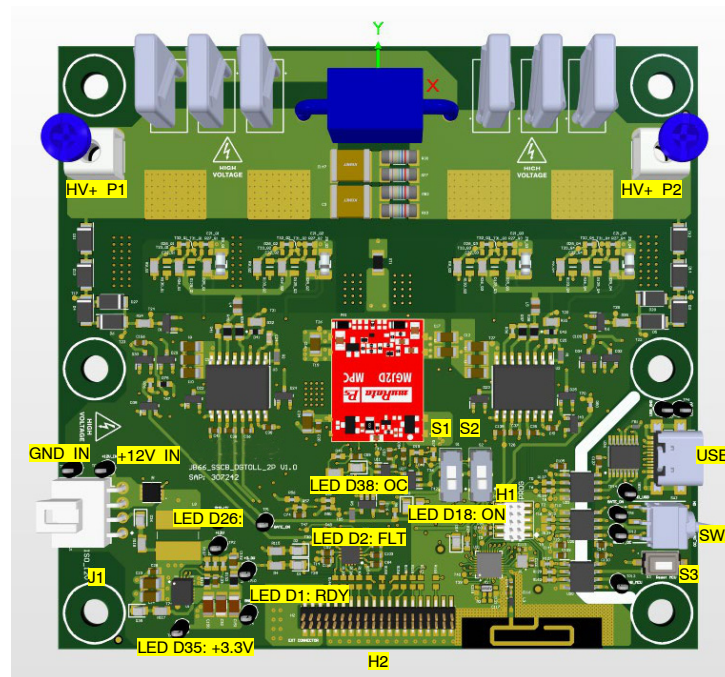


Figure 13. Interfaces

Table 1. INTERFACE DEFINITION

Interface	Function	Definition	Connector	Mating Part	Note
HV+_P1	Power Terminal 1	0–350 V AC/DC	Screw Terminal	NA	10 Arms
HV+_P2	Power Terminal 2	0–350 V AC/DC			
J1	12 V Power Supply	+12V, isolated power supply	105313–1204, Connector Header Through Hole, Right Angle 4 position 0.098" (2.50mm)	105307–1204, Rectangular Connectors – Housings Receptacle Black 0.098" (2.50mm) 1053002300, Non–Gendered Contact Gold 20–22 AWG Crimp Power	Cable connection
S1	Slide switch	GATE_ON signal switch between manual control and MCU control	NA	NA	
S2	Slide switch	RESET_OC signal switch between manual control and MCU control	NA	NA	
S3	Push button	MCU reset signal	NA	NA	
SW2	Manual control	GATE_ON and RESET_OC manual control signal	NA	NA	
H1	MCU Program connector	0/+3.3 V	FTSH–105–01–L–DV–K–TR, CONN, HDR, 10 POS, 0.050", SMD	1.27 mm, dual row, 10 position, receptacle	
H2	External access signals	0/+3.3 V	M50–3612042, Connector Header Surface Mount 40 position 0.050" (1.27mm)	1.27 mm, dual row, 40 position, receptacle	

Test Setup – Manual Control

Precaution: this test has high voltage involved and can potentially be explored if failure happens. The lab safety instructions must be followed, and users of this board shall take their own responsibility for safety.

1. For manual control mode, S1 and S2 need to be switched to the position towards MCU/Antenna side, see Figure 14.

2. Power the board with 12 V power supply (isolated to main power lines) through connector J1, or test point (+12V_IN and GND_IN).
3. Power the safe area (USB powered) by plugging in USB cable.
4. On/Off control: switch SW2 to turn the power switch on (towards antenna) or off (towards USB port), see Figure 14.

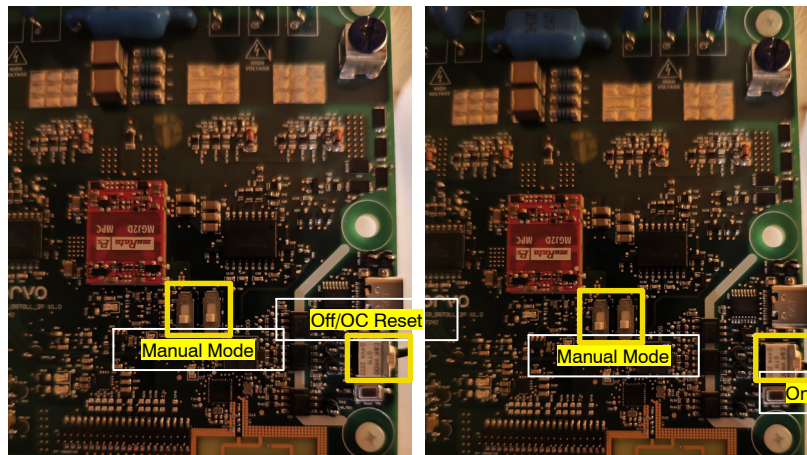


Figure 14. Manual/MCU Mode (S1 and S2), ON/OFF Switch

The test setup for over current protection is shown as Figure 15, the length of L1 and L2 is 2 feet for test results in this user guide.

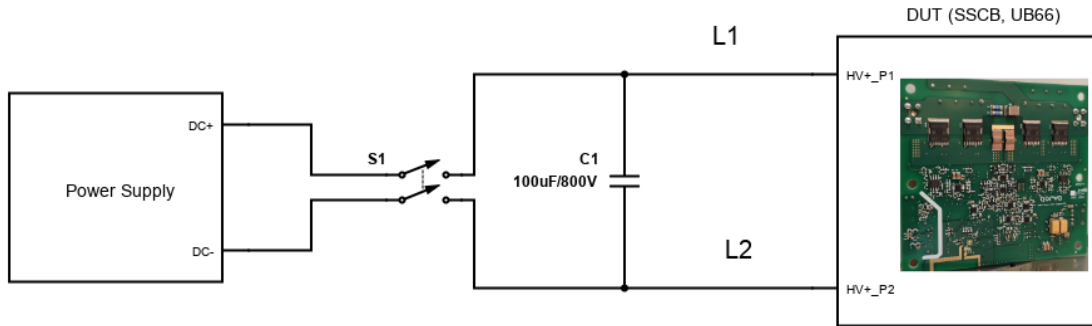


Figure 15. Over-current Protection Test Setup

Test Results

The junction temperature can be sensed by measuring the gate to source voltage of JFET when over-drive it. Details see ref [4] and ref [5]. This method was modified for the Combo JFET because there is no access to JFET source for the

Combo JFET package. This modified method can cancel the offset caused by the voltage drop of low voltage MOSFET. The test result verified this method works.

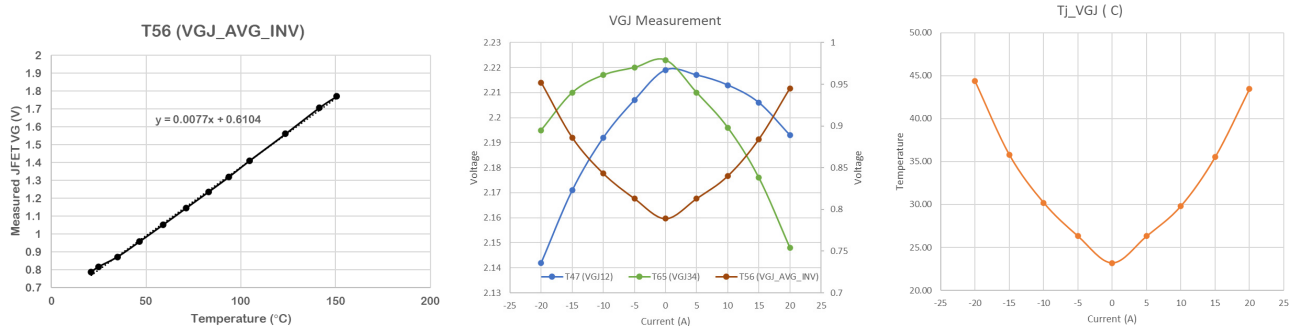


Figure 16. Junction Temperature Sensing Test Results, Left: Calibration, Middle: Comparison of with and without Low Voltage MOSFET Voltage Drop Cancellation, Right: Junction Temperature Sensing Result under Different DC Current

Figure 16 shows the results of calibration and junction temperature sensing results.

The conduction current is sensed by shunt resistors or derived from measuring of drain to source voltage drop

(V_{DS}) and estimated conduction resistance ($I = V_{DS}/R_{DSon}$), the conduction resistance (R_{DSon}) is estimated by plugging in sensed junction temperature into the curve of Normalized on-resistance vs. temperature.

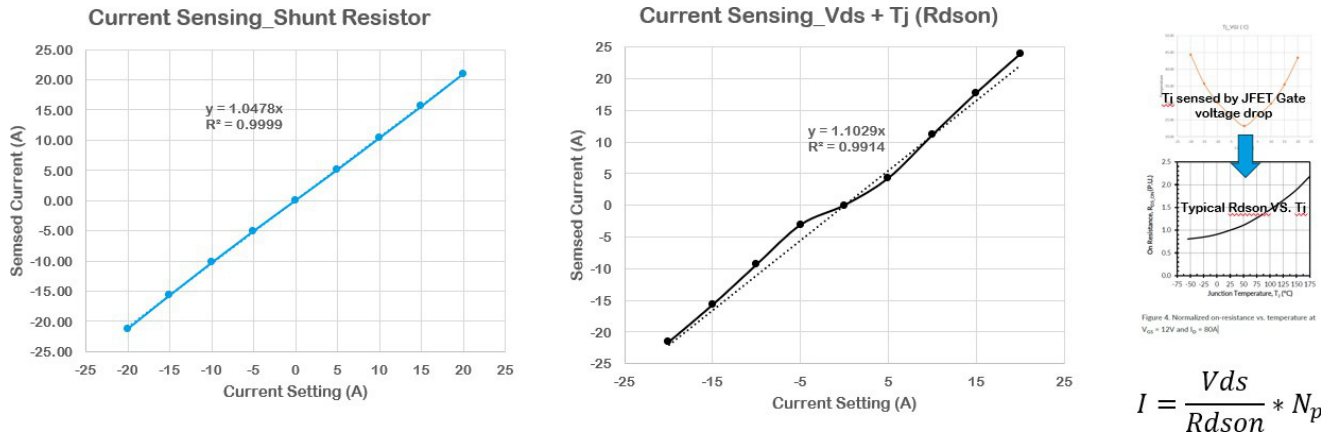


Figure 17. Current Sensing Test Results, Left: Shunt Resistors, Middle: V_{DS} and T_J , Right: Method of Current Sensing by V_{DS} Measurement

Figure 15 shows how the over-current protection is tested, the test results (Figure 18) show the effectiveness of turning off speed control by JFET gate resistance. The gate

resistance of JFET shall be selected based on the application, the limits are the switching off energy and FET over-shoot voltage must be within its safety operation area (SOA).

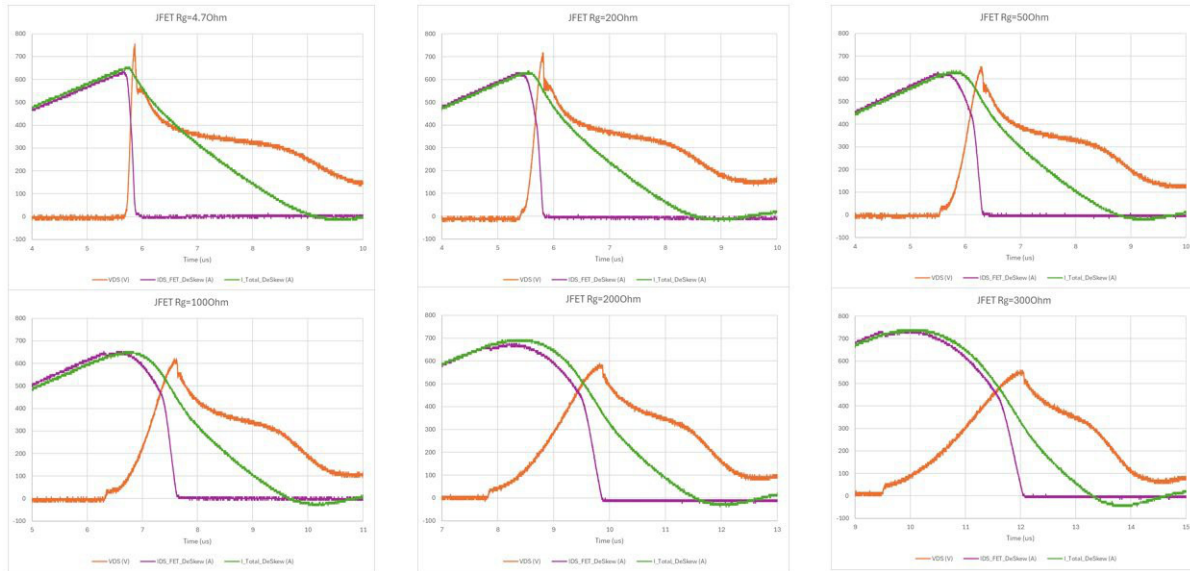


Figure 18. Over-current Protection Test Results

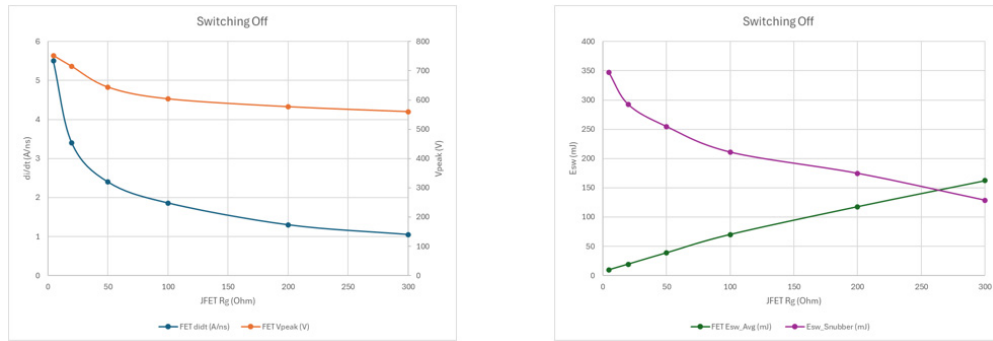


Figure 19. Over-shoot Voltage and Switching Energy with Different JFET Gate Resistance

Evaluation Board with JFET

onsemi has developed another Solid-State Circuit Breaker (SSCB) evaluation board with JFET (UJ4N075004L8S) and external low voltage MOSFET. Details refer to device website: [UJ4N075004L8S](http://www.onsemi.com/pdf/datasheet/UJ4N075004L8S.pdf)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations: www.onsemi.com

Design Documents

- [Schematic](#)
- [Gerber files](#)
- [Bill of Material \(BoM\)](#)

Qorvo name and logo are trademarks of Qorvo, Inc.

Bluetooth and the Bluetooth logo are registered trademarks of Bluetooth SIG.

Zigbee is a registered trademark of Zigbee Alliance.

All other brand names and product names appearing in this document are registered trademarks or trademarks of their respective holders.

REVISION HISTORY

Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division document and updated the main document title to comply with onsemi standards for SiC products.	1/23/2025
2	Document converted to onsemi Evaluation Board User's Manual format.	2/28/2025
3	The "Design Document" section on page 11 updated to include references to Schematics, Gerber files, and Bill of Materials (BoM).	6/23/2025

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

THE BOARD IS PROVIDED BY ONSEMI TO YOU "AS IS" AND WITHOUT ANY REPRESENTATIONS OR WARRANTIES WHATSOEVER. WITHOUT LIMITING THE FOREGOING, ONSEMI (AND ITS LICENSORS/SUPPLIERS) HEREBY DISCLAIMS ANY AND ALL REPRESENTATIONS AND WARRANTIES IN RELATION TO THE BOARD, ANY MODIFICATIONS, OR THIS AGREEMENT, WHETHER EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, INCLUDING WITHOUT LIMITATION ANY AND ALL REPRESENTATIONS AND WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, NON-INFRINGEMENT, AND THOSE ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE CUSTOM OR TRADE PRACTICE.

onsemi reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by **onsemi** shall not constitute any representation or warranty by **onsemi**, and no additional obligations or liabilities shall arise from **onsemi** having provided such information or services.

onsemi products including the boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. You agree to indemnify, defend and hold harmless **onsemi**, its directors, officers, employees, representatives, agents, subsidiaries, affiliates, distributors, and assigns, against any and all liabilities, losses, costs, damages, judgments, and expenses, arising out of any claim, demand, investigation, lawsuit, regulatory action or cause of action arising out of or associated with any unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of any products and/or the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

FCC WARNING – This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by **onsemi** to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

onsemi does not convey any license under its patent rights nor the rights of others.

LIMITATIONS OF LIABILITY: **onsemi** shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if **onsemi** is advised of the possibility of such damages. In no event shall **onsemi**'s aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

The board is provided to you subject to the license and other terms per **onsemi**'s standard terms and conditions of sale. For more information and documentation, please visit www.onsemi.com.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales