NIV3071 Evaluation Board User's Manual

EVBUM2959/D

Overview

The NIV3071MTW3GEVB and NIV3071MTW4GEVB evaluation boards are designed to support testing and evaluation of the NIV3071MTW3 and NIV3071MTW4 devices, respectively. These 4-channel eFuses operate over an input voltage range of 8 V to 60 V and provide up to 2.5 A per channel. The NIV3071MTW3 is the latch version, while the NIV3071MTW4 is the auto-retry version. The evaluation boards allow users to apply DC input voltage and loads levels within the recommended operating range as suggested in the product datasheet. For ease of evaluation, the boards include test points for all device pins, selectable output voltage slew rate adjustment capacitors via jumper settings, output voltage and enable/fault status indicator LEDs, and a potentiometer for current limit adjustment.

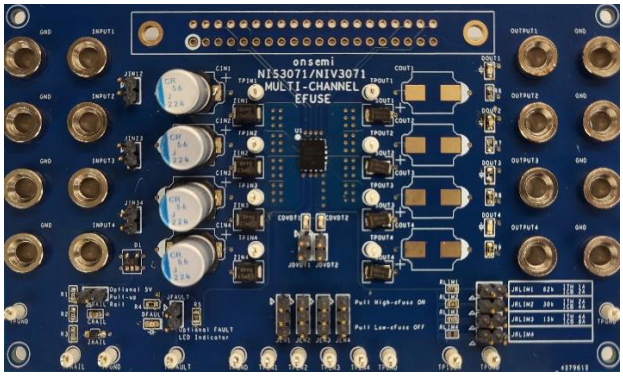


Figure 1. Evaluation Board

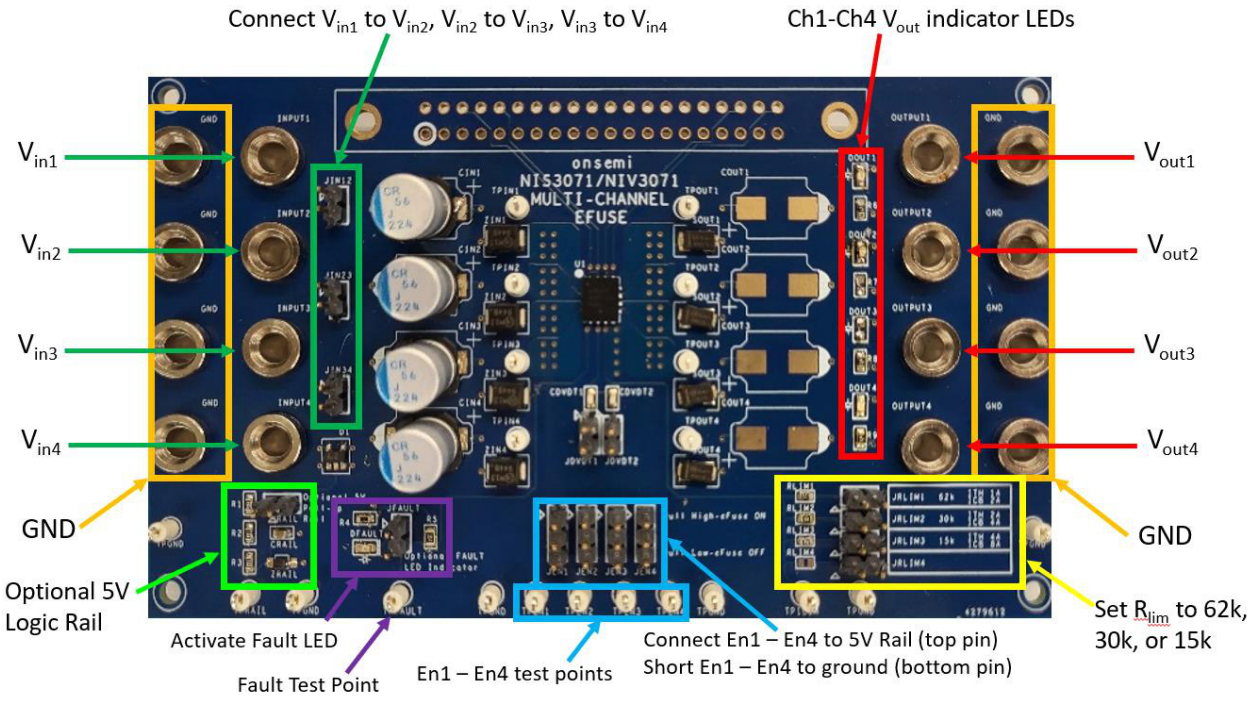


Figure 2. Features of Evaluation Board

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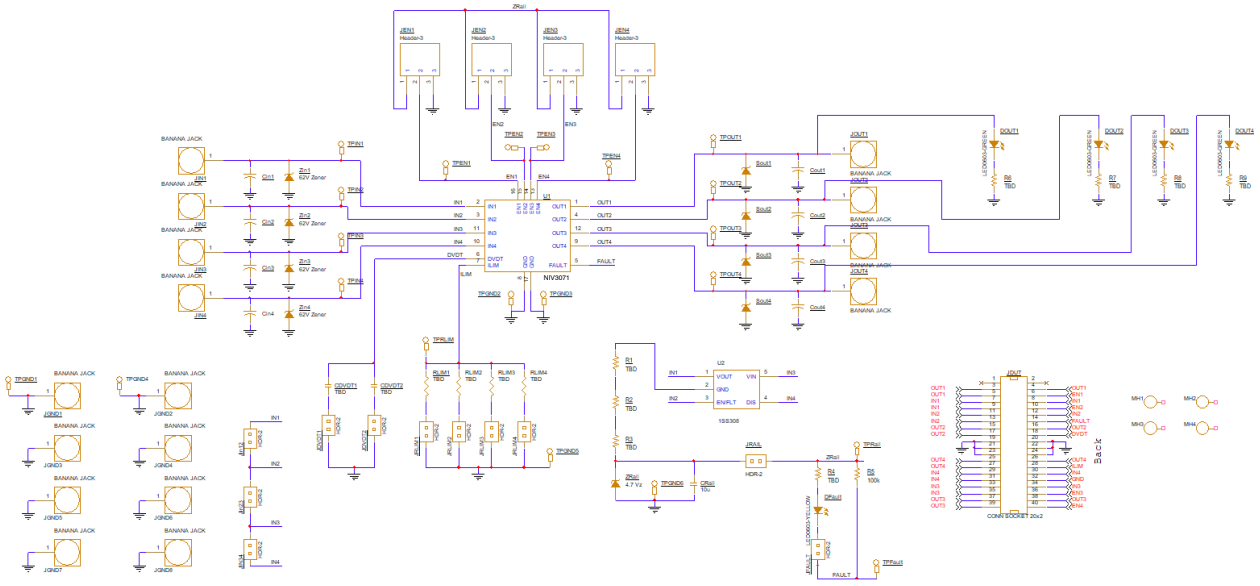


Figure 3. Evaluation Board Schematic

Table 1. BILL OF MATERIALS

Qty	Reference	Part	DigikeyPN	Manufacturer	Manufacturer Part #	Notes
21	All Test Points	TP-HOOK	36-5002-ND	Keystone Electronics	5002	
1	CDVDT1	100 pF/50 V 0603	311-1069-1-ND	Yageo	CC0603JRNPO9BN101	
1	CDVDT2	180 pF/50 V 0603	311-3890-1-ND	Yageo	CC0603FRNPO9BN181	
4	Cin1, Cin2, Cin3, Cin4	56 μF/63 V	493-13781-1-ND	Nichicon	PCR1J560MCL1GS	
4	Cout1, Cout2, Cout3, Cout4					Do not populate
1	CRAIL	10 μF/25 V 0603	311-3494-1-ND	Yageo	CC0603MRX5R8BB106	
1	U2	4 Diode Array Common Cathode	1SS309(TE85LF)CT-ND	Toshiba	1SS309(TE85L,F)	
1	DFAULT	LED0603-YELLOW	160-1448-1-ND	Lite-On Inc	LTST-C191KSKT	
4	DOUT1, DOUT2, DOUT3, DOUT4	LED0603-GREEN	160-1888-1-ND	Lite-On Inc	LTST-C191TGKT	
1	JDUT (Edge Connector)	CON40	S3314-ND	Sullins	EBC20DRTH	Do not populate
4	JEN1, JEN2, JEN3, JEN4	3-pin Header	3M9457-03-ND	3M	961103-6104-AR	
11	JRLIM1, JDVDT1, JRLIM2, JDVDT2, JRLIM3,JRLIM4, Jin2, Jin23, JIN34, JRAIL, JFAULT	2-pin Header	3M9447-ND	3M	961102-6404-AR	
16	JOUT1, JIN1, JGND1, JOUT2, JIN2, JGND2, JOUT3, JIN3, JGND3, JOUT4, JIN4, JGND4, JGND5, JGND6, JGND7, JGND8	BANANA JACK	36-575-8-ND	Keystone Electronics	575-8	
1	RLIM1	62 kΩ 0603 0.1%	P62KAYCT-ND	Panasonic	ERA-3APB623V	
1	RLIM2	30 kΩ 0603 0.1%	P30KDBCT-ND	Panasonic	ERA-3AEB303V	
1	RLIM4					Do not populate
4	R1, R2, R3, RLIM3	15 kΩ 0603 0.1%	P15KDBCT-ND	Panasonic	ERA-3AEB153V	
1	R4	100 Ω 0603 1%	P100HCT-ND	Panasonic	ERJ-3EKF1000V	
1	R5	100 kΩ 0603 1%	P100KHCT-ND	Panasonic	ERJ-3EKF1003V	
4	R6, R7, R8, R9	120 kΩ 0603 1%	P120KHCT-ND	Panasonic	ERJ-3EKF1203V	
4	Sout1, Sout2, Sout3, Sout4	Schottky Diode		**onsemi**	MBRS360BT3G	Cathode toward left of PCB
1	U1	NIV3071MTW3TWG or NIV3071MTW4TWG		**onsemi**	NIV3071MTW3TWG or NIV3071MTW4TWG	
4	Zin1, Zin2, Zin3, Zin4	Protection Zener Diode	1SMB5944BT3GOSCT-ND	**onsemi**	1SMB5944BT3G	Cathode toward right of PCB
1	ZRAIL	Regulator Zener Diode	MMSZ5230BT1GOSCT-ND	**onsemi**	MMSZ5230BT1G	Cathode toward bottom of PCB

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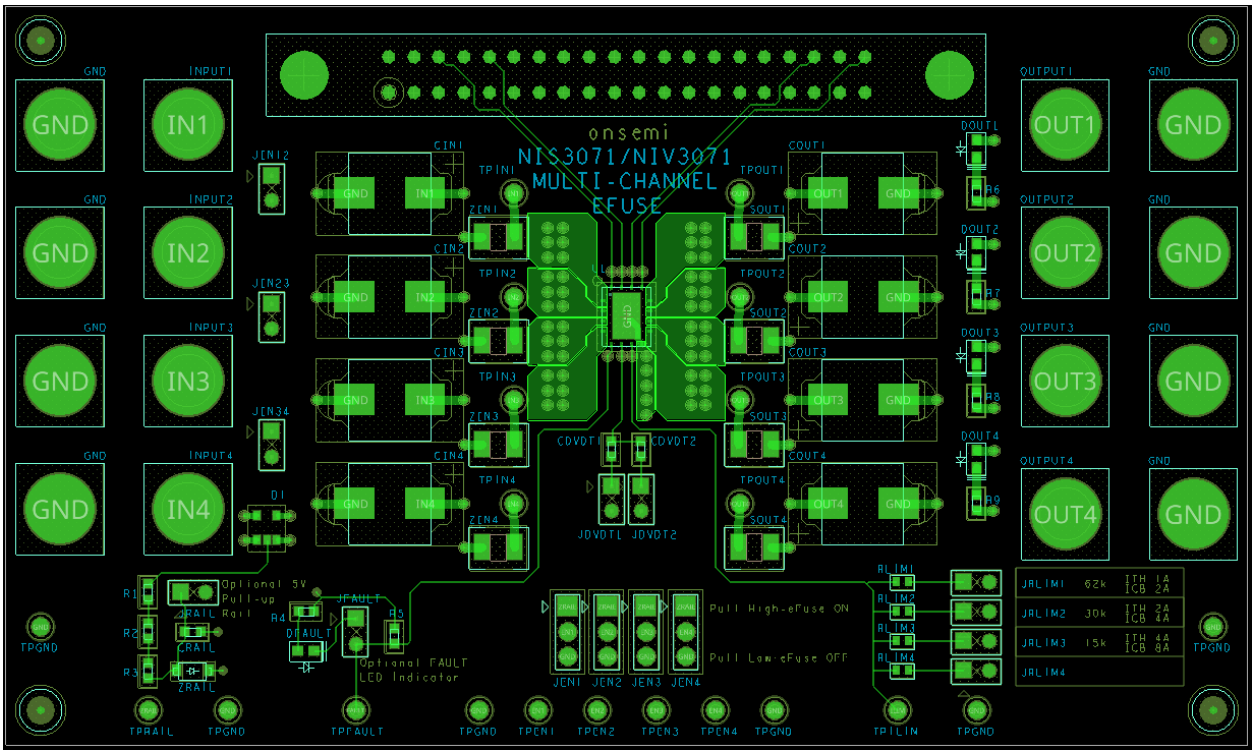


Figure 4. Evaluation Board Layout Image (6 Layers)

INSTRUCTIONS

CAUTION: Observe all precautions while testing this evaluation board (wear safety glasses, do not connect potentially dangerous high voltages, be sure to not make **incorrect** reverse connections). Do **NOT** exceed a DC input voltage of 60 V.

Board Set Up

1. Connect a DC voltage source to one or more of the 4 input banana jacks on the left-hand side. Connect the negative terminal to ground and leave the source off until all set-up steps are complete.
2. Connect a jumper across RLIM1, 2, or 3 to select an Rlim of 62 kΩ, 30 kΩ, or 15 kΩ respectively. The I_{th} and I_{CB} trip points associated with each resistor choice is located on the EVB. Use the I_{lim} test point (TPILIM to TPGND) to ensure the total resistance matches the desired value.
3. Select a dvdt adjustment capacitor by putting a jumper across JDVDT1 (100 pF), JDVDT2 (180 pF), or leave disconnected.
4. Connect a jumper to JFAULT to observe the behavior of the fault pin. A simple 5 V rail is provided externally to the eFuse by a Zener diode, which can optionally be used by connecting JRAIL.
5. Connect voltage probes to the test points of interest. It is recommended to connect to one of the input test points, one of the output test points, and to the fault pin test point.
6. Connect a load or multiple loads from one or more outputs to ground or leave the outputs floating.
7. Turn on the DC voltage source. A controlled voltage ramp is recommended due to a hot plug connection with excessive input voltage on the input potentially damaging the eFuse. Capacitors and Zeners from input to GND are there for protection, however.
8. Check the green V_{out} indicator LEDs as a quick reference for which channel(s) are on.

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Enable Testing

- The 4 enable pins control each of the 4 outputs with the same number (e.g. EN1 controls OUT1). The enables are pulled up internally but can also be externally controlled, as shown in Figure 5 below.

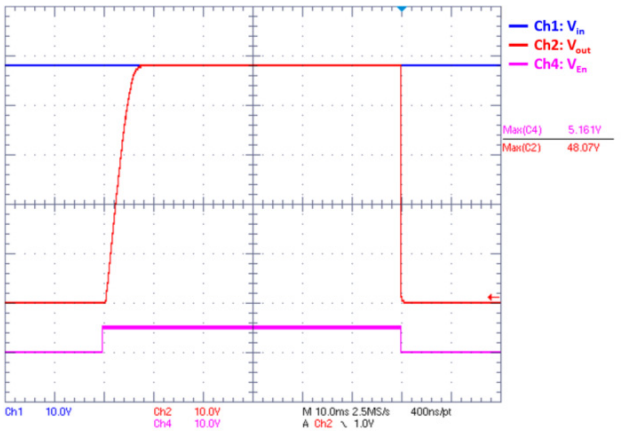


Figure 5. Turning on Output with Enable

- Pulling Enables Low
  1. Locate the 4 jumper pins at the bottom-center of the board labeled JEN1, 2, 3, and 4.
  2. Disable an enable (i.e ground the EN pin) by placing a jumper across the bottom two pins of the corresponding JEN.
     - Ex. Short Enable 1 to ground by connecting a jumper across bottom pins of JEN1.
  3. Ensure the LED on the associated output has turned from green to off.
     - *Note: If multiple output channels are shorted together, their green Vout indicator LEDs may be on even if one of those channels has been disabled.*
- Pulling Enables High
  1. Locate the 4 jumper pins at the bottom-center of the board labeled JEN1, 2, 3, and 4.
  2. Pull an enable high (to 5 V) by placing a jumper across the top two pins of the corresponding JEN.
     - Ex. Pull Enable2 high by connecting a jumper across top pins of JEN1.
     - *Note: All enables are pulled high internally by NIV3071 if left floating.*
- Controlling Enables
  1. Locate the 4 Test Points on the bottom of the board labeled TPEN1, 2, 3, and 4.
  2. Connect a voltage source to the inputs and to the enable(s) that will be controlled.
  3. Connect a voltage probe to the input and output associated with controlled enables.
  4. Set the input voltage source between 7 and 60 V.
  5. Set the enable voltage source between 0 and 0.4 V, this is the enables off state.
  6. Observe the output voltage is now 0 V and not changing with the input.
  7. Set the enable voltage source between 1.2 and 5 V, this is the enables on state.
  8. Observe the output voltage is now at the input voltage value, and changes with it.

Paralleling Channels

- This device allows for each of the 4 channels to operate independently of one another, or in parallel to increase the maximum supported load current.
- Connecting Inputs
  1. Locate the 3 jumper pins on the left-hand side of the board labeled JIN1-2, 2-3, and 3-4.
  2. Connect the inputs together by placing a jumper across the JIN pin.
     - Ex. Connect INPUT1 to INPUT2 by connecting a jumper across JIN1-2.
  3. Note that the only connections available are 1 to 2, 2 to 3, and 3 to 4.
- Connecting Outputs
  1. Locate the 4 output banana jacks on the right-hand side of the board labeled OUTPUT1, 2, 3, and 4.
  2. Connect the outputs by connecting a cable across the 2 outputs of interest.
     - Ex. Connect a cable across OUTPUT1 to OUTPUT 2 to connect the channels.

Multi-Channel Use

- An additional functionality of the device is the ability to operate each channel independently of the others, each with their own input, output, enable, and protection.
- Two Rail Configuration Test
  1. Parallel Channels 2 and 3 (inputs and enables) using jumpers as described in the above section.
  2. Connect a 12 V voltage source to INPUT1 and a 48 V source to INPUT2 or 3.
  3. Connect a voltage probe to the output 1 test point (TPOUT1), the output 2 or 3 test point, and the fault voltage test point (TPFAULT). Connect an ammeter to output 2 or 3.
  4. Follow the ITH or I_{CB} fault event tests below to cause a fault on channel 2 and 3.
  5. Observe the output 1 voltage remaining constant while the output 2 and 3 voltage drop to 0 (See Figure 6).

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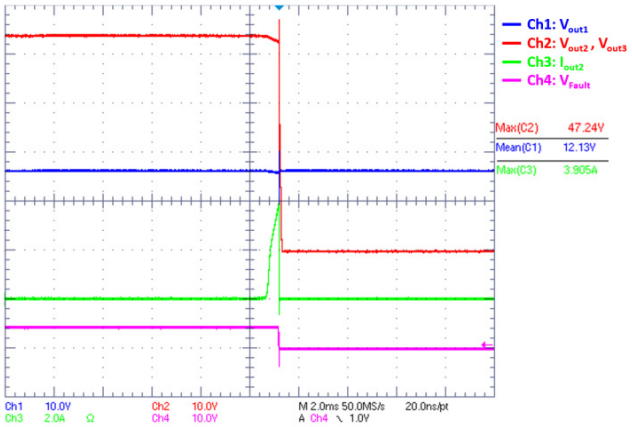


Figure 6. Turning Off 48 V Rail with I_{CB} Event while 12 V Rail Stays On

Under Voltage Lock Out

- This device will automatically set the output to 0 V when the input voltage is below 6V as can be seen in Figure 7 below.

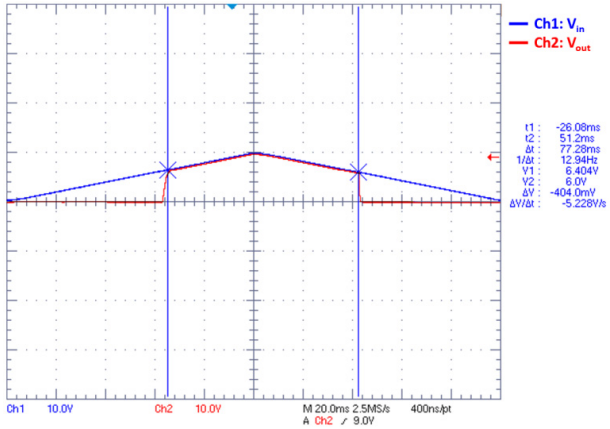


Figure 7. Slow Input Ramp to Show UVLO

- UVLO Test
  1. Connect the DC voltage source at the input(s) to be tested.
  2. Connect a voltage probe at the input and output test points.
  3. Use a voltage ramp to vary the source at the input from 10 V to 5 V.
  4. Take note of the input voltage level when the output falls to 0 V.

Turn on Time

- The turn on time (or slew rate) of the output can be adjusted by connecting a capacitor from the dvdt pin to ground. In this EVB's case, there are 2 different capacitors to choose from that will show this functionality effectively.
- Changing Turn on Time
  1. Locate the 2 jumper pins on the board labeled JDVDT1 and 2.
  2. Leave the jumper pins disconnected for the first test case.
  3. Connect a voltage probe from an oscilloscope to the input and output to be tested.
  4. Connect a voltage source at the input set anywhere between 7 and 60 V.
  5. Connect a voltage source at the enable set anywhere from 0 to 0.4 V (enable off).
  6. Change the enable voltage to between 1.2 and 5V (enable on).
  7. Observe the time it takes for the output voltage to rise to the input level.
  8. Set the enable back to its off state.
  9. Repeat steps 6–8 with a jumper across JDVDT1, JDVDT2, and both. The expected results can be seen in Figure 8 below.

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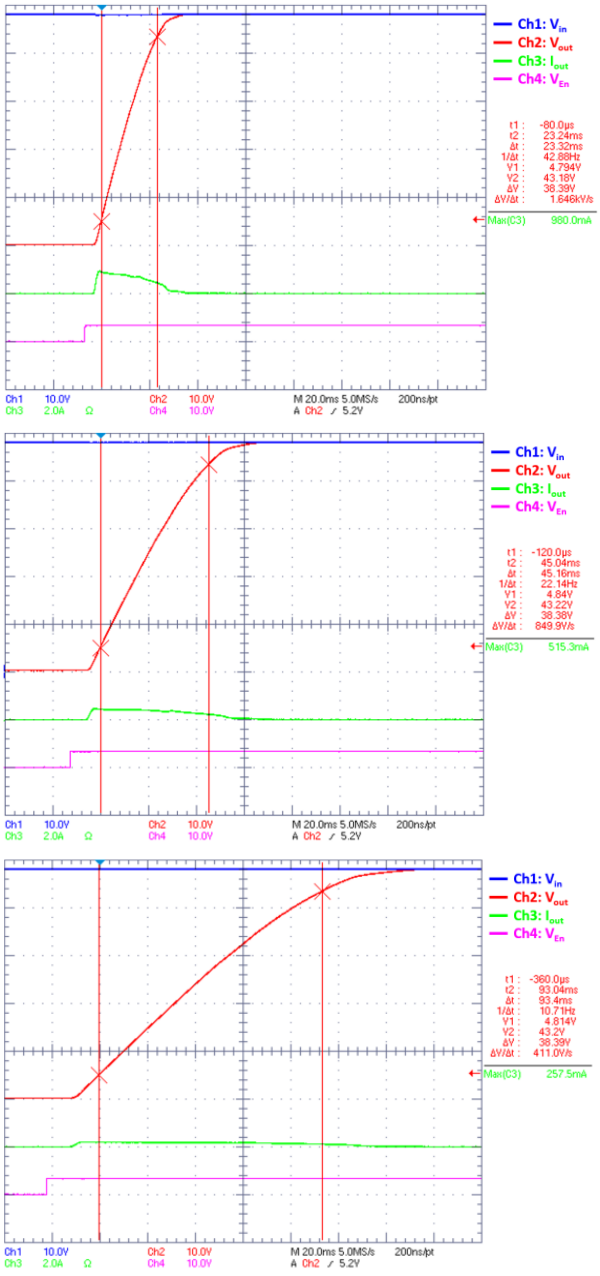


Figure 8. Turn On Time for Increasing DVDT Capacitance

R_{ds_on}

- The total resistance of the device when powered on is an important metric to note for desired applications.
- Measuring On Resistance
  1. Connect a voltage source at the input set anywhere between 7 and 60 V.
  2. Connect a load that would push ~100 mA through the device.
  3. Connect a voltage probe at the input and output pins in the middle of the board.
     - *Note: For the most accurate measurement, a kelvin connected measurement should be used*
  4. Divide the measured voltage by the current through the device, this is the devices on resistance.
     - Ex. 0.080 mV/100 mA = 80 mΩ

I_{TH}

- I_{TH} is a threshold current that, when reached or exceeded for longer than 1.5 ms, will turn off the eFuse. The value of I_{TH} is set by R_{Lim} and that relationship can be seen in Figure 5 of the datasheet.
- I_{TH} Fault Event
  1. Connect an E-load at the output.
  2. Connect a voltage source at the input set anywhere between 7 and 60 V.
  3. Connect a current probe and a voltage probe from an oscilloscope to the output.
  4. Slowly ramp up the current being drawn from the output eFuse, waiting longer than 1.5 ms on each step.
  5. Observe the current going through the eFuse at the moment the output goes to 0 V.
  6. Check that the fault pin is low through probing its test point (CH4 on Figure 9) or seeing the associated LED turn orange.
  7. Ground, then pull up the enable(s) associated with the output to reset the channel if using a latching device.

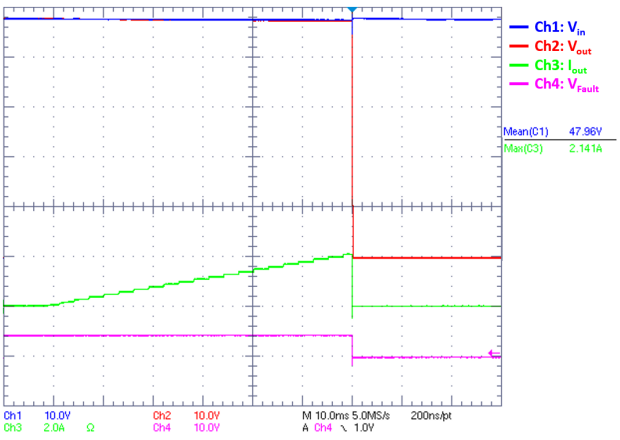


Figure 9. Output Turn Off Due to I_{TH} Event (R_{lim} = 30 kΩ)

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- I_{TH} Fault Event
  1. Follow Steps 1−3 in previous section for set-up.
  2. Quickly (in less than 1.5 ms) ramp the current being drawn from the output eFuse up to a fault level current, and then down to a current below fault level.
  3. Observe the peak of current going through the eFuse and the output voltage level.
  4. Check to ensure the pulse width of the overcurrent value was less than 1.5 ms and the output never dropped to 0 V.

I_{CB}

- I_{CB} is a threshold current that, when reached or exceeded, will immediately turn off the eFuse. The value of I_{CB} is set by R_{Lim} and that relationship can be seen in Figure 5 of the datasheet.
- ICB Event
  1. Connect an E-load at the output.
  2. Connect a voltage source at the input set anywhere between 7 and 60 V.
  3. Connect an ammeter and a voltage probe from an oscilloscope to the output.
  4. Quickly ramp up the current being drawn from the output eFuse, ensuring that the current will reach the I_{CB} limit faster than 1.5 ms.
     - *Note: If this ramp is not fast enough, I_{TH} may trigger first.*
  5. Observe the current going through the eFuse at the moment the output goes to 0 V.
  6. Check that the fault pin is low through probing its test point (CH4 on Figure 10) or seeing the associated LED turn orange.

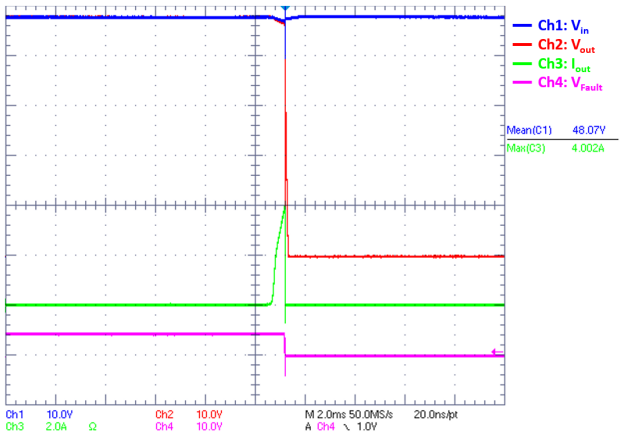


Figure 10. Output Turn Off Due to I_{CB} Event (R_{lim} = 30 kΩ)

Thermal Shutdown

- When the temperature of the eFuse reaches 175 °C, it will enter thermal shutdown to protect itself from damage.
- TS Test
  1. Connect a voltage source at the input set anywhere between 7 and 60 V.
  2. Connect a voltage probe at the output test points on the right side of the board.
  3. Bring the temperature of the device up through the following methods:
     - Power dissipation through high current.
     - Placing into an oven with ambient temp at 175 °C.
     - Using a heating element.
  4. Observe the temperature of the device through a thermal camera or other thermal sensor.
  5. Record the temperature of the device at the moment the output voltage drops to 0 V.

Bias Current

- Measuring Bias Current
  1. It is difficult to measure the bias current on evaluation board from the additional currents seen from the 5 V logic rail and LED indicators on the PCB. It is recommended to measure this current on a simpler PCB, however, it can still be done by removing the extra components mentioned above.
  2. Once components are removed, connect a voltage source at the input and set anywhere between 7 and 60 V.
  3. Connect an ammeter between the PCB and the input source.
  4. Set the Enable pin low to measure the off-state bias current. Set the Enable pin high to measure the on-state bias current.

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REVISION HISTORY

Revision	Description of Changes	Date
2	Document converted to **onsemi** format.	11/6/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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