User Guide for NCP3286 Evaluation Board

EVBUM2967/D

This user guide is intended to assist those using the NCP3286 BGA359 Evaluation Board. It will provide useful tips and procedures for powering up and using the Evaluation Board (EVB). It is intended as a quick-start guide rather than a comprehensive manual.

DESCRIPTION

The NCP3286 Evaluation Board BGA359 is a test vehicle for the PMBus-compatible NCP3286 single-phase voltage regulator. The printed circuit board assembly (PCBA) contains all the circuitry and connections necessary to evaluate the performance of the NCP3286 under various load and system conditions, including PMBus operation. The PCBA includes a BGA359 socket (if provided) which directly interfaces with an Intel Generation 4 Voltage Regulator Test Tool (Gen4 VRTT).

Features

- V_{IN} =3 V ~ 18 V with Input Feed-forward
- V_{OUT} = 0.5 V ~ 5.5 V with Remote Output Voltage Sense
- Stackable up to 160 A with 4 devices in Parallel
- Fixed-Frequency Current-Mode Control
- Integrated 5V LDO or External 5V Supply
- Enable with Programmable Vin UVLO
- Programmable Switching Frequency
- Programmable Boot Up Voltage
- Programmable Soft Start
- Output Discharge in Shutdown
- Programmable Current Limit
- Under-Voltage Protection and Over-Voltage Protection
- Programmable Thermal Shutdown Protection
- Selectable Protection Mode (Latch-off or Hiccup)
- Power Good Indicator
- Internal Registers to Record Faults

Quick Start Connection Guide

1. Connect the power supplies.
   There are two pairs of power input terminals:
   a. Input Power: provides power for PVIN pin of the device
   b. Logic Power: provides power for various logic and LDO circuits, as well as the I2C/PMBus interface signals (SCL, SDA and Alert#).

   Connect the power supplies for Input Power and the Logic Power connectors shown in the table below.

J71	Input Power Ground
J74	Input Power: 4.5 V to 18 V (12 V typ.), 5 A min current limit
J73−1	Logic Power Ground
J73−2	Logic Power: +5 V, 1 A current limit

2. Enable the device. There are two options to enable the device.
   a. Through the Enable Switch (SW3): set jumpers so that pin 2 and pin 3 of header J78 are shorted and also pin 1 and pin 2 at header J115 are shorted
   b. Through Input Voltage with a voltage divider: short pin 1 and pin 2 of header J78 with a jumper and leave header J115 open
   Once the device is enabled, the green LED (D22) indicating PGOOD should light.
3. I2C interface:
   a. Connect the I2C Interface Module with the NCP3286 EVB through the I2C Interface Header, as shown in Figure 2.
4. Start up the GUI application. If not installed, install dgSCOM software/GUI with dgSCOM Setup.exe.
5. Connect the external load either or both pairs of screw terminals (J70/J69 and J145/J146). Leave the load disconnected or OFF until the board has been powered up successfully.
6. Use the following test points for specific measurements.

J72(+), J66(−), R176	Input current measurement (10 A/V)
J119	output ripple measurement
J147, J148, J149	VIN/VOUT kelvin voltage test points for efficiency measurement
J133, R275	closed-loop response/measurement and connecting ac injection tool

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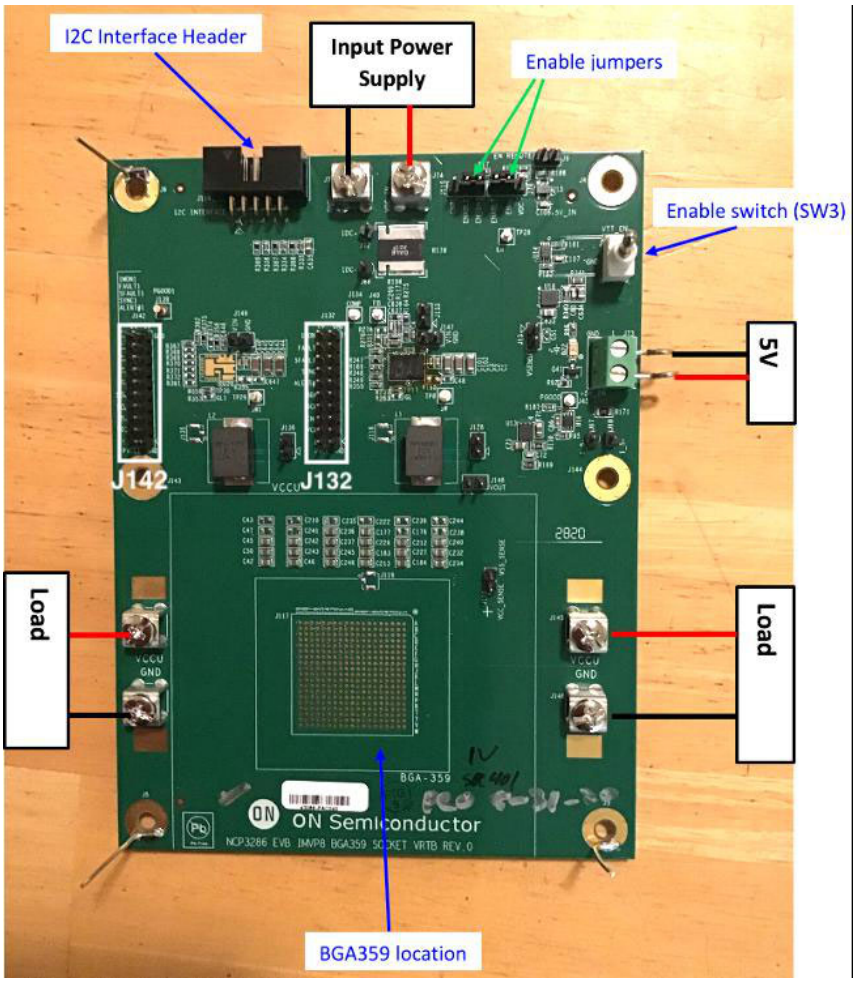


Figure 1. Evaluation Board Connection Diagram

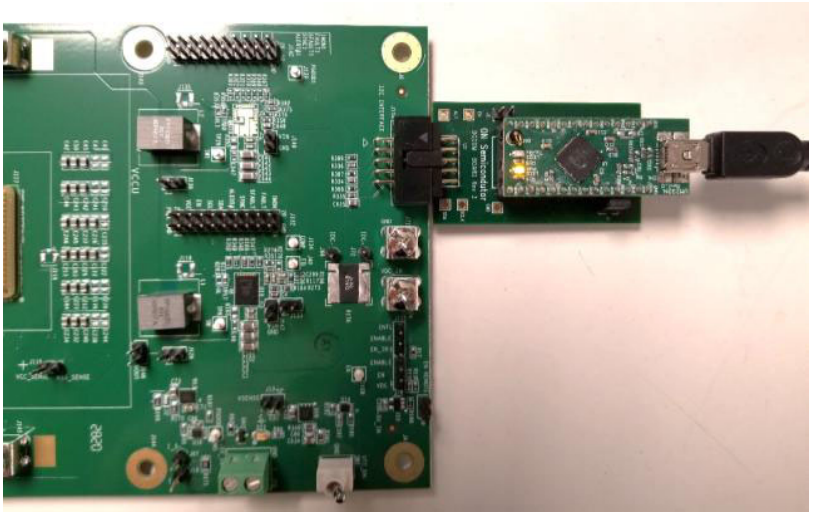


Figure 2. Evaluation Board I²C Interface Module Connection Diagram

EVALUATION BOARD SPECIAL FEATURES

Direct Logic Signal Access

The evaluation board comes with the output pins to access logic controls including the I^2C through the pin headers (J132 and J142).

GUI Application

1. Click the Connect button to establish connection between the GUI and the I2C Interface Module. dgSCOM should recognize the I2C Interface Module as UM232H. FT_OK is shown after connecting the GUI to the I2C Interface Module properly.

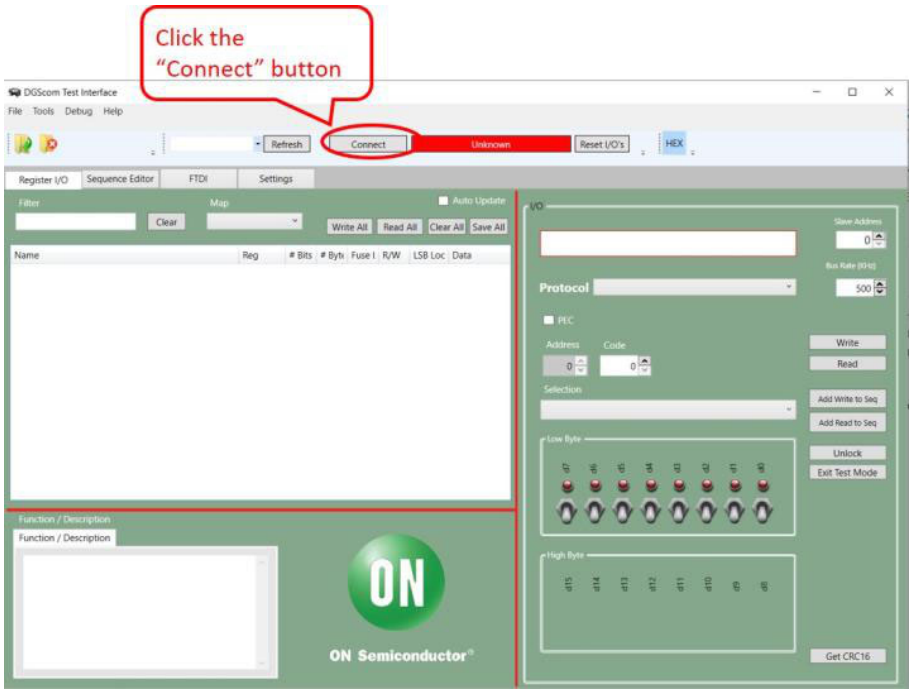


Figure 3.

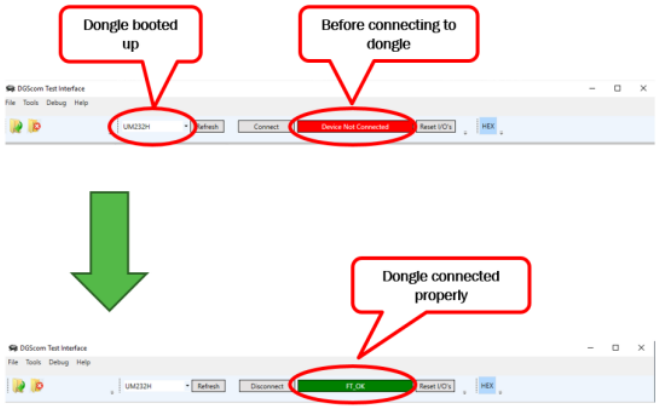


Figure 4.

2. Click the icon shown below to load the register map

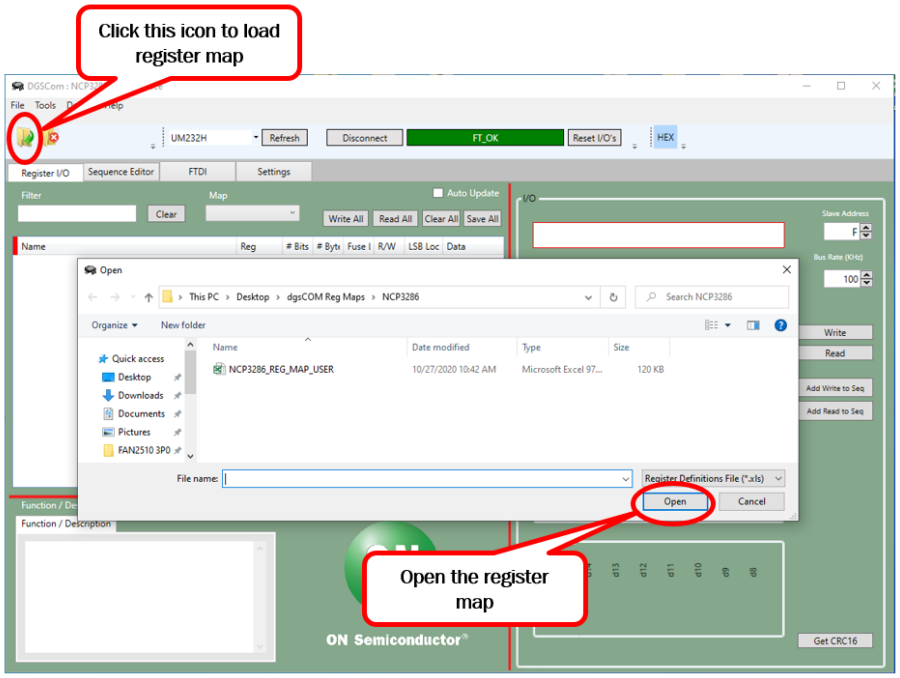


Figure 5.

3. dgSCOM GUI after loading register map:

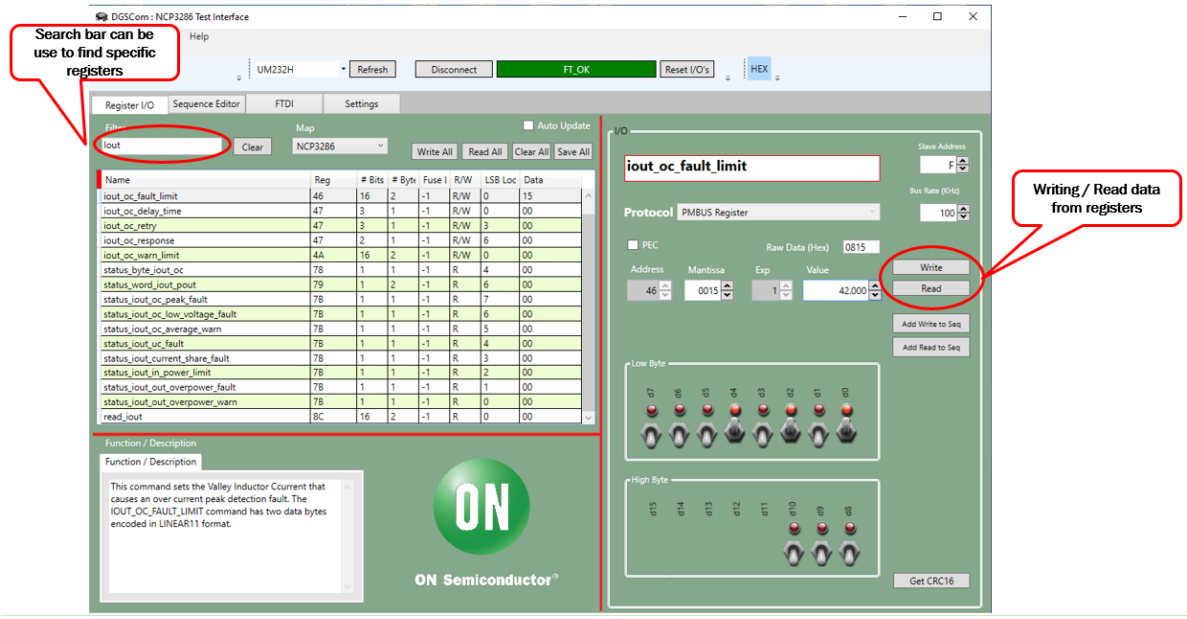


Figure 6. Register Map of GUI

Now you can write to the registers to change the parameters of the device, as long as VCC is present on the board (through either the LDO or an external +5 V supply). The device(s) does not need to be enabled to change the operating parameters. If the defaults are modified by PMBus commands, these values will persist, even if the EVB is disabled, until VCC is below the UVLO threshold.

Operation using Gen4 VRTT

The EVB is designed to use the Gen4 VRTT as a test tool for load transients only. All communications with the NCP3286, including, but not limited to, setting the output voltage and monitoring fault conditions, must be executed though the I2C Interface Module and the dgSCOM software/GUI.

1. Plug Gen4 VRTT directly into the BGA359 socket (J117, if provided) on the EVB. When inserted properly, the Gen4 VRTT will have the control board facing to the right, as shown in Figure 7.
2. Apply the power cable to the Gen4 VRTT
3. Connect the USB cable with the Mini 'B' end to the VRTT and connect the 'A' end to the computer USB port
4. Start the Gen4 VRTT program and set the rail for VCCGT. This will select the correct rail for VRTT operation.



Figure 7. NCP3286 2-Phase EVB with Gen 4 VRTT installed in BGA359 Socket

EVALUATION BOARD CONFIGURATIONS

The default settings for the NCP3286 Evaluation Board are:

Resistor Value @ the Pin	Settings
Pin 11 = 10 kΩ,	SS time = 1 ms, Vout_Scale = 1/1
Pin 12 = 33.2 kΩ	ILIM/IMON = 42 A/phase
Pin 13 = 82.5 kΩ	VBOOT = 1.00 V @Vout_Scale = 1/1
Pin 14 = 10 kΩ	ADDRS =10h (Master)
Pin 17 = 10 kΩ (1-Phase) or 24.7 kΩ (2-Phase)	Switching Frequency = 500 kHz

All of these parameters (except PMBus Master address) can be changed via PMBus.

SCHEMATIC

2-Phase Evaluation Board Schematic

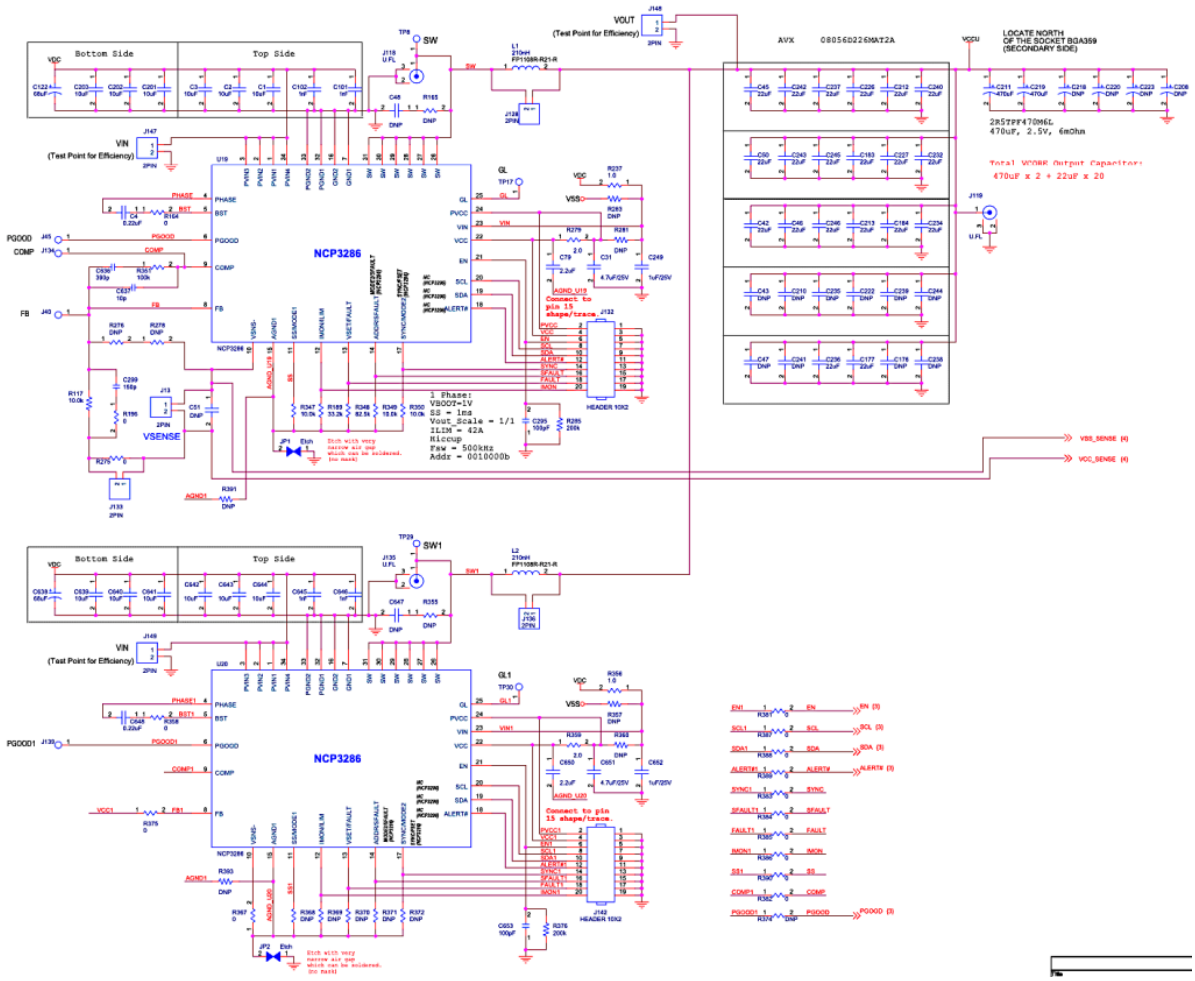


Figure 8. 2-Phase Evaluation Board Schematic, Part 1

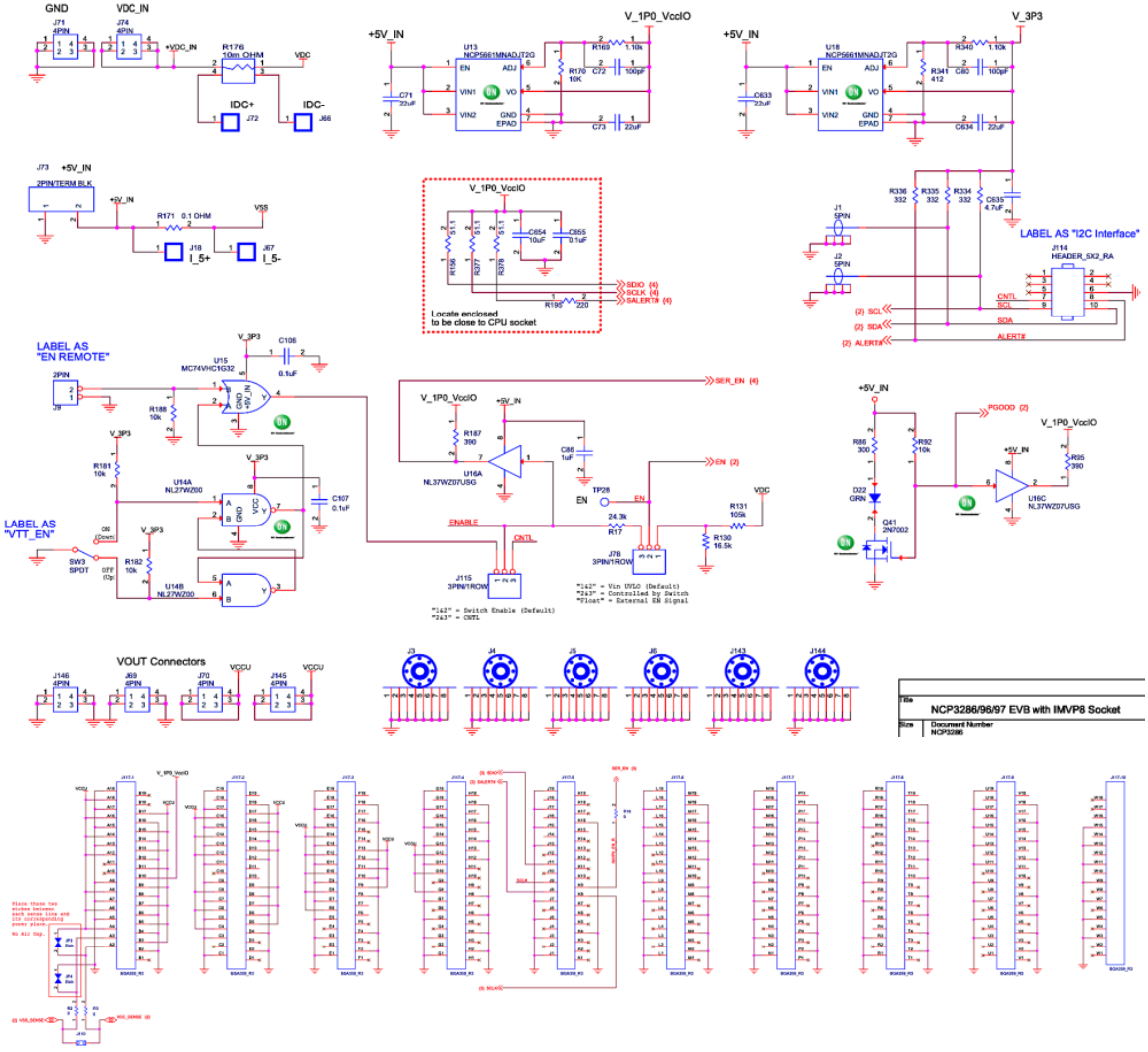


Figure 9. 2-Phase Evaluation Board Schematic, Part 2

4-Phase Evaluation Board Schematic

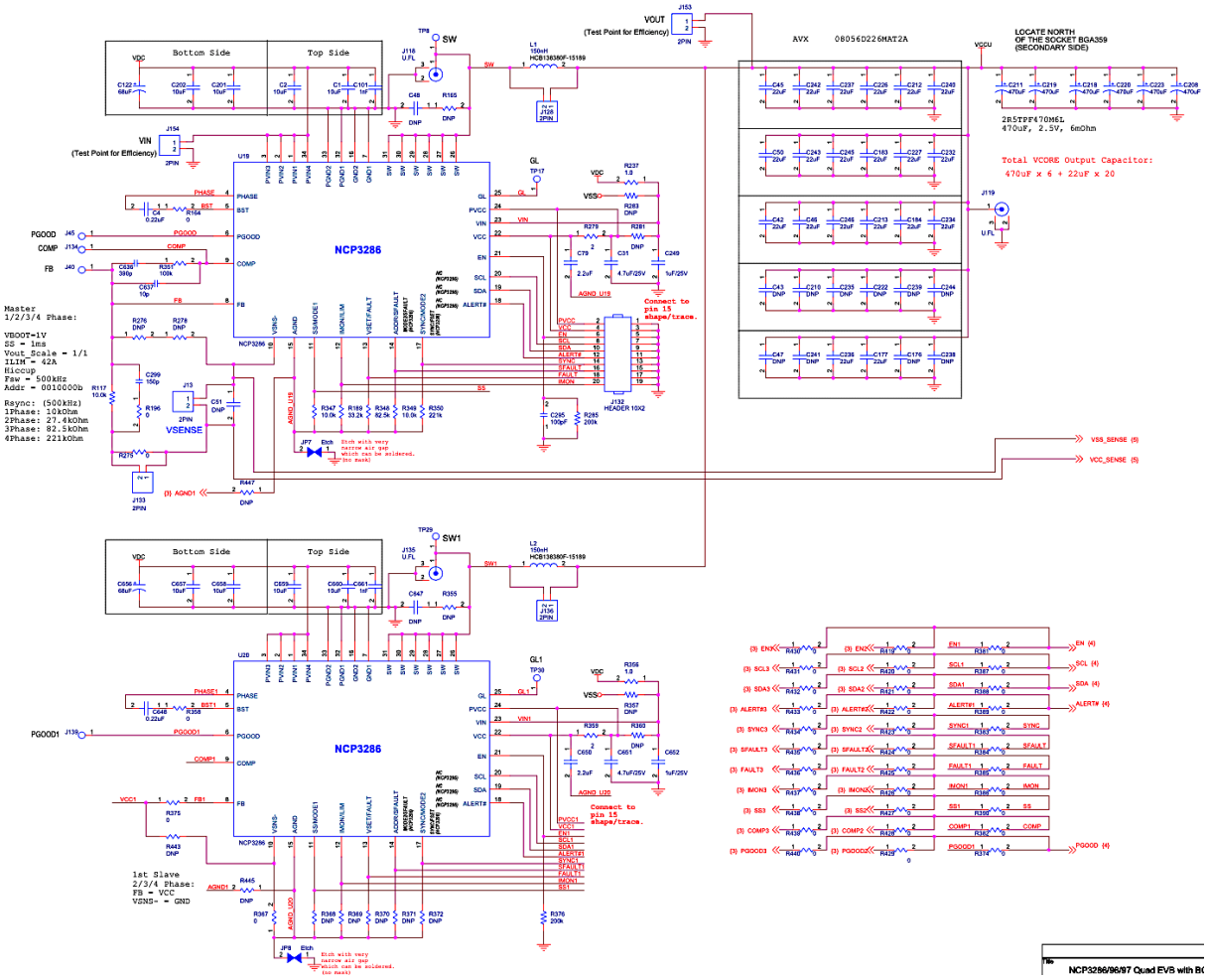


Figure 10. 4-Phase Evaluation Board Schematic, Part 1

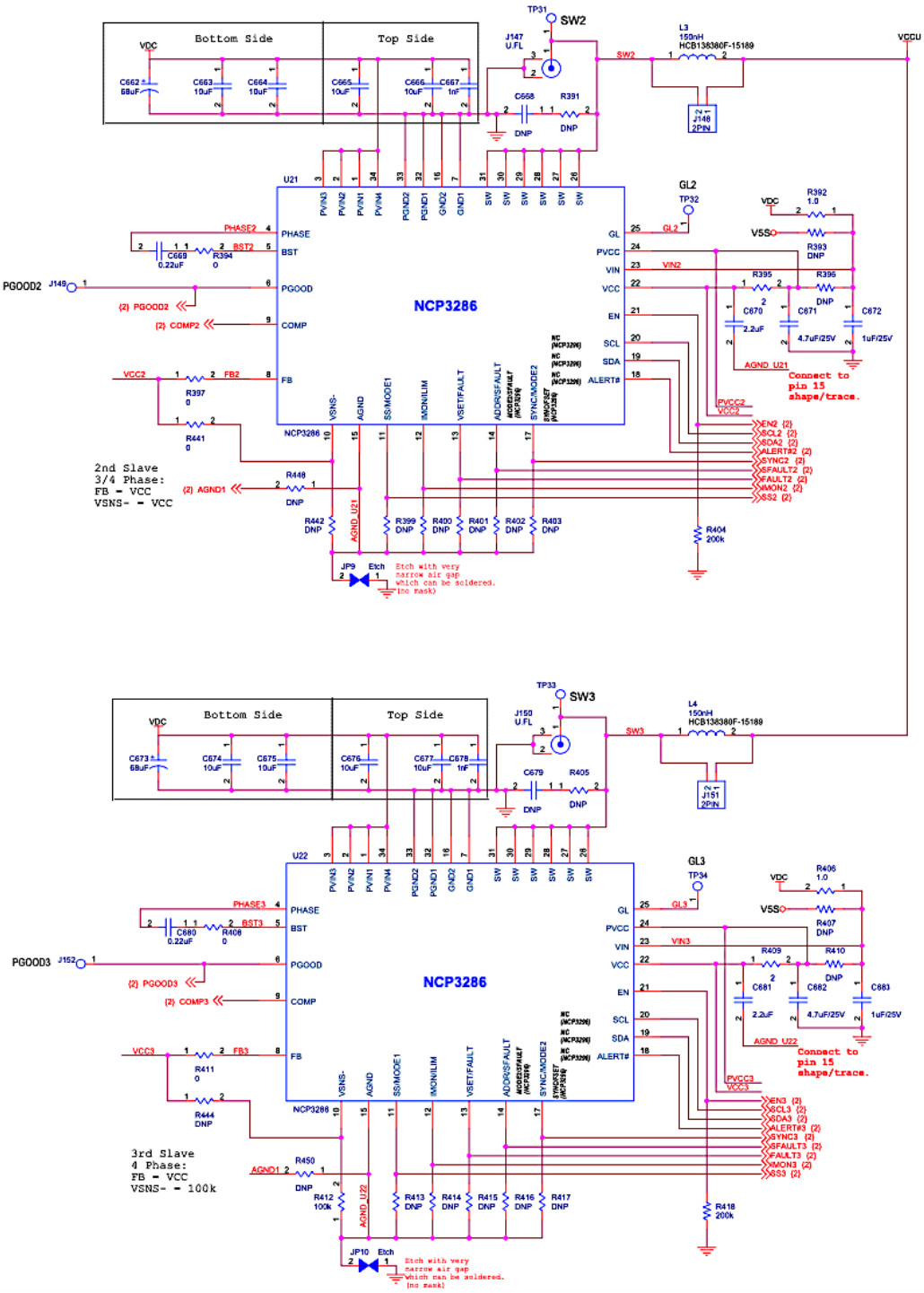


Figure 11. 4-Phase Evaluation Board Schematic, Part 2

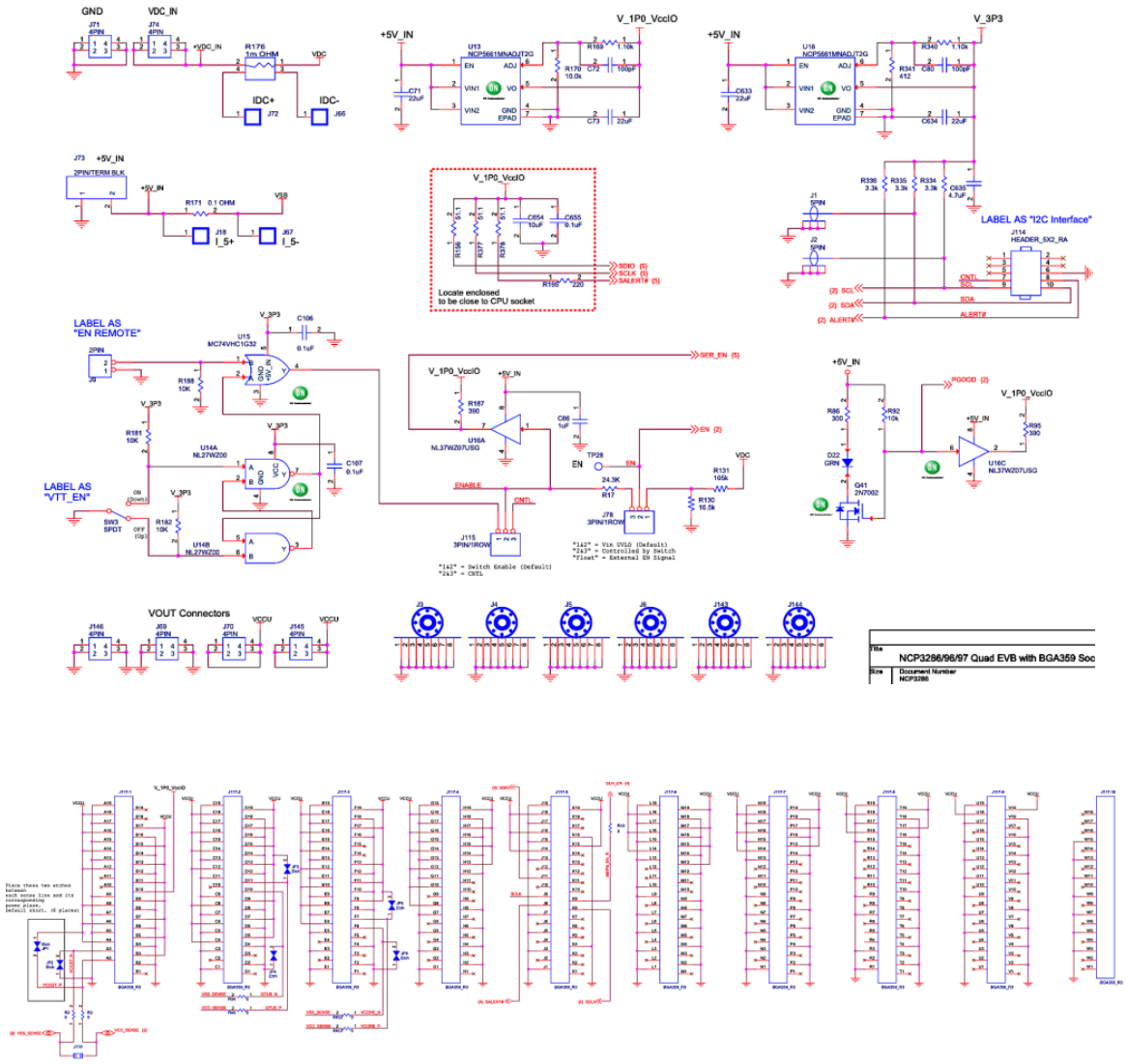


Figure 12. 4-Phase Evaluation Board Schematic, Part 3

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	11/2/2025

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