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NB3W800LMNGEVB

Evaluation Board Manual

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EVALUATION BOARD MANUAL

NB3W800LMNGEVB Evaluation Board Manual

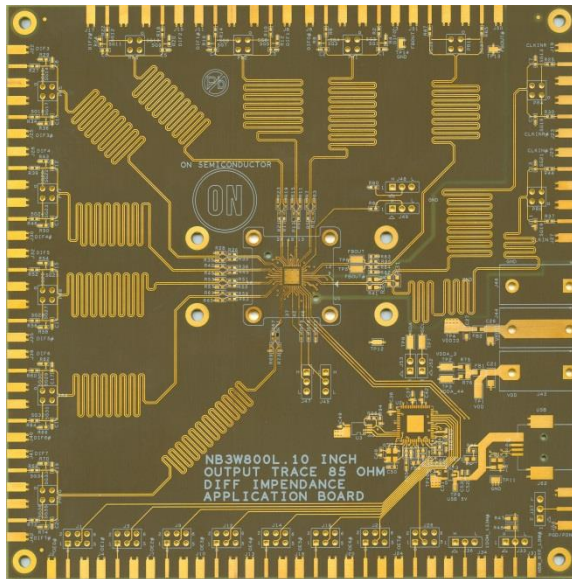
Introduction

The NB3W800LMNGEVB evaluation board was developed for the NB3W800L (HCSL-Compatible low power NMOS push pull Output). This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of the NB3W800L devices.

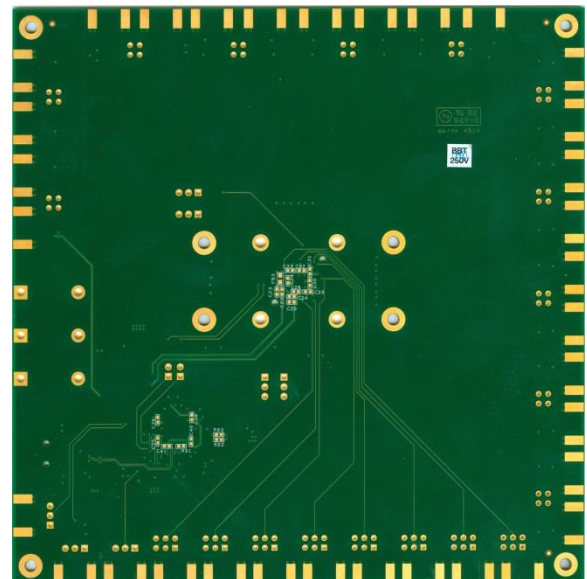
This evaluation board manual contains:

- Information on the NB3W800L Evaluation Board
- Assembly Instructions
- Test and Measurement Setup Procedures
- Board Schematic and Bill of Materials

This manual should be used in conjunction with the device datasheet which contains full technical details on the device specifications and operation.



Top View



Bottom View

Board Features

One Board Design/Layout:

- Accommodates the electrical characterization of the NB3W800L (Low power NMOS Push pull outputs)
- Accommodates a custom QFN-48 pogo-pin socket for lab evaluation, or a soldered down QFN-48 package.
- Incorporates on board SDI I2C/SMBus interface circuitry; powered from a USB connection, minimizing cabling.
- Convenient and compact board layout
- 3.3V power supply device operation
- Differential inputs and output signals are accessed via SMA connectors or high impedance probes

The evaluation board is with 10” output traces, with 85-Ω differential trace impedance.

All Inputs & Outputs have signal access via side-launch SMA connectors, installed, except SDA and SCL.

- SDA and SCL can be externally accessed by means of jumper headers & “test-point” anvils (for use with mini-grabber cables)

Each control pin can be managed directly through an SMA connector or manually with a H/L jumper header; H = VCC, L = DUTGND.

Other Board Features

There are no vias on the differential I/O metal traces so as to eliminate via impedance and stub effects on the high-speed I/Os.

This board accommodates a custom QFN-48 socket for lab evaluation, so there is a socket keep-out area.

Stand-offs are installed.

Board Layout

The NB3W800L QFN-48 Evaluation Board provides a high bandwidth, 43-Ω controlled impedance environment and is implemented in four layers.

All layers are constructed with FR4 dielectric material.

The first layer is the primary signal layer, including all of the differential inputs and outputs.

The second layer is the ground plane. It is dedicated for the SMA connector ground plane and for DUT ground.

The third layer is dedicated as the power plane. A portion of this 3rd layer is designated for the device VDD and VDDIO power planes.

The fourth layer contains control lines, power supply banana jacks and device power pin bypass capacitors.

Layer Stack

L1 (top) Signal (FR4)

L2 DUTGND (device ground) and SMA Ground, SMAGND

L3 VDD, VDDIO (separate device power supplies)

L4 (bottom), power supply by-pass capacitors, control pin traces and banana jacks

Power Supplies

Each VDD, VDDIO and GND power supply have a separate side-launch banana jack

Board Layer #2 = SMAGND = DUTGND = 0V.

GND Banana Jack = negative power supply for DUTGND and SMAGND.

Exposed Pad (EP): The exposed pad footprint on the board is mechanically connected (soldered) to the exposed pad of the QFN-48 package, and is electrically connected to DUTGND power supply, the negative supply of the device.

Board Layer #3 = VDDx Power Supplies

VDD = positive power supply for VDDA (pins #3, 44)

VDDIO = positive power supply for VDDIO (pins #10, 15, 19, 27, 34, 38, 42)

VDD & VDDIO have the power supply filtering per datasheet, and the bypass caps are located on top, by the banana jacks.

All VDD/VDDA /VDDIO device pins have 0.1uF bypass caps installed on bottom side of package pins.

Board is capable of measuring device IDD & IDDIO.

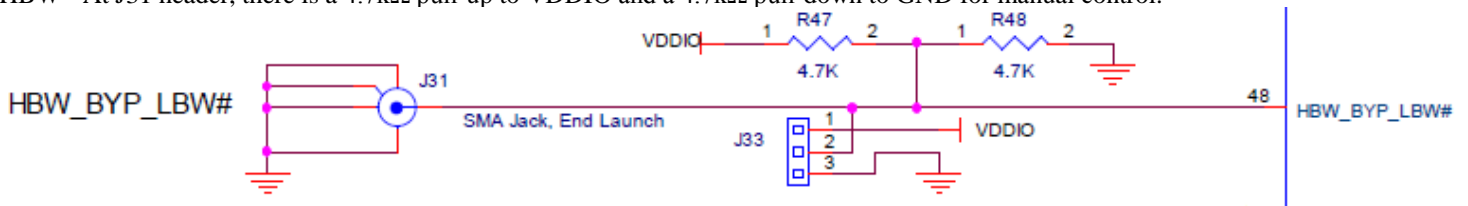
Control Pins

Each control pin can be managed directly through an SMA connector or manually with a H/L jumper header;

Tri-Level Input Pins - HBW_BYP_LBW#

On the 85ohm, 10inch output trace boards, the tri level input pin, HBW, has a 4.7kohm pull up to VDD and a 4.7kohm pull down to GND resistors; defaults to midlevel. Need to jumper for a High or jumper for a Low.

HBW - At J31 header, there is a 4.7kΩ pull-up to VDDIO and a 4.7kΩ pull-down to GND for manual control.



OE# Pins (Output Enable/Disable Function)

There are eight OE# pins available to control differential outputs

DIF0/0# to DIF7/7#. All of the OE#s can be controlled individually:

- 1) externally via the SMA connector for evaluation purposes, no jumper installed on OE#.
- 2) automatically by GUI control when jumper is installed on OE# in middle header.
- 3) manually with the convenient High/Low OE# jumper headers.

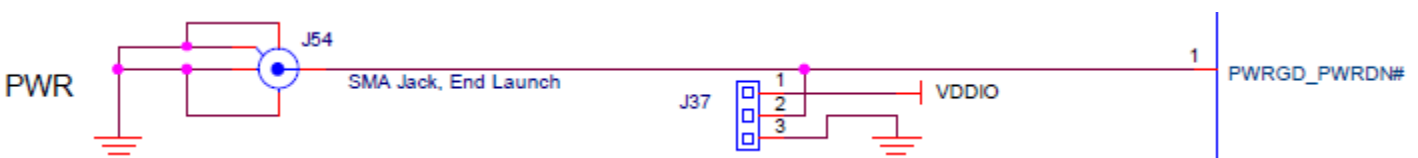
100M_133M# - Frequency Selection

The 100M_133M# frequency selection pin can be controlled manually with the High/Low header jumper (J34) at the SMA or externally with a control signal through the SMA connector; H = 100MHz, L = 133MHz.



PWRGD/PWRDN

The PWRGD/PWRDN pin can be controlled manually with the High/Low header jumper (J54) at the SMA connector or externally with a control signal through the SMA connector; H = PWRGD, L = PWRDN.



Differential Clock Inputs and Outputs

Differential Inputs - CLK_IN & CLK_IN#

The differential Clock input traces, CLK_IN/CLK_IN#, are routed from the SMA connectors on the right side directly to the DUT; there are no vias on metal traces.

CLK_IN & CLK_IN# have resistor pads (R40 & R41) to GND just outside the keep-out area of the socket to terminate a signal generator, if used. 50-ohm resistors are installed. **Remove these resistors** if CLK_IN & CLK_IN# are driven by another IC device.

Differential Outputs - DIFx and DIFx#

All eight differential output metal traces are designed to have equal length from the device under test (DUT) pins to the SMA connectors. These outputs have 43-ohm trace impedance (FR4), 85-ohm line-to-line.

All of the outputs have SMA connectors installed; there are no vias on the metal traces.

Each DIFx output has a provision for C_{Load} at the SMA; **2pF capacitors are installed on all outputs.**

R_s & R_p – Located close to DUT, just outside socket area.

43-ohm board - Installed with $R_s = 27\text{-}\Omega$ and $R_p =$ not installed.

HCSL outputs are typically terminated with 50- Ω to ground. This can be easily accomplished by connecting the HCSL outputs to the 50- Ω internal impedance in the oscilloscope.

Series R provision at SMA

A 0-ohm series resistor is installed between the end of the transmission line and the SMA connector:

- For measuring HCSL outputs with a Hi-Z probe.
- For measuring HCSL outputs with a 50- Ω scope head.

Hi-Z Probe Use

- 1) Single-ended Hi-Z probes or,
- 2) Differential Hi-Z probe; (see layout below)

A “solder gap” is employed at each output SMA connector.

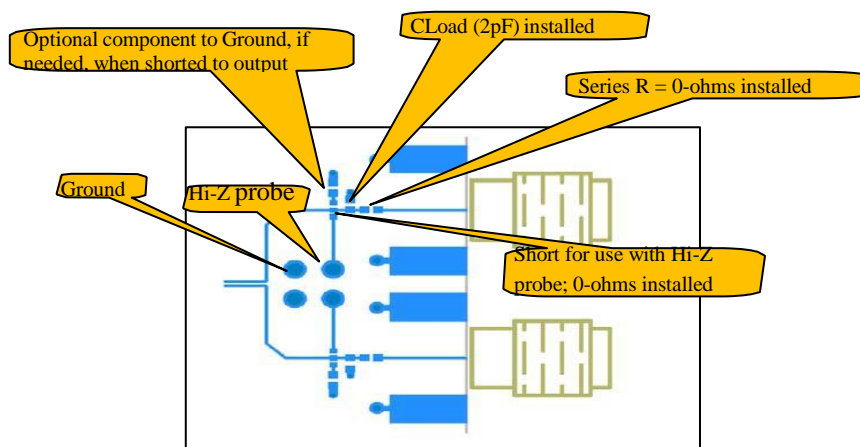
Short the gap with a solder blob or 0- Ω resistor to enable use of a Hi-Z probe. This solder gap is shorted with a 0-ohm resistor.

Holes for headers to connect to Hi-Z probes are available, but the header pins are not installed.

An optional component can be installed on each output. Additional capacitance loading can be accomplished with this board feature.

The NB3W800L EVB was designed with the flexibility to configure the board to measure the differential HCSL or low power NMOS Push Pull outputs with a 50-ohm scope head or High impedance FET probe.

The following figure describes the board's output features:



FB_OUT & FB_OUT# - External Feedback Termination

Since the FB_OUT & FB_OUT# pins do not drive transmission lines, the board layout has these pins loaded/terminated per datasheet;

These pins have series R pads, R82 & R83, to GND located close to the DUT, just outside the socket area.

USB & I2C / SMBus Interface

The NB3W800L EVB has an on-board I2C/SMBus interface circuitry located in the lower left section of the board.

This circuitry will interface with the program and the device via the SDA and SCL input pins, and can control the OE# pins, PLL Mode and Frequency Select directly from the GUI.

SCL & SDA- The SMBus Clock (SCL) and Data (SDA) pins are exercised through the on-board I2C interface.

In order to enable the I2C control of the DUT, **header jumpers J52 & J53 must be shorted.**

The I2C / SMBus interface circuitry is powered separately from the USB type-B connection and is isolated from device VDD and VDDIO. The USB GND is connected to DUTGND.

“Test-point anvils” TP7 & TP8 are available for external control of the device’s SCL and SDA pins by another off-board programmer, allowing other SMBus emulators to be used to program the DUT. If used, remove both jumpers J52 & J53.

NB3W800L Evaluation Board **Quick Start Lab Set-Up User’s Guide**

Pre Power Up

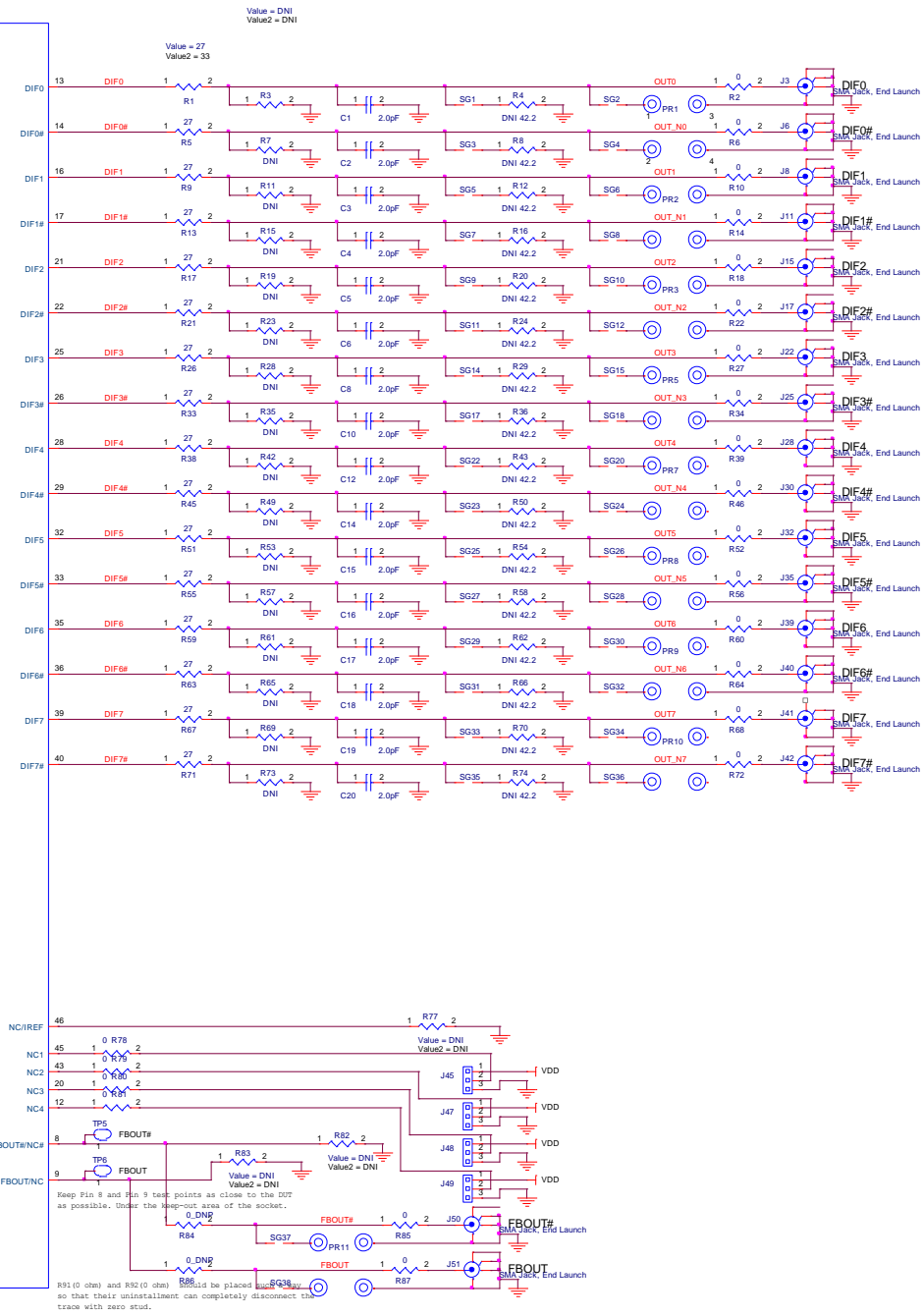
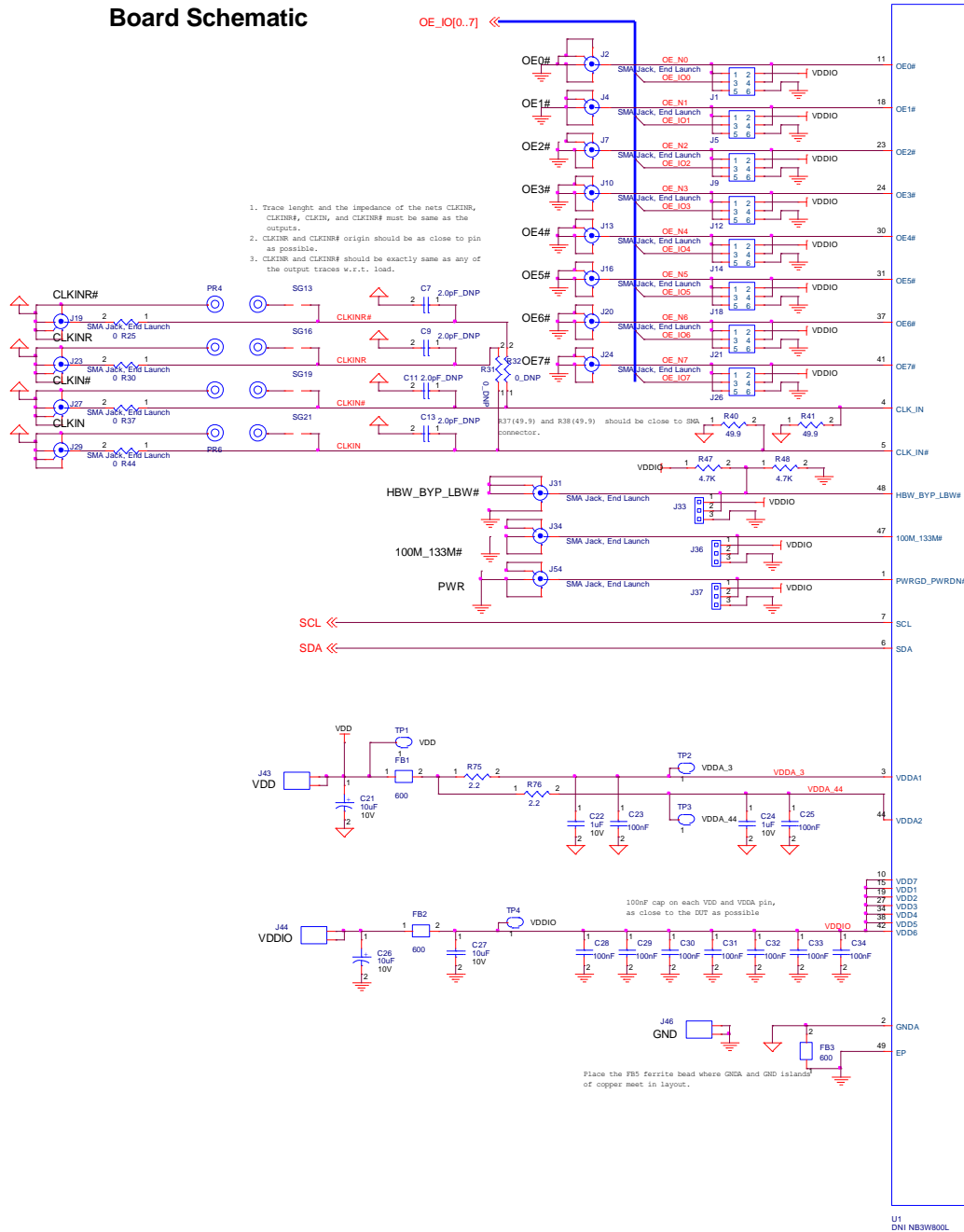
- 1) Connect power supply cables to VDD, VDDIO and DUTGND banana jacks; (do not turn power on, yet)
- 2) Connect a signal generator to the SMA connectors for the CLK_IN & CLK_IN# inputs, pins 4 and 5. 50-ohm termination resistors are installed for a signal generator on the board. Set-up appropriate input signal levels according to the device data sheet.
- 3) Ensure the PWRGD/PWRDN# pin (Pin #1) is in the Low state before power up (PWRDN#). There is a jumper (J37) on pin 1 to easily select between High and Low.
- 4) The 100M_133M# and HBW_BYP_LBW pins need to be hardware selected with jumpers J36 and J33 respectively.

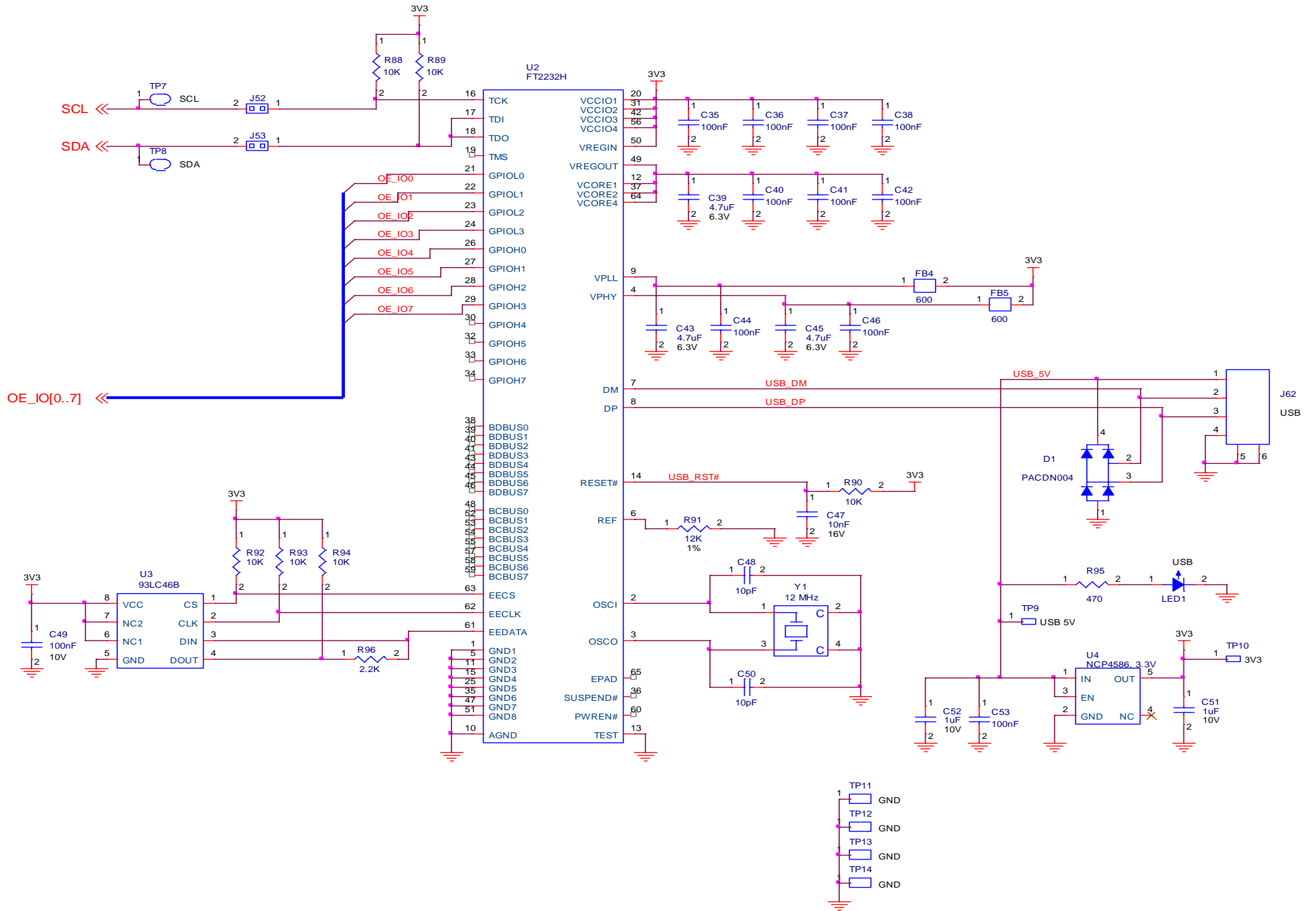
Power Up Sequence

- 1) Turn on power supply, 3.3V (VDD & VDDIO)
- 2) Move PWRGD/PWRDN# jumper to logic High, PWRGD
- 3) Turn on the Differential Clock Signal for the CLK_IN inputs (HCSL input, VIL = 0V, VIH = 700mV, Frequency based on J36 selection to 100MHz or 133MHz)
- 4) Monitor DIF_x/DIF_x# outputs on oscilloscope

Board Schematic

- Trace length and the impedance of the nets CLKIN#, CLKINR#, CLKIN, and CLKIN# must be same as the outputs.
- CLKIN# and CLKIN# origin should be as close to pin as possible.
- CLKIN# and CLKIN# must be exactly same as any of the output traces w.r.t. load.





Bill Of Materials

NB3W800L 85 Ohms, 10" trace board

Item	Quantity	Part Number	Reference	Part	PCB Footprint	Vendor	Vendor PN	Mfr	Remarks
1	20	C1005C0G1H020C	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20	2.0pF	c0402	DigiKey	445-4863-1-ND	TDK	DNP C7, C9, C11, C13
2	2	TR3A106K010C2000	C21,C26	10uF	c1206	DigiKey	718-1300-1-ND	Vishay	
3	4	GRM155R61A105ME15D	C22,C24,C51,C52	1uF	c0402	DigiKey	490-5409-1-ND	Murata	
4	20	0402ZD104KAT2A	C23,C25,C28,C29,C30,C31, C32,C33,C34,C35,C36,C37, C38,C40,C41,C42,C44,C46, C49,C53	100nF	c0402	DigiKey	478-1129-1-ND	AVX	
5	1	C1608X5R1A106M	C27	10uF	c0603	DigiKey	445-6853-1-ND	TDK	
6	3	C1005X5R0J475M	C39,C43,C45	4.7uF	C0402	DigiKey	445-7395-1-ND	TDK	
7	1	0402YC103KAT2A	C47	10nF	C0402	DigiKey	478-1114-1-ND	AVX	
8	2	GRM1555C1H100JZ01D	C48,C50	10pF	C0402	DigiKey	490-1278-1-ND	Murata	
9	1	PACDN004SR	D1	PACDN004	sot_143	Mouser	748-PACDN004SR	ON Semi	
10	3	BLM18KG601SN1D	FB1,FB2,FB3	600	L0603	DigiKey	490-5258-1-ND	Murata	
11	2	BLM15AG601SN1D	FB4,FB5	600	L0402	DigiKey	490-1006-1-ND	Murata	
12	8	67996-206HLF	J1,J5,J9,J12,J14,J18,J21, J26	Header 2x3 Thru-Hole	berg_2x3_2p54	DigiKey	609-3210-ND	FCI	
13	33	142-0701-801	J2,J3,J4,J6,J7,J8,J10, J11,J13,J15,J16,J17,J19, J20,J22,J23,J24,J25,J27, J28,J29,J30,J31,J32,J34, J35,J39,J40,J41,J42,J50, J51,J54	SMA Jack, End Launch	sma_jack_end_launch	Digikey	J502-ND	Johnson Components	
14	7	961103-6404-AR	J33,J36,J37,J45,J47,J48, J49	Header 3-pin	hdr_1x3_2p54	DigiKey	3M9448-ND	3M	
15	1	571-0500	J43	Banana Jack, Thru-Hole, Red	con_571-0500	Mouser	164-6219	Deltron	
16	1	571-0700	J44	Banana Jack, Thru-Hole, Yellow	con_571-0500	Mouser	164-7170	Deltron	
17	1	571-0100	J46	Banana Jack, Thru-Hole, Black	con_571-0500	Mouser	164-6218	Deltron	
18	2	961102-6404-AR	J52,J53	Header 2-pin	hdr_1x2_2p54	DigiKEY	3M9447-ND	3M	
19	1	USB-B1SMHSW6	J62	Conn, USB-B, SMT	con_usb_b_ra	DigiKey	ED2994-ND	On Shore Technology	
20	1	LTST-C190KGKT	LED1	LED, Green	led_0603	DigiKey	160-1435-1-ND	Lite-On	
21	11	No Part	PR1,PR2,PR3,PR4,PR5,PR6, PR7,PR8,PR9,PR10,PR11	4 Round Pads, .060 with .040 Hole	berg_2x2_2p54				
22	16	ERJ-2GEJ270X	R1,R5,R9,R13,R17,R21,R26, R33,R38,R45,R51,R55,R59, R63,R67,R71	27	r0402	DigiKey	P27JCT-ND	Panasonic	
23	27	CRCW04020000Z0ED	R2,R6,R10,R14,R18,R22, R25,R27,R30,R34,R37,R39, R44,R46,R56,R60,R64,R68, R72,R78,R79,R80,R81,R84, R85,R86,R87	0	r0402	DigiKey	541-0.0JCT-ND	Vishay	DNP R78, R79, R80, R81, R84, R86
24	19	ERJ-2RKF42R2X	R3,R7,R11,R15,R19,R23, R28,R35,R42,R49,R53,R57, R61,R65,R69,R73,R77,R82, R83	DNI	r0402	DigiKey	P42.2LCT-ND	Panasonic	
25	16	ERJ-2RKF42R2X	R4,R8,R12,R16,R20,R24,	DNI 42.2	r0402	DigiKey	P42.2LCT-ND	Panasonic	

			R29,R36,R43,R50,R54,R58, R62,R66,R70,R74						
26	2	CRCW06030000Z0EA	R31,R32	0	r0603	DigiKey	541-0.0JCT-ND	Vishay	DNP R31, R32
27	2	ERJ-3EKF49R9V	R40,R41	49.9	r0603	DigiKey	P49.9HCT-ND	Panasonic	
28	2	ERJ-3GEYJ472V	R47,R48	4.7K	r0603	DigiKey	P4.7KGCT-ND	Panasonic	
29	1	CRCW04020000Z0ED	R52	0	r0402	DigiKey	541-0.0JCT-ND	Vishay	
30	2	ERJ-3GEYJ2R2V	R75,R76	2.2	r0603	DigiKey	P2.2GCT-ND	Panasonic	
31	6	ERJ-2GEJ103X	R88,R89,R90,R92,R93,R94	10K	r0402	DigiKey	P10KJCT-ND	Panasonic	
32	1	ERJ-2RKF1202X	R91	12K	r0402	DigiKey	P12.0KLCT-ND	Panasonic	
33	1	ERJ-2GEJ471X	R95	470	r0402	DigiKey	P470JCT-ND	Panasonic	
34	1	ERJ-2GEJ222X	R96	2.2K	r0402	DigiKey	P2.2KJCT-ND	Panasonic	
35	38	No Part	SG1,SG2,SG3,SG4,SG5,SG6,	Solder Gap	r0201				
			SG7,SG8,SG9,SG10,SG11,						
			SG12,SG13,SG14,SG15,SG16,						
			SG17,SG18,SG19,SG20,SG21,						
			SG22,SG23,SG24,SG25,SG26,						
			SG27,SG28,SG29,SG30,SG31,						
			SG32,SG33,SG34,SG35,SG36,						
SG37,SG38									
36	8	5015	TP1,TP2,TP3,TP4,TP5,TP6, TP7,TP8	Test Point, SMT	tp_70_135	DigiKey	5015KCT-ND	Keystone	
37	2	No Part	TP9,TP10	Test Pad 30 x 60 mil	tp_30_60				
38	4	No Part	TP11,TP12,TP13,TP14	Test Pad 50 x 100 mil	tp_50_100				
39	1	DNI NB3W800L	U1	DNI NB3W800L	MODULE_48QFN_0P40	On Semi	-	ON Semi	
40	1	FT2232HQ-REEL	U2	FT2232H	qfn_64_0p5	DigiKey	768-1025-1-ND	FTDI	
41	1	93LC46BT-I/ST	U3	93LC46B	tssop_8_4p4w_0p65	DigiKey	93LC46BT-I/STCT-ND	Microchip	
42	1	NCP4586DSN33T1G	U4	NCP4586, 3.3V	sot23_5p	ON Semi	NCP4586DSN33T1G	ON Semi	
43	1	ABM8G-12.000MHZ-4Y-T3	Y1	12 MHz	CRY-4P-SMD1	DigiKey	535-10901-1-ND	Abracon Corp	