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# NCL30488LED1GEVB

## NCL30488LED1

### 60 W High Power Factor LED Driver Evaluation Board

### User's Manual

#### Evaluation Board Overview

This manual covers the specification, construction, and testing of the NCL30488 demonstration board. This board is configured as a 60 W high PF flyback LED driver for LED lighting.

#### The Key Features of this Demo Board

- PSR (Primary Side Regulation)
- Low THDi
- High Power Factor
- CC/CV Modes
- Quasi-Resonant Operation
- Valley Count Frequency Foldback
- High Line Valley Skip
- Brown Out/In
- Line Feedforward Compensation
- Current Limit Protection
- Output Over Voltage Protection
- Open/Short Pin Protection



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#### Specifications

Input Voltage	100 – 277	V ac
Line Frequency	50/60	Hz
THDi (>20% Load)	20%	Max.
Power Factor (>75% Load)	0.9	Min.
Output Voltage	40	V dc
Output Current	1.5	A dc
Efficiency	90%	Max
Ripple	< 50%	Pk - Pk
Startup Time	< 200	ms

## Controller Pin Descriptions

### COMP Pin

#### *Primary Control*

The OTA error amplifier output is available on this pin. A Type 2 compensation network connected between this pin and ground controls loop bandwidth for constant voltage (CV) control. Voltage on the COMP pin is discharged to zero when Vcc is below reset level.

#### *Secondary Control*

The COMP pin supports optional secondary side control. The collector of an opto-coupler connects here allowing a secondary side feedback control function providing tighter output regulation of voltage and/or current. Optional programming provides a pull-up resistor, disabled OTA error amplifier, and disabled boost current source.

### ZCD Pin

#### *Demagnetization Function*

The power magnetic is monitored through an auxiliary winding connected to this pin. Core demagnetization is detected and processed by the valley count control before issuing a DRV pulse starting the next switching cycle. This processing insures quasi-resonant operation which minimizes losses by initiating the next switching cycle near a minimum drain voltage.

#### *Shorted Output Detection*

Should the ZCD voltage remain at or below 0.65 volts for 90 ms, it is assumed the converter output is shorted. The controller will cease drive pulses for 4 seconds allowing a cooling period before automatically restarting.

#### *Voltage Monitoring*

Auxiliary winding voltage is monitored as part of CV regulation control. Voltage is sensed after a blanking time and processed for CV regulation. Voltage regulation threshold is 3.50 volts. Actual output voltage is determined by the transformer turns ratio and the resistor divider network between the ZCD pin and auxiliary winding.

It can be seen that the ZCD voltage is limited to a range of 0.65 volts (shorted output) to 3.50 volts (regulation threshold) resulting in an output voltage control range of 5.38:1. Thresholds should be carefully matched to LED voltage to avoid unintentionally limiting constant current (CC) output level by entering CV mode, especially at low temperatures. However, the CV mode can be used to limit output power if needed.

#### *Over Voltage Protection*

If the aux winding voltage exceeds the Slow OVP threshold (115% nominal) for 4 consecutive cycles, DRV pulses are suspended for 1.5 ms. After this delay, a DRV pulse is issued to check output voltage. The cycle repeats until the aux winding voltage is below Slow OVP threshold. Note that at very light loads, the test pulse can cause the output voltage to increase.

If the aux winding voltage exceeds the Fast OVP threshold (130% nominal) for 4 consecutive cycles, or 2 cycles if Slow OVP is already active, DRV pulses are suspended for 4 seconds. After this time, DRV pulses resume.

## **CS Pin**

### *Current Mode Control*

MOSFET current information enters through this pin. The control algorithm uses this current information to compute output current. The overcurrent protection threshold is 1.38 volts with a 330 ns blanking period. When the threshold is reached, the switching cycle is terminated. The next cycle will start when ZCD conditions are met. In case of extreme faults a higher threshold of 1.99 volts with 170 ns blanking will initiate a 4 second shutdown after 4 consecutive pulses. Recovery is automatic.

### *CS Short Detection*

When Vcc bias power is first applied, the controller delivers 500  $\mu$ A out the pin and monitors the voltage on the CS Pin. If the voltage is below 60 mV, the controller assumes a shorted pin and will not issue DRV pulses. With tolerance, the minimum resistance in series with the CS pin is 225  $\Omega$ .

### *Line Feedforward*

The control algorithm accounts for many errors, such as leakage inductance, when computing the output current. Some error sources are variable with line voltage, such as the effect of delays in the power stage. As the input voltage increases, the power stage delays cause the peak current to slightly overshoot. While this is not usually a large increase in output current, the control can compensate for this by sourcing a current out of CS Pin which is proportional to the input voltage. This introduces a voltage drop across the series resistor between CS Pin and MOSFET current sense resistor. The voltage drop reduces the target peak current slightly such that the effect of the delay is cancelled and regulation is improved. The

optimal value for the series resistance is a trial and error process, bearing in mind the previously described minimum value. Note that any impedance between DRV pin and the gate of the switching MOSFET will affect regulation.

## **GND**

This is the ground or return reference pin for the controller. Use good PCB layout practices to ensure switching currents do not degrade control signals.

## **DRV Pin**

The DRV pin connects to the gate of the MOSFET. A direct connection to the gate is recommended for optimal primary side regulation. If necessary, switching times can be modified via a collection of resistors and diodes for EMI considerations.

## **Vcc Pin**

This pin receives the bias power for the controller. The internal HV Startup provides initial charge to the Vcc capacitor. After the converter is operational, an external source provides bias power. Typically, the ZCD winding is dimensioned to also supply bias power.

Proper bypassing is required for the Vcc Pin. Place sufficient capacitance to maintain operating voltage during DRV Pin sourcing. A good quality electrolytic capacitor is typically sufficient, however some applications may require a 100 nF ceramic capacitor as well. 10  $\mu$ F is a good first choice. Excessive capacitance or external loads will increase stress on the HV startup current source.

Over Voltage Protection is included on Vcc Pin. Typical OVP threshold is 26.5 Vdc. Ensure the external bias does not exceed the minimum

OVP threshold of 25 Vdc to avoid activating the protection feature. A voltage regulator can be used for applications requiring wide output voltage range since aux winding voltage follows output voltage and may exceed the OVP threshold.

### **HV Pin**

The High Voltage Pin provides three essential functions: start up current, input line reference, and line range selection. It is recommended that a resistance is placed in series with the rectified ac bus, and a capacitor is connected to return. The corner frequency of this RC filter is between 12 kHz and 20 kHz to limit high frequency noise. Recommended resistance is 1 k $\Omega$  to 3.3 k $\Omega$ .

#### *HV Start*

An internal HV current source charges the Vcc capacitor when ac input is first applied. Initial current is limited to 300  $\mu$ A until Vcc exceeds 1 V. This prevents excessive dissipation in the event Vcc is shorted. Nominal charge current is 6.5 mA which is applied until V<sub>CC(on)</sub> is reached, typically 18 V.

After reaching V<sub>CC(on)</sub>, the HV current source is turned off, the controller is activated, and DRV pulses are issued. Bias power is derived from the Vcc capacitor until alternate bias power is available. Typically, the ZCD winding is configured as an Auxiliary source to supply bias power. If alternate power is not available, the controller will cease DRV pulses when Vcc falls below 8.8 V. At this point, the HV current source resumes charging the Vcc capacitor as another start up attempt is made.

#### *Rectified Line Sensing*

The rectified ac input supplies a reference for the Power Factor control loop. The signal is internally scaled and used to match input current to the input voltage thereby providing High Power factor and low Total Harmonic Distortion. Care should be taken in the design of the EMI input filter to not introduce excessive distortion or phase delay which could cause poor performance. It is essential the HV Pin voltage be a good representation of the rectified ac input voltage. In particular, the voltage must reduce to a low level at zero crossings.

The rectified ac input is also used for brown out detection. When the applied voltage exceeds a threshold, DRV pulses are enabled. Conversely, when the applied voltage falls below another lower threshold, DRV pulses are terminated. A 25 ms blanking time is used with brown out. Two ranges of brown out protection are available.

The controller has an optional input over voltage protection feature. If the rectified ac input exceeds 469 V dc nominal, DRV pulses are terminated. When voltage drops below 443 V dc for 25 ms, operation resumes.

#### *Line Range Selection*

The gain of the feedback loop is dynamically changed to provide optimum PF, THDi, and output regulation over a wide range of ac input voltage. An internal comparator monitors ac input voltage present on the HV Pin and changes the gain at a voltage which is not internationally used for commercial power. Transitioning through this input voltage band will appear as a disturbance in output power as

a one-time event. It is not indicative of a problem within the controller.

As previously mentioned in the CS Pin section, a current proportional to the ac input voltage is sourced out the CS Pin. This current introduces a voltage in the series resistor to compensate for delays which are related to ac input voltage. The basis for this current is the voltage monitored on the HV Pin.

## Setting Up the LED Driver

### Constant Current Control

The Primary Side Regulation control loop monitors the voltage presented on the CS Pin to maintain proper Constant Current output. This PSR control function eliminates the need for an opto-coupler and yet maintains tight load current regulation.

The parallel combination of R11 and R12 is  $R_{sense}$ . The term  $N_{sp}$  is the secondary to primary winding turns ratio of the transformer.  $V_{ref}$  is fixed at 1.00 volts. The formula below establishes the full output current regulation point in CC mode.

$$I_{out} = \frac{V_{REF}}{2N_{SP}R_{sense}}$$

Note that this calculation is independent of transformer inductance. In addition, leakage

inductance is compensated via the control algorithm. Best performance is obtained if capacitor C11 of the primary winding clamp is connected to the source of Q2.

### Constant Voltage Control

The Primary Side Regulation also includes a Constant Voltage mode. The Auxiliary winding voltage is scaled by resistor divider R6 & R7 and present to the ZCD pin. The voltage is sampled during the switch off-time after a blanking delay and used for CV feedback. The internal reference voltage is 3.50 V nominal. In other words, CV regulation point is determined by the output winding to Aux winding turns ratio and the resistor divider.

Care must be taken when setting the CV regulation point. LEDs have a negative temperature coefficient, which means the voltage drop will be higher at low temperature. Ensure the CV regulation voltage is higher than the maximum LED string voltage in order to maintain Constant Current operation. Note that it is possible to limit output power at low temperature by adjusting the CV regulation point within the expected LED string voltage at low temperature. Careful tolerance allowance is required in this case.

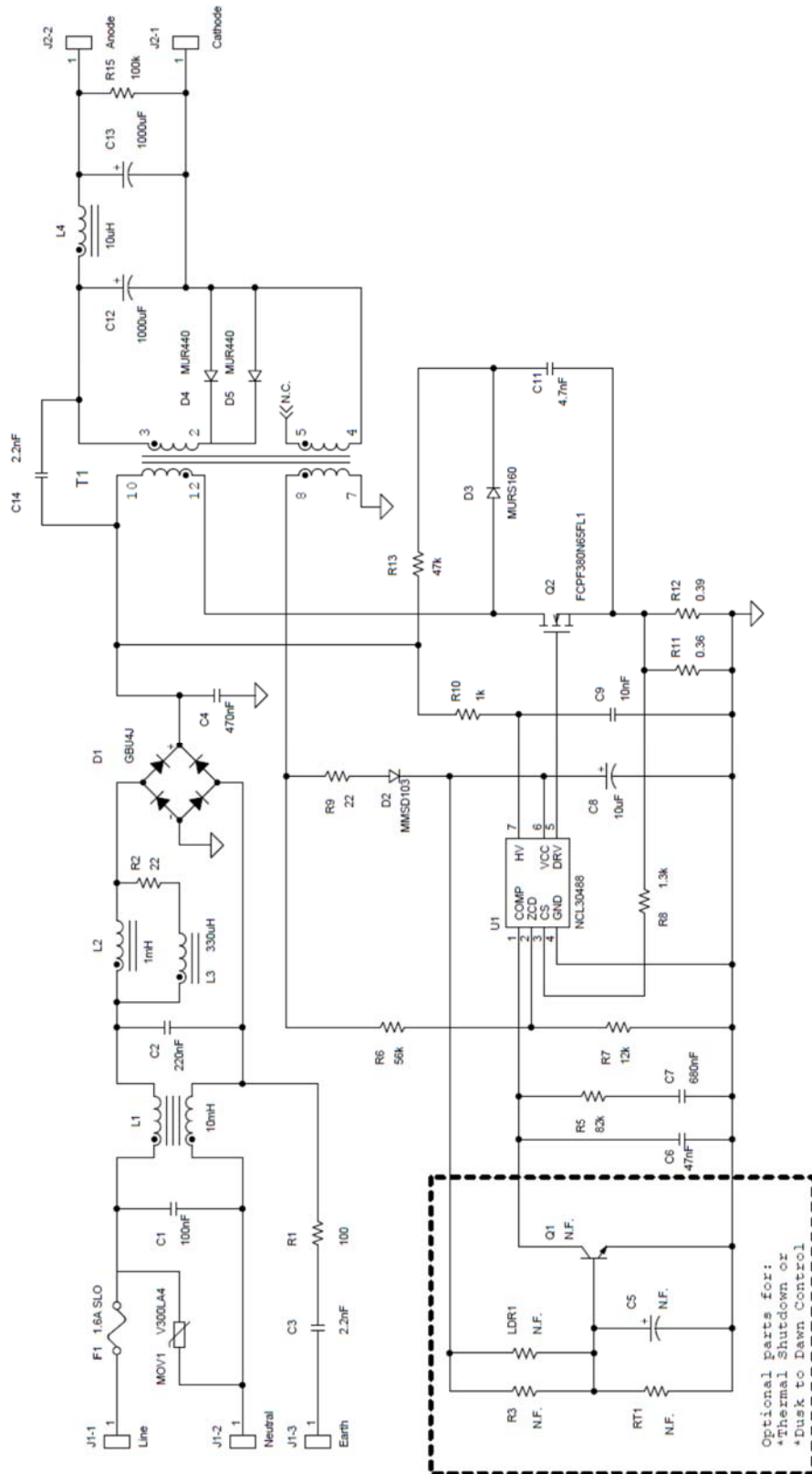


Figure 1. Schematic

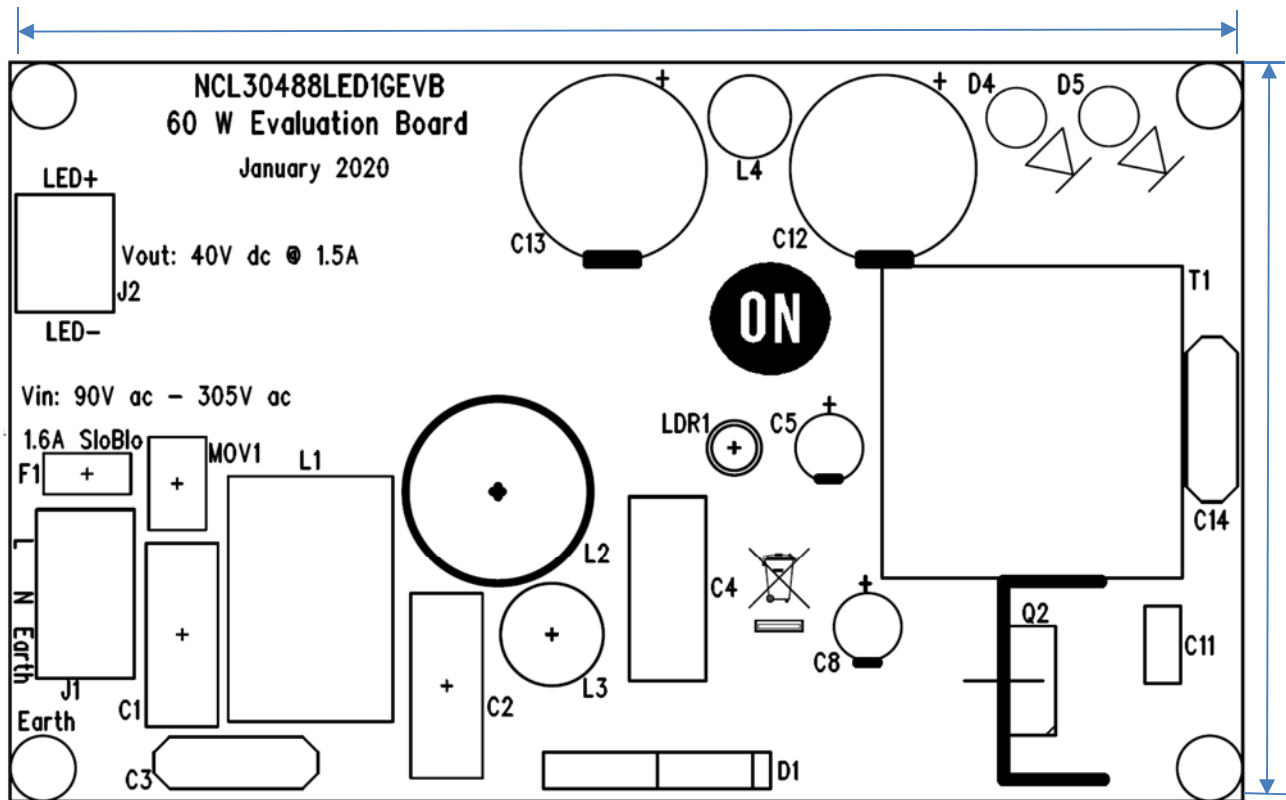


Figure 2. PCB Outline and Top Silkscreen (120mm x 72mm)

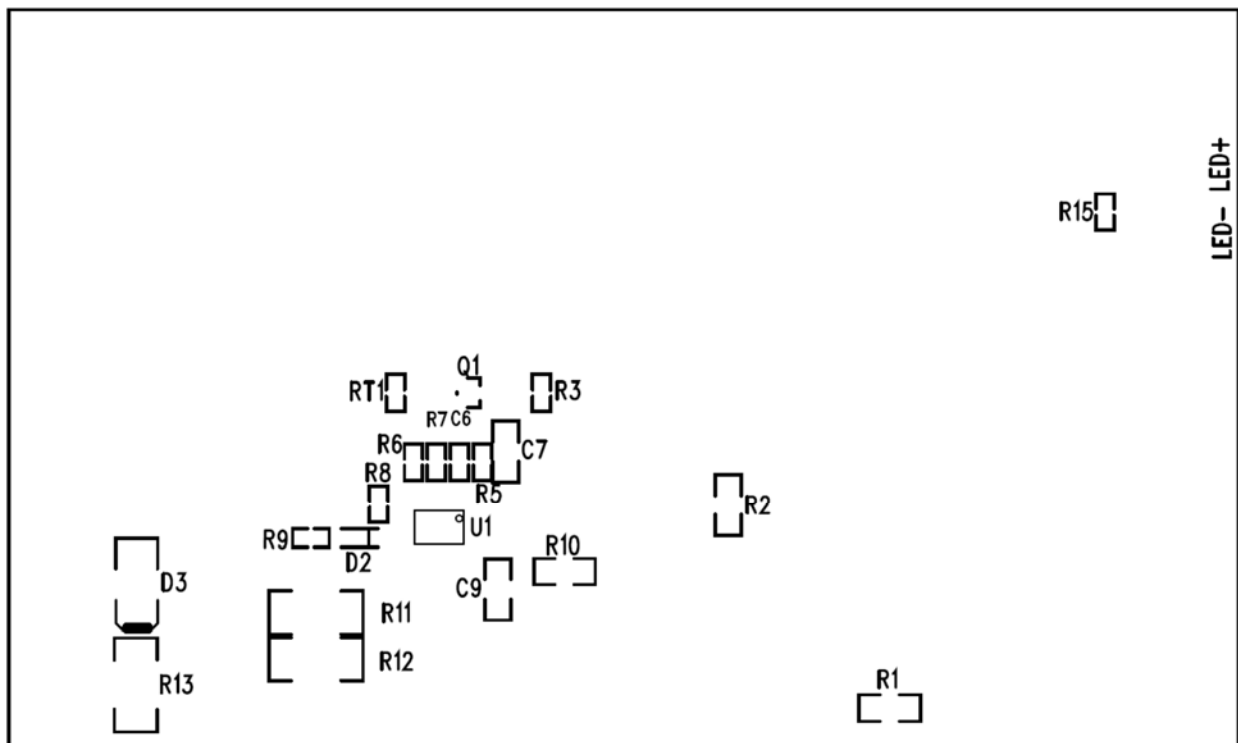


Figure 3. Bottom Silkscreen



## TEST PROCEDURE

### Required Equipment

- AC Source – 90 to 277 V ac 50/60 Hz, Minimum 100 W capability
- AC Wattmeter – 100 W Minimum, Power Factor measurement capability
- DC Voltmeter – 100 V dc Minimum, 0.1% accuracy
- DC Ammeter – 2 A dc Minimum, 0.1% accuracy
- LED Load – 35 V to 40 V dc, rated 1.5 A dc
- Resistor Load – 100  $\Omega$ , 30 W minimum

### Test Connections Per Figure 4

1. Connect AC power to the input of the wattmeter. Connect output of wattmeter to input connector J1 of UUT (Unit Under Test). Observe 'L' and 'N' connections. Connect J1 Earth to ground for safety.
2. Connect UUT output connector J2 'LED+' to DC ammeter. Connect other lead of DC ammeter to "+" of LED Load. Connect UUT output connector J2 'LED-' to "-" of LED Load. *Caution: Observe correct polarity or the load may be damaged.*
3. Connect DC voltmeter to UUT output connector J2 'LED+' and 'LED-'.

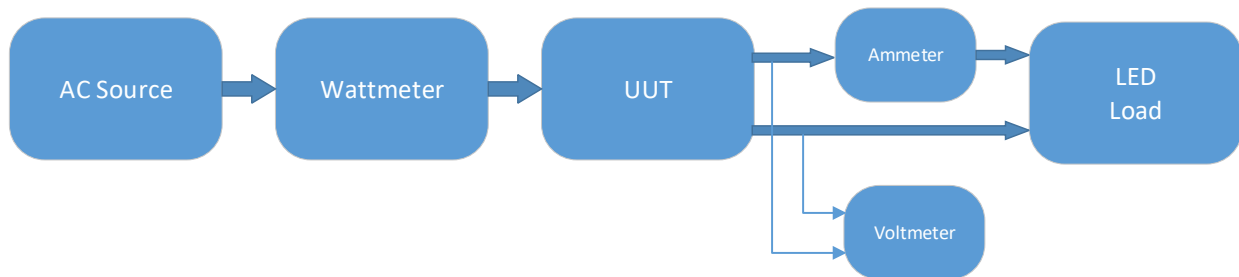


Figure 4. Test Setup

### Constant Current Regulation

1. Set the LED Load between 36 and 38 V dc
2. Set the AC Source as indicated in the chart below. **Caution: Do not touch the UUT once it is energized. Hazardous voltages are present.**
3. Enter 'P' or 'F' in column below depending on test result.
4. When test is completed, set AC Source to zero volts, Set DC Supply to zero volts

Input Vac	Input Power	Power Factor		Output Current			Output Voltage
		Reading	P/F (>0.9)	Reading	Limits	Pass/Fail	
90					1.42 – 1.58 A dc		
120					1.42 – 1.58 A dc		
230					1.42 – 1.58 A dc		
277					1.42 – 1.58 A dc		

### Constant Voltage Regulation

1. Remove the LED Load and replace with 100  $\Omega$  resistor
2. Set the AC Source as indicated in the chart below. **Caution: Do not touch the UUT once it is energized. Hazardous voltages are present.**
3. Enter 'P' or 'F' in column below depending on test result.
4. When test is completed, set AC Source to zero volts, Set DC Supply to zero volts

Input Vac	Output Voltage		
	Reading	Limits	Pass/Fail
120		37 – 41 V dc	
277		37 – 41 V dc	

Test Complete

### TYPICAL TEST DATA

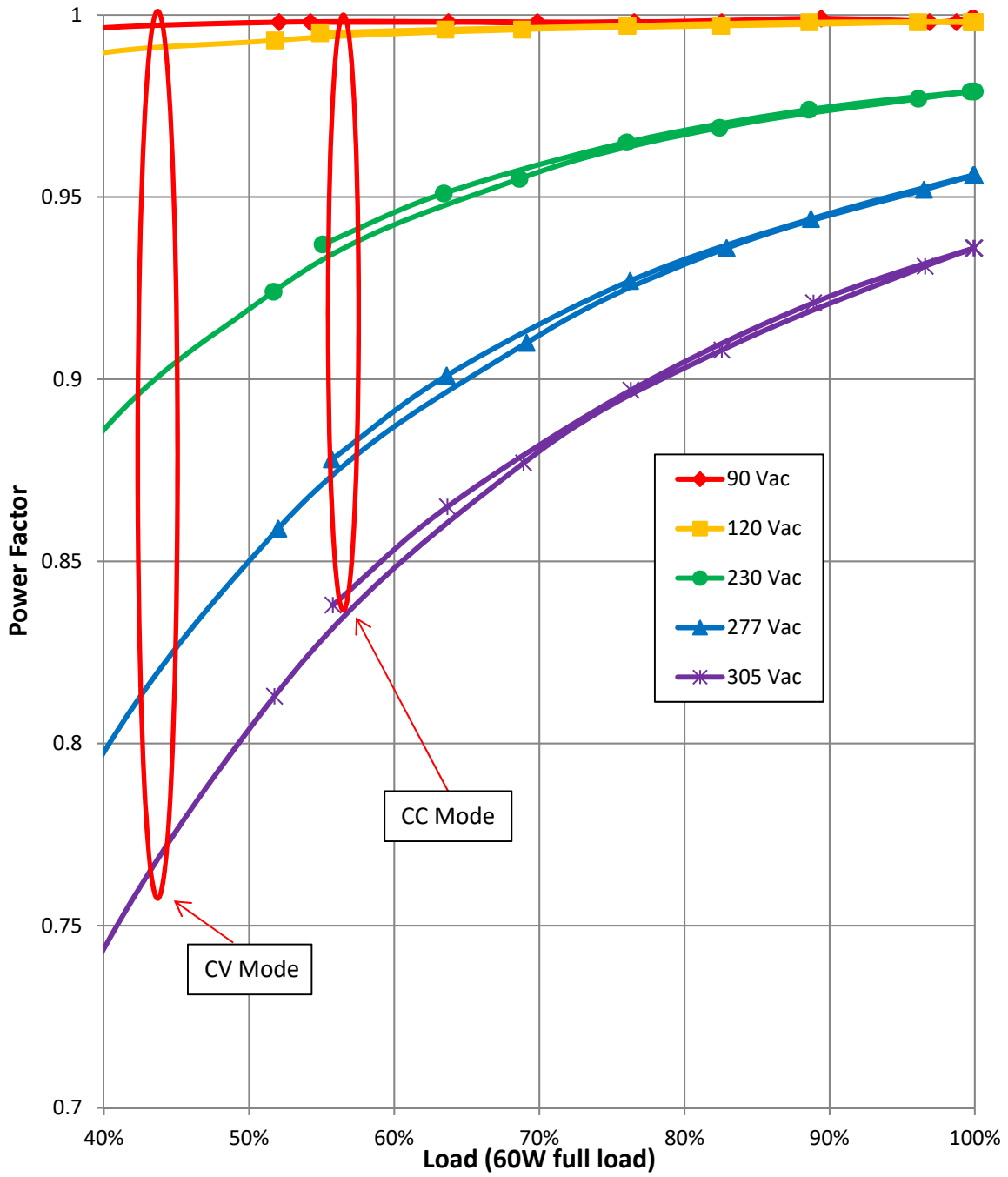


Figure 5. Power Factor Performance

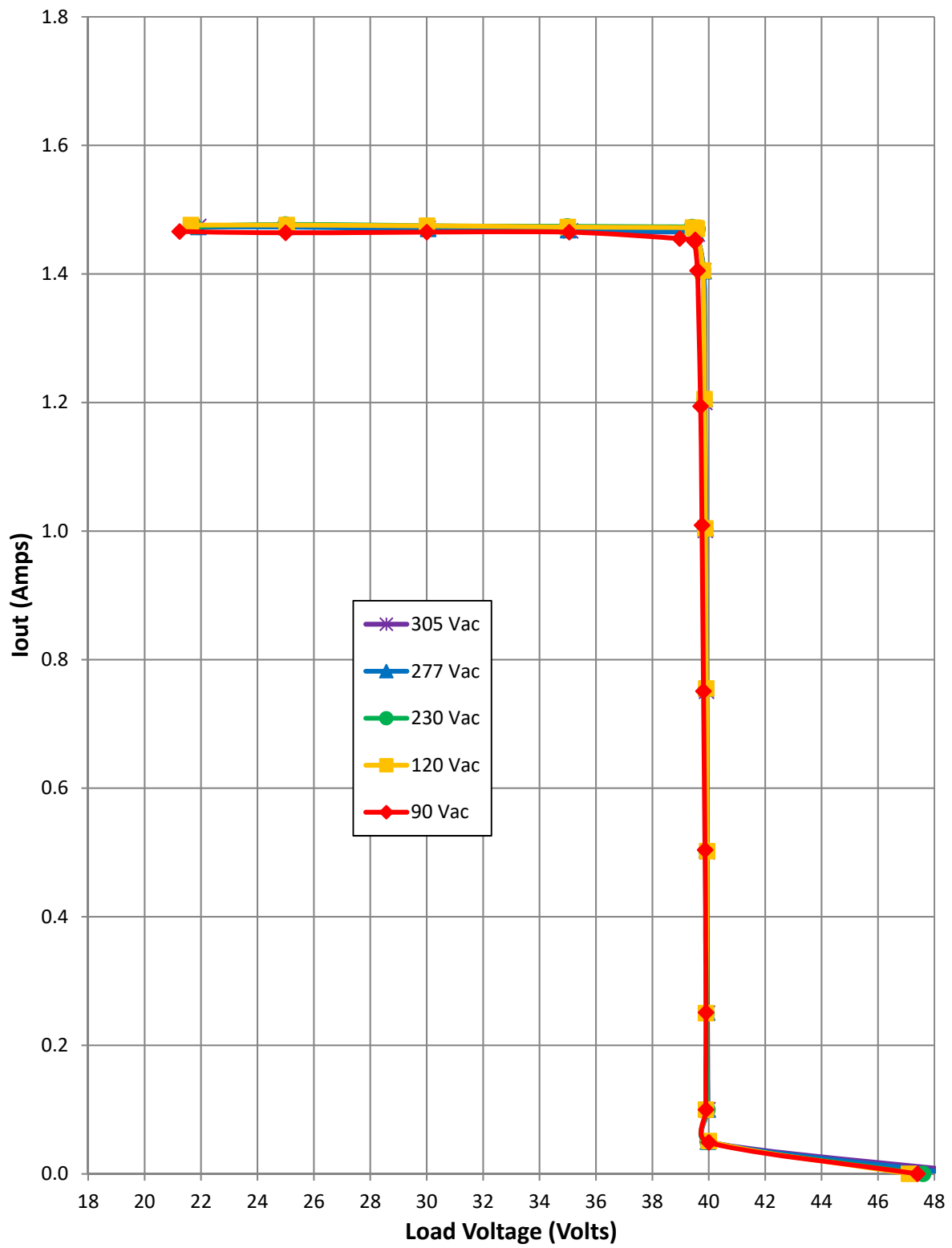


Figure 6. Line and Load Regulation Performance

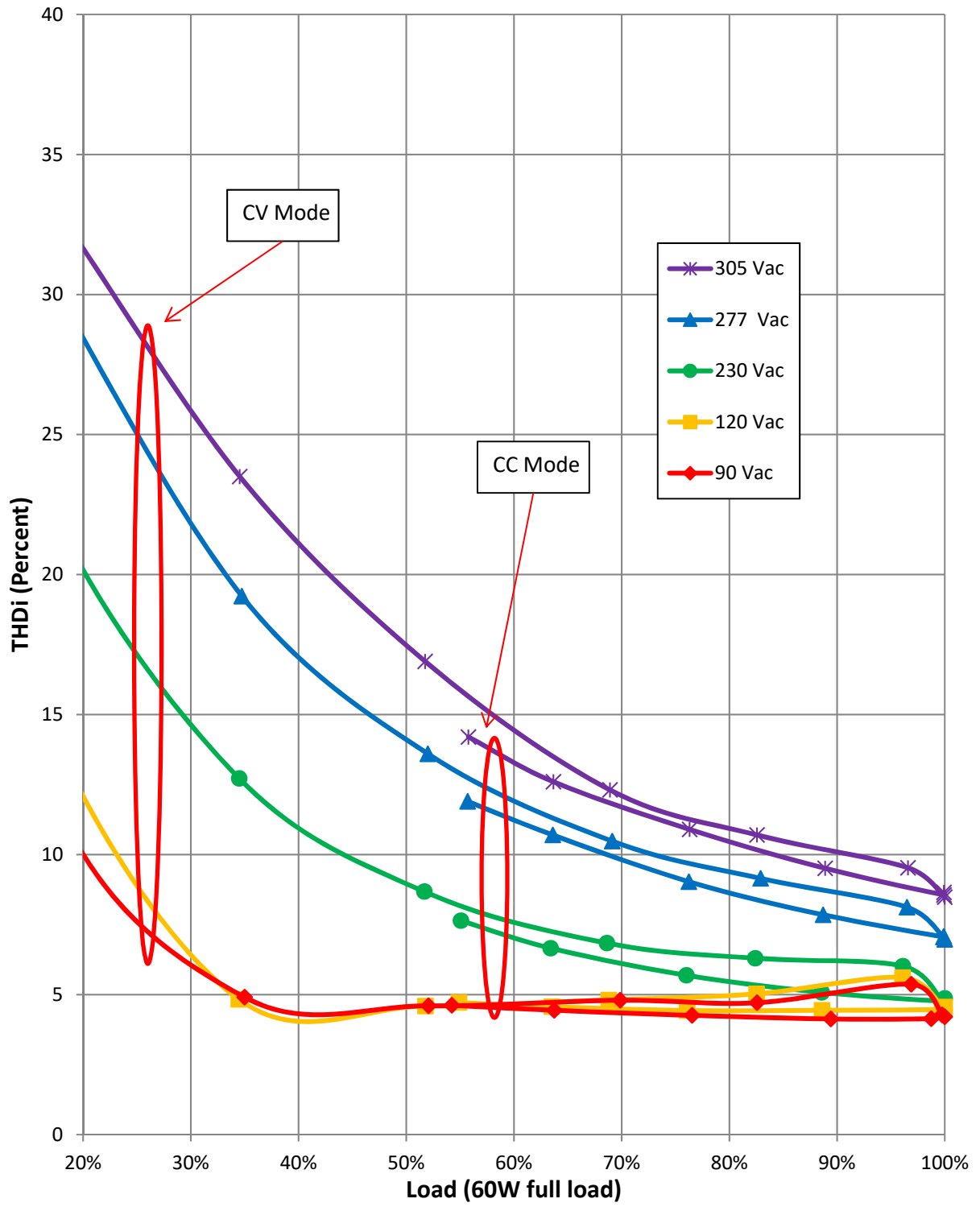


Figure 7. THDi Performance

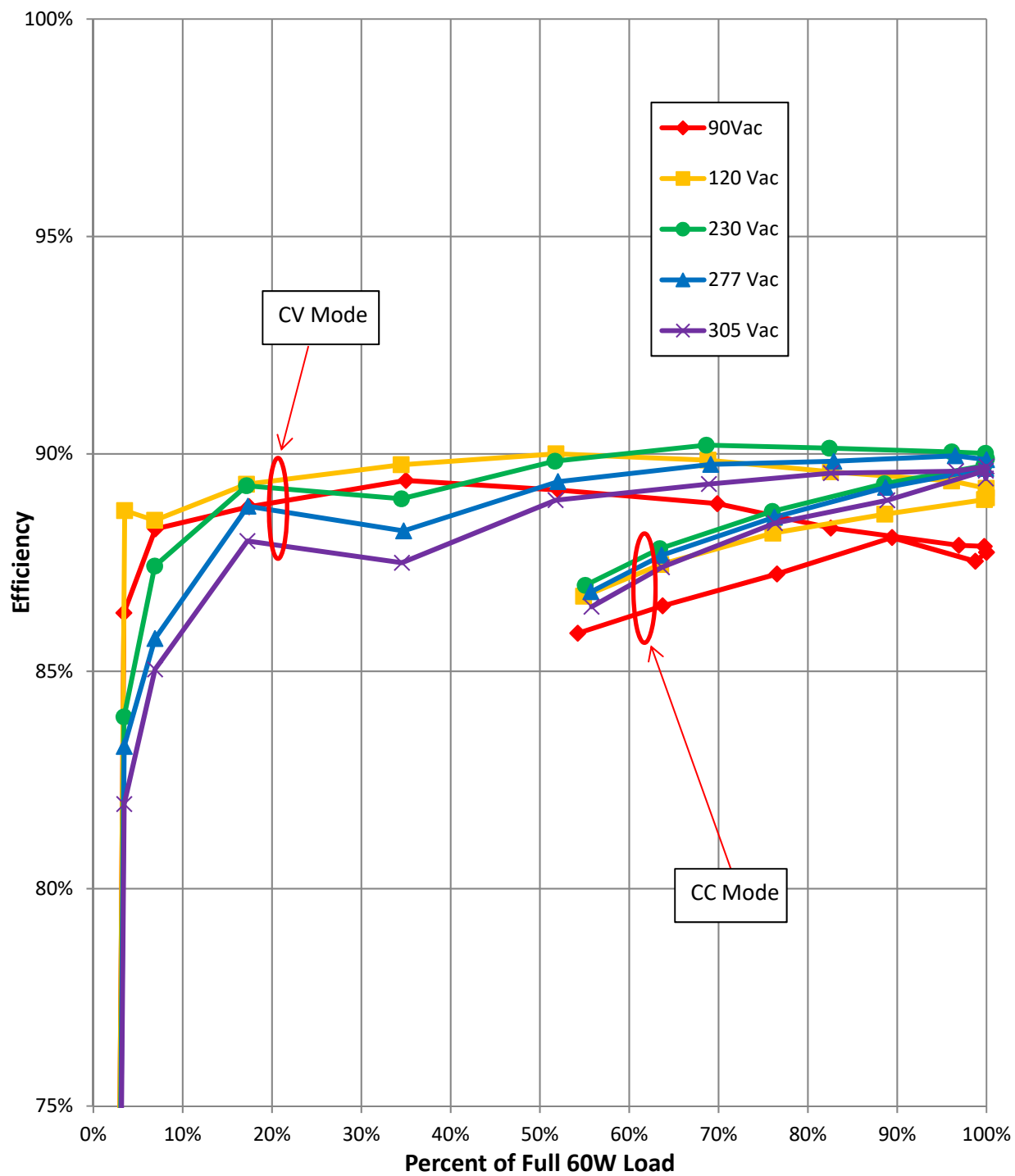


Figure 8. Efficiency



Figure 9. Full Load Start Up with 120 V ac Input

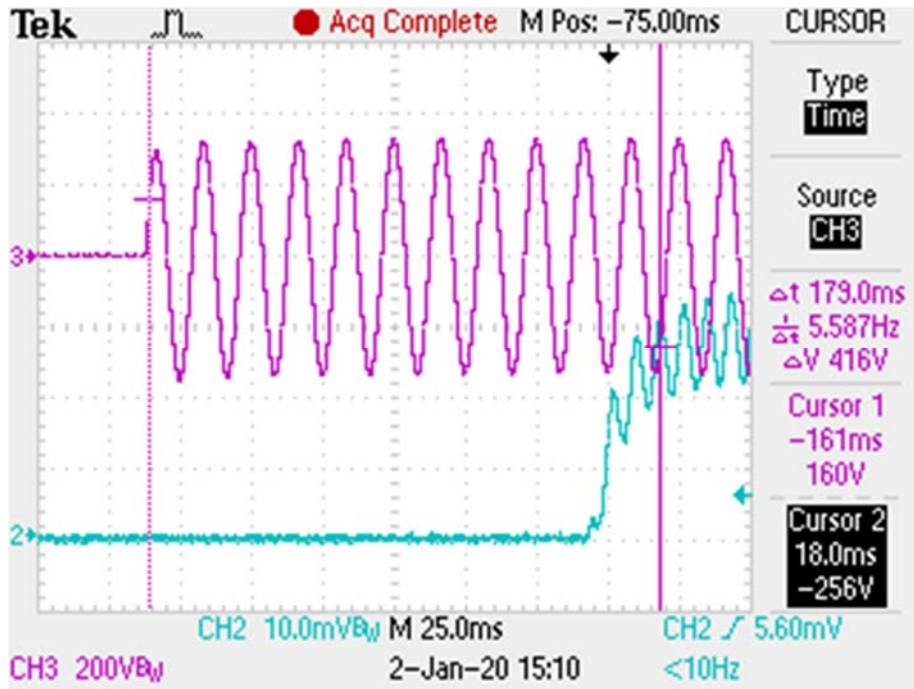


Figure 10. Full Load Start Up with 230 V ac Input

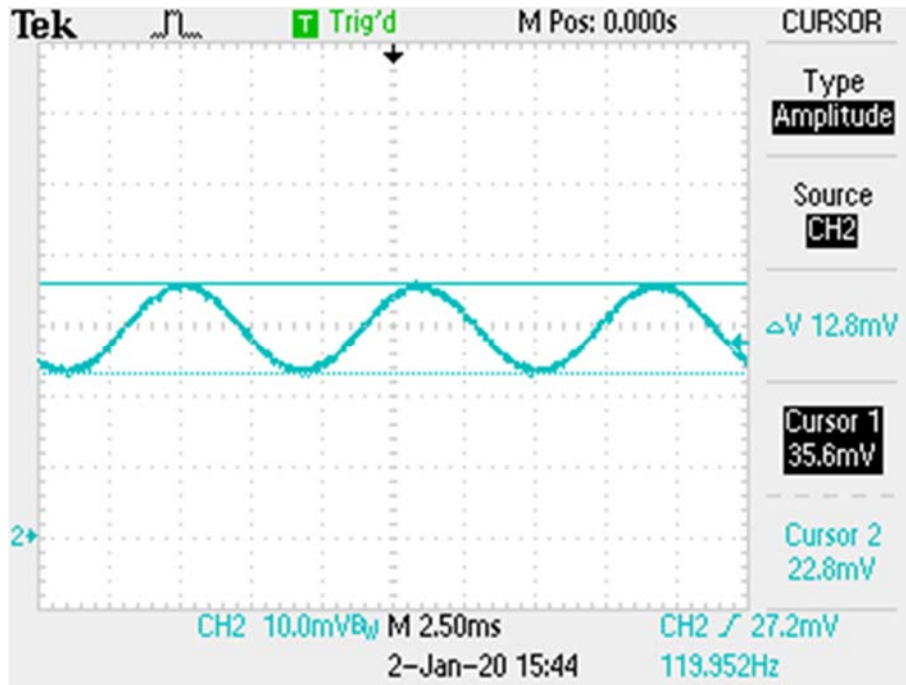


Figure 11. Output Ripple Current with 120 V ac Input

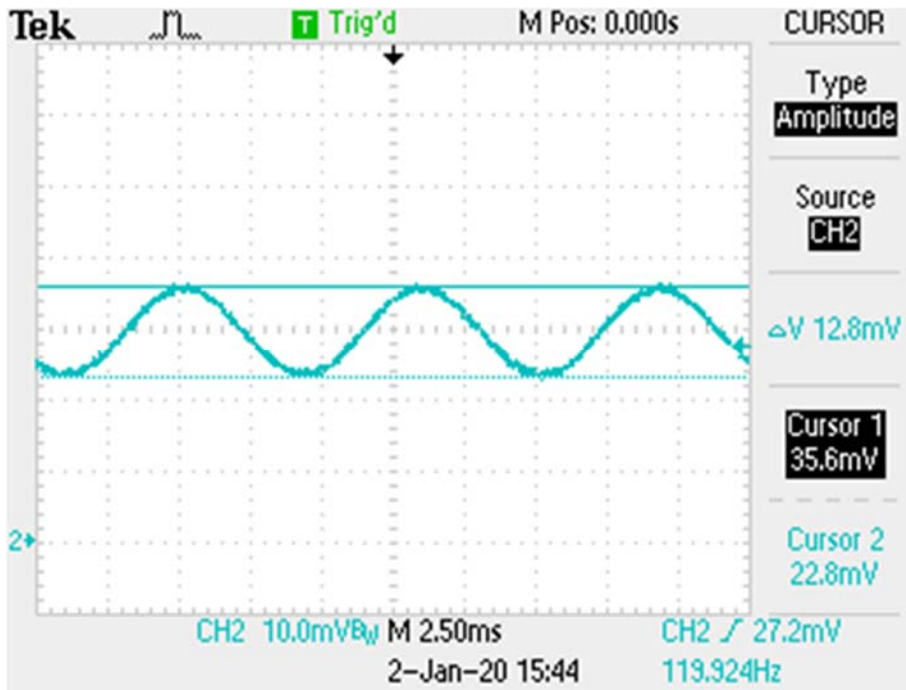


Figure 12. Output Ripple Current with 230 V ac Input